Cooling of Power MOSFETs in Electrical Power Steering Systems

The latest surface mount power packages work in parallel with thermal substrates and interface materials to reduce the number of MOSFETs required, as well as size and complexity, when building drives and controls for electrical vehicle power steering systems. **Nico Bruijnis, The Bergquist Company, Laren, The Netherlands**

Electro-Hydraulic Power Steering (EHPS) and Electrical Power Steering (EPS) are favoured by car makers seeking to reduce weight, trim costs, and add new features to increase performance and driver satisfaction. Both types of systems deliver benefits including enhanced fuel economy, system independence from the engine, modularity, scalability and programmability. Leading tier one suppliers already have a number of EHPS and EPS systems, typically using a Permanent Magnet AC (PMAC) or Brushless DC (BLDC) motor, mounted in the steering column or on the steering rack. The motor delivers assist-torque directly to a gear on the steering rack in the case of EPS, or may drive a fluid pump that assists the steering rack in the case of EHPS.

Controller ratings and design

Electrical power assistance systems are characterised in terms of the rack assist torque and force delivered. In an EPS system, a motor power of around 500W may provide up to 10,000N of assist force or around 90Nm of assist torque. Systems for larger cars may employ a motor in the region of 800W.

Drivers for BLDC and PMAC motors in EPS and EHPS systems tend to be three-phase inverters, converting the 14VDC vehicle supply to a three-phase AC supply for smooth speed-and-torque control. When choosing MOSFETs or IGBTs for the inverter bridge, power designers are already turning to enhanced surface mount power packages that use multi-lead construction and large leadframe T-post design, as well as die-on-leadframe or die-on DBC technology, to minimise die-free package resistance and increase current carrying capability. Another aspect of the role of these enhanced power packaging technologies is to remove heat efficiently from the MOSFET or IGBT die. Despite having low on-resistance to minimise losses, high peak currents approaching - and in some cases exceeding - 100A lead to significant heat generation. Switching losses inside the transistor also generate heat that must be removed sufficiently quickly from the die to prevent overheating of the device.

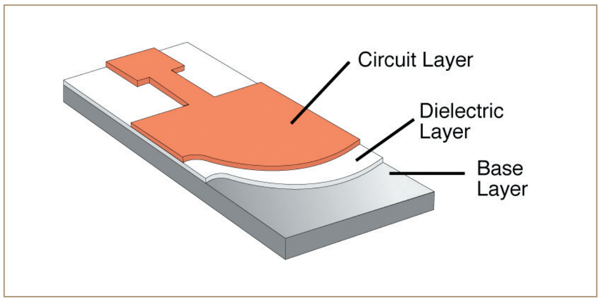

Figure 1: Construction of the IMS

Thermal design

Fortunately, the measures employed to reduce die free package resistance in packages such as D2Pak also serve to establish a path of low thermal resistance along which heat can escape to the edge of the package. Other package-level techniques to aid thermal management include embedding a large heat slug to be soldered directly to the PCB, as well as measures to extract heat through the top surface of the device. These high-performance package technologies such as D2Pak and other techniques create a low thermal resistance path from the die to the edge of the package. However, measures to continue the efficient removal of heat from this point into the heatsink are the responsibility of the system integrator.

The usual solution is to conduct the heat dissipated in the MOSFET or IGBT bridge into the vehicle chassis, which effectively provides an infinite heatsink. This may be achieved by maximising the thermal path from the transistor package through the substrate and controller casing into the chassis. Typically, an Insulated Metal Substrate (IMS) is used, as an ordinary FR4 PCB substrate does not offer sufficient thermal conductive performance to transport the heat away from the devices.

Insulated Metal Substrate (IMS) provides a high-performance alternative technology. IMS is a composite construction, typically comprising an aluminium or copper baseplate that not only increases the thermal capacity of the PCB, but also improves heat dissipation into ambient or into a larger heatsink, if used. A thin, thermally-conductive dielectric layer insulates the metal baseplate from the circuit layer that

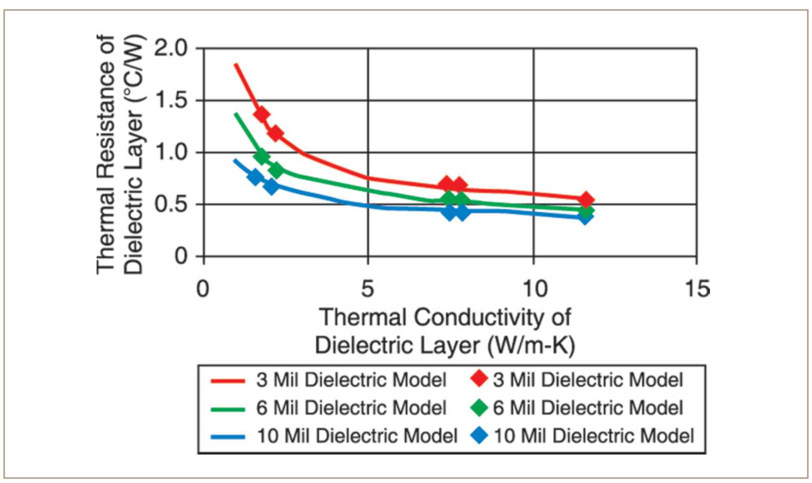

Figure 2: Thermal impedance versus thermal conductivity at different thicknesses for the dielectric layer

provides the interconnect between the MOSFETs and other components mounted on the circuit board (Figure 1).

The dielectric layer is critical in the thermal management of power MOSFETs, since it is potentially one of the highest thermal resistance interfaces in the entire path from die to ambient. However, its specification also has an important bearing on the cost of the chosen IMS. Thermal Clad IMS i.e. has a 75µm dielectric with relatively high thermal conductivity and is available in different thermal conductivity ratings, as well as different glass-point temperatures. This insulation layer is critical in the thermal management of power transistors, because the isolation layer is potentially one of the highest thermal resistance interfaces in the stack. Thermal impedance depends, among a variety of factors, on thermal conductivity and thickness. Figure 2 depicts thermal impedance versus thermal conductivity at different thicknesses for the dielectric layer.

The overall thermal resistance of the build is where

$$R_{Total} = \sum_i R_i$$

- R_i is bulk or interfacial resistance
  -Conduction $R_b = L/kA$
- Interfacial resistance must be determined empirically (generally small, but not always)
  -Convection $R = 1/hA$

The overall power dissipation in a given temperature rise

$$q = \frac{T_2 - T_1}{R_{Total}}$$

is

Hence, it can be seen that the overall temperature rise

$$T_2 = T_1 + qR_{Total}$$

for a given power dissipation is

Then the following formula may be used to calculate the total

$$\frac{q}{A} = -k\frac{dT}{dx}$$

heat transfer for the stack, from the heat source to the chassis.

Power that can be dissipated under a given temperature constraint is then influenced by:
- area of the layer [A],
- the thermal conductivity [K],
- the thickness of the layer[dx] and the power [q].

These simple equations are good for first approximations of temperature rise in power transistor designs. However, bench top testing and data confirmation are advisable to verify the design. A thin layer of thermal interface material is also required between the baseplate of the IMS and the casing. This should only be of sufficient thickness to overcome any physical irregularities in the surface, and should not contribute substantially to the thermal stack.

Sil-Pad 1200 (Figure 3) i.e. is a silicone based fiberglass-reinforced thermal interface material, featuring an optional adhesive coating. The material's smooth and non-tacky surfaces allow for easy re-positioning and error reduction in assembly. Sil-Pad 1200 is supplied without a liner in dry form and on a carrier liner when supplied with optional adhesive coating. It is available in sheets, rolls,
die-cut parts of any shape or size and slit-to-width roll form, with a standard thickness of 0.229mm. Standard sheet size is 305mm x 305mm, and the standard roll size offered is 305mm x 76m.

Conclusion

As electrical subsystems take over vehicle subsystems that traditionally demand large quantities of torque or power, the thermal properties of power packages, PCB substrates and thermal interface materials are critical to implementing solutions that meet the expectations for cost and performance and reliability.

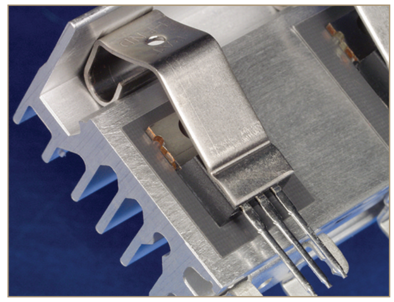

Figure 3: Application of Sil-Pad 1200, a silicone based fibreglass-reinforced thermal interface material