Transfer Mold IPM for Photovoltaic Application

A new low loss large Dual In-line Package Intelligent Power Module with rating of 50A/600V is designed for photovoltaic generation. It features a high heat dissipating insulation sheet, 5th generation CSTBT IGBTs and high output current driver IC leading to higher switching frequencies. **Ming Shang, Hirofumi Oki, Kazuhiro Kuriaki, Toru Iwagami, Toshiya Nakano, Power Device Works, Mitsubishi Electric Corporation, Fukuoka-City, Japan**

Mitsubishi Electric manufactured the Dual In-line Package Intelligent Power Module (DIPIPM™) with transfer mold structure from 1997, and since that it has been adopted as the inverter driver of appliances or industrial motors. Low loss photovoltaic large DIPIPM is (PV DIPIPM) developed in respond of the current, fast growing photovoltaic generation market (Figure 1) providing a good trade-off between efficiency and cost. Figure 2 shows a typical block diagram of a photovoltaic inverter. Here the DIPIPM is used as a DC/AC converter to convert the DC electricity to AC electricity.

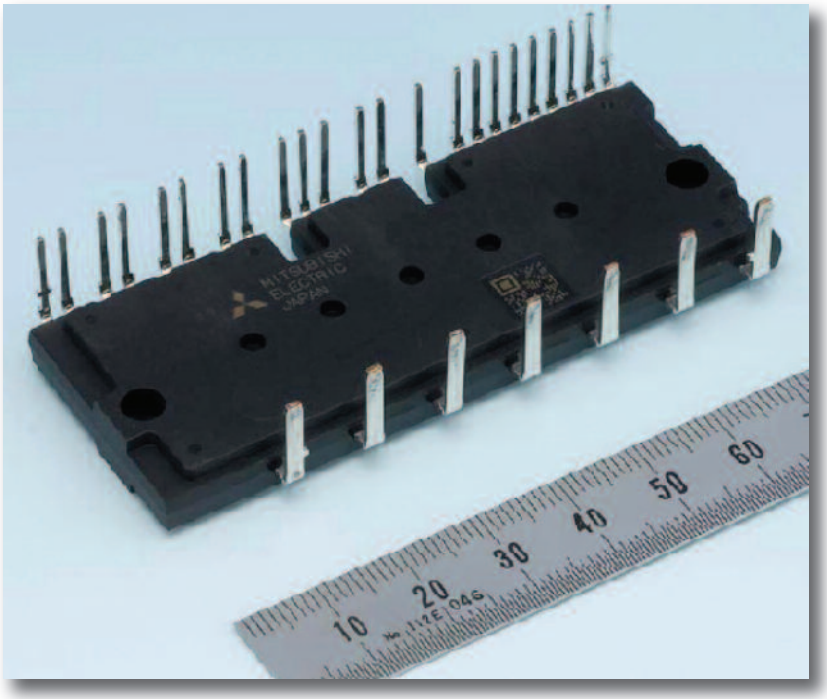

Figure 1: **Photovoltaic 50A/600V DIPIPM with package size of 79mm x 31mm**

Improved IGBT structure

PV DIPIPM adopts the Carrier Stored Trench-Gate Bipolar Transistor (CSTBT™) chip with full gate structure, in order to improve the trade-off relationship of on-state voltage and turn-off loss achieving a loss reduction of about 10% compared with conventional CSTBT (plugged cell merged CSTBT). Figure 3 shows the structure of full gate CSTBT, Figure 4 the structure of plugged cell merged CSTBT.

In a normal IGBT, the resistance of the n-drift layer has to be kept high in order to withstand the blocking voltage at off-state. As the hole injection from collector to n-drift layer at on-state, the resistance of the n-drift layer is reduced, and power loss is reduced. However, the resistance of the n-drift layer near emitter side is difficult to deduce because the hole density here becomes low due to the far away distance to the collector. Hence, it is difficult to achieve a very low on-state voltage.

CSTBT reaches a much lower on-state voltage by the virtue of optimization of the hole density in the whole n- drift layer. A special n barrier called n barred layer is designed under the P base layer to hinder the holes injected from the collector from penetrating to the emitter. This makes the further reduction of the on-state voltage possible because hole density is increased in the n-drift layer even near the emitter side. However, the major hurdle prevent full gate CSTBT from being used in our past design of DIPIPM are it's large gate input capacitance and weak short-circuit withstand ability which need a new driver IC wafer process.

In order to reduce the input capacitance, conventional CSTBT was developed to be with high current carrying capability, sometimes it is designed in a structure called

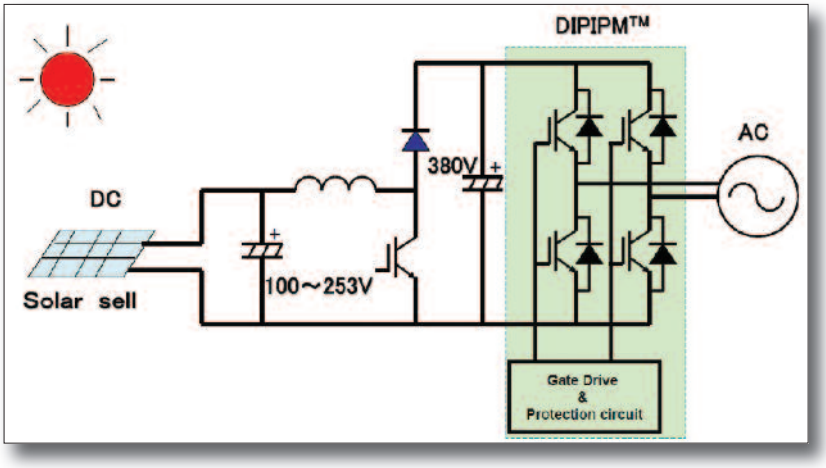

Figure 2: **Typical block diagram of photovoltaic generation system**

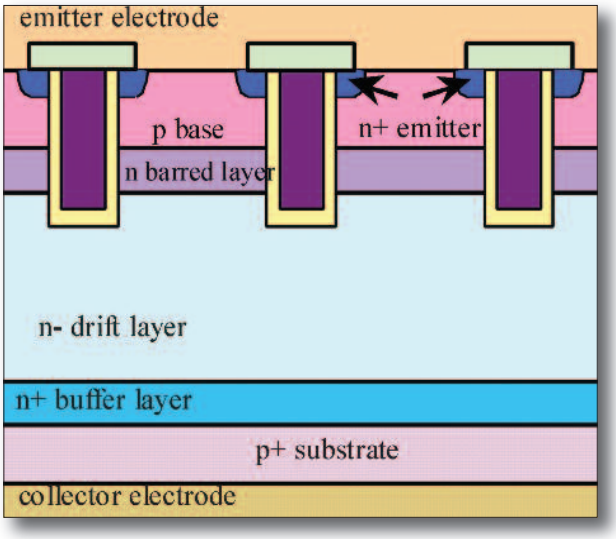

Figure 3: **Structure of full gate CSTBT**

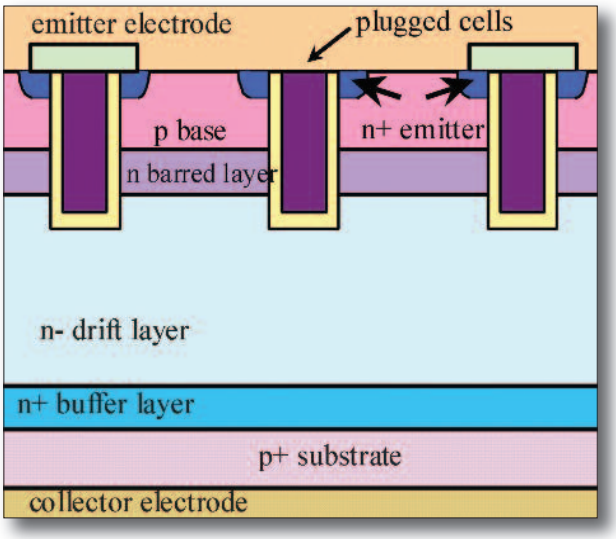

Figure 4: **Structure of plugged cell merged CSTBT**

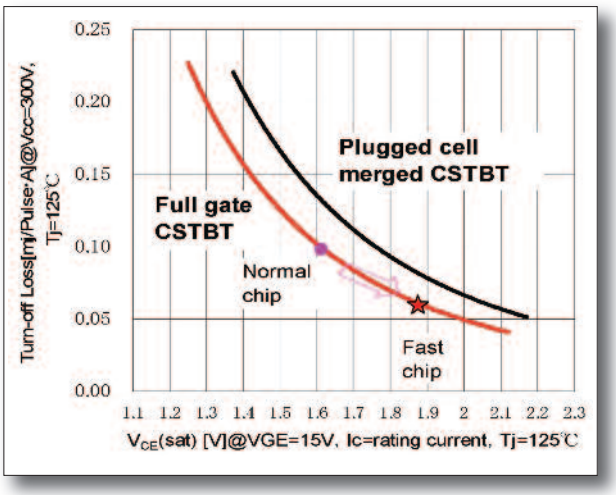

Figure 5: **Trade-off characteristic of CSTBT**

plugged cell merged CSTBT so as to ensure a certain withstanding capability against short circuit failure (Figure 4). With this structure the cell pitch is adjusted by "plugging" some portion of the cells in a conventional high cell density device. The polysilicon in the "plugging" cell is connected to the emitter electrode. Therefore, the CSTBT was not able to use 100% of performance in this structure.

Because the converter used for photovoltaic generation system applies fast switching, reducing the switching power loss could be a very effective way to enhance the whole system efficiency. In order to achieve an optimized trade-off relation between on-state voltage and turn-off loss, our PV DIPIPM adopted the fast full gate CSTBT chip combined with the advanced driver IC that is capable to handle higher short circuit current. Figure 5 shows the improvement of the trade-off between on-state voltage

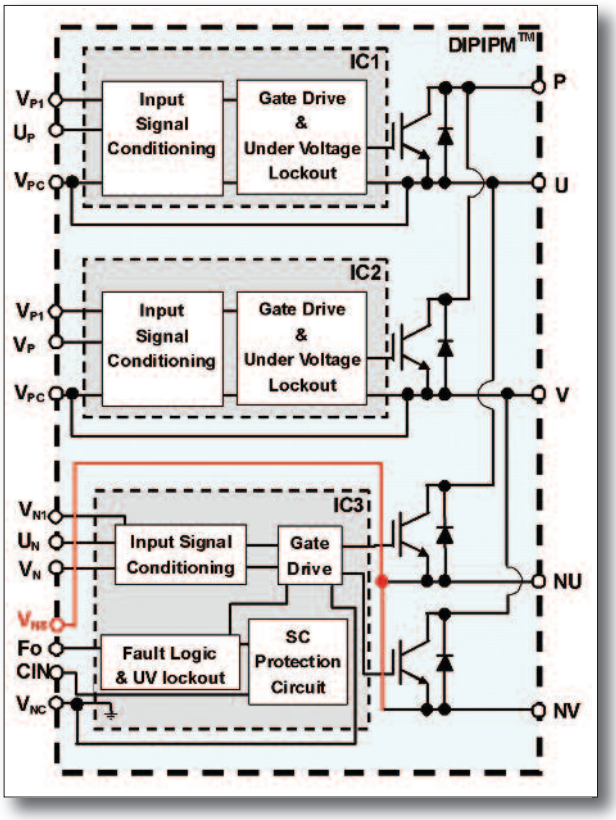

Figure 6: **Internal block diagram of Photovoltaic DIPIPM**

the full gate CSTBT needs larger drive capability than a plugging cell, the fine process technology can realize an IC with high drive capability without sacrificing chip size.

Circuit configuration and components

The internal circuitry of PV DIPIPM is composed of IGBTs and FWDs (Free Wheel Diode) in a two-phase inverter structure together with control ICs, which make it different from normal large DIPIPM Ver. 4. Figure 6 shows the internal block diagram of the PV DIPIPM.

Control ICs realize functions such as IGBT drive, under-voltage (UV) lockout, short circuit (SC) protection and fault signal output (FO). The output current of control IC gate driver circuit is up to 5A ensuring high speed IGBT switching.

When DIPIPM is used in fast switching mode, a balanced operation of upper and lower arm power chips is difficult to be achieved. This is because the N-side IGBT's VGE could be significantly lower than the power supply V_{N1}, due to the effect of ΔV1 ($\Delta V1 = I_o \times R$), generated by the shunt resistor (R) and ΔV2 ($\Delta V2 = di/dt * L$), generated by the parasitic inductance (L) of the external circuit.

In order to minimize the side-effect of ΔV1 and ΔV2, an extra control terminal pin V_{NS} is internally connected to the emitter of N-side IGBT (as is shown in Figure 6). Meanwhile, an external opto-coupler is needed to maintain the isolation between power GND and control GND, since the short-circuit protection signal can not be taken directly by shunt resistor voltage sampling. External short-circuit protection circuit is shown in Figure 7. Experimental result has proved that switching power loss of IGBT chip was reduced 13% when compared with non-V_{NS} pin PV modules.

Loss simulation

Figure 8 shows inverter loss simulation result imitated two phases modulation sinusoidal waveform. This fast CSTBT reduced switching power loss compared with a conventional CSTBT leads to a 20% increase in efficiency.

Conclusions

A new low loss Photovoltaic DIPIPM in a large package has been developed by applying fast full gate CSTBT and its optimized drive IC, together with the high-efficient heat dissipating insulation sheet.

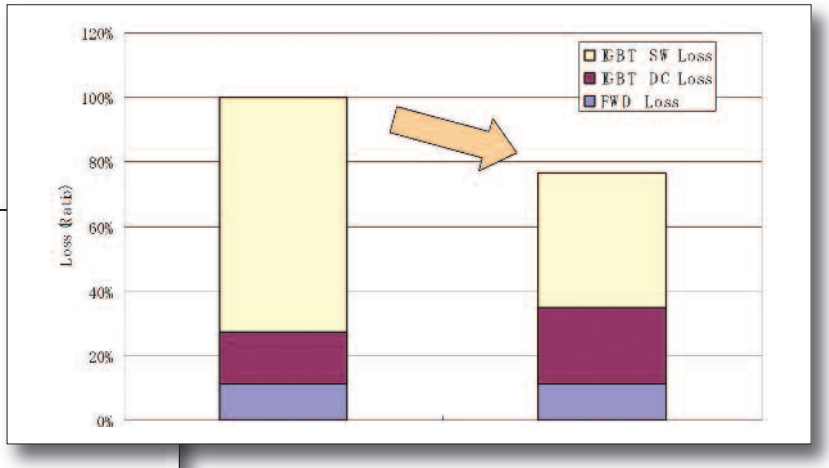

Figure 8: **Power loss comparison (Conditions: T_j=125_, V_{cc}=380V, V_D=15V, I_o=15Arms, PF=0.95, f_{sw}=15.5kHz)**

By adopting the high-speed full gate CSTBT, 10% of IGBT power loss was reduced. By changing the drive circuit of N-side IGBT, since 13% of IGBT switching loss reduction was realizable, 20% of module total loss reduction was realized.

Literature

Shang Ming: "New Low loss Transfer Mold IPM for Photovoltaic Generation", PEE Special Session "Power Electronics for Efficient Inverters in Renewable Energy Applications", PCIM Europe 2010, May 4, Room Paris

($V_{CE(sat)}$) and turn-off loss.

The internal IC provides optimized drive for the full gate CSTBT and realizes high function by means of the 0.5μm shrink process technology. The traditional offset structured transistor has been finely processed in the lateral direction by combining shallow junction technology which increases the output capability without enlarging the chip size. Although

Figure 7: **Short circuit protection circuit of Photovoltaic DIPIPM**