Application of Silicon Carbide MOSFETs

The Cree SiC MOSFET has removed the upper voltage limit of silicon MOSFETs. However, there are some differences in characteristics when compared to what is usually expected with high voltage silicon MOSFETs. These differences need to be carefully addressed to get maximum benefit from the SiC MOSFET. In general, although the SiC MOSFET is a superior switch compared to its silicon counterparts, it should not be considered as a direct drop-in replacement in existing applications. **Robert Callanan, Application Engineering, Cree Inc., Durham, USA**

There are two key characteristics that need to be kept in mind when applying the SiC MOSFET (see Figure 1): modest transconductance requires that V_{GS} needs to be 20V to optimize performance. This can be see in the Output and Transfer Characteristics shown in Figures 2-4. The modest transconductance also affects the transition where the device behaves as a voltage controlled resistance to where it behaves as a voltage controlled current source as a funtion of V_{DS}. The result is that the transition occurs over higher values of V_{DS} than are usually experienced with Si MOSFETs and IGBTs. This might affect the operation anti-desaturation circuits, especially if the circuit takes advantage of the device entering the constant current region at low values of forward voltage.

The modest transconductance and short-channel effects are important, the CMF20120D needs to be driven with a higher gate voltage swing than what is customary with SJMOSFETS or IGBTs. Presently, a +20V and -2V to -5V negative bias gate drive is recommended. Care needs to be taken not to exceed -5V in the negative region. The rate of rise of gate voltage will have a greater effect on the rate of rise of the drain current due to the transconductance. Therefore, the gate drive needs to supply a fast rise and fall time gate pulse to maximize switching speed. The device also has a threshold voltage similar to the Si SJMOSFET (2V nominal). Like the SJ MOSFET, considerations need to be made for the lower threshold voltage, especially at high temperatures.

The rather large triode region can have an impact on certain type of fault detection schemes, mainly the active de-saturation circuitry. Some of these designs assume that the switching device enters a fairly high impedance constant current and/or transconductance saturation region during over-current faults. For the CMF20120D, the output impedance is lower and the device does not go into a clean constant current region during this type of over-current fault, especially under moderate over-currents. Therefore, the drain-to-source voltage will not increase as much. These characteristics of the SiC MOSFET need to be carefully considered in fault protection schemes.

Gate drive requirements

The modest transconductance needs to be carefully considered also in the design of the gate drive circuit. The first obvious requirement is that the gate be capable of a >22V (+20V to -2V) swing. The recommended on state V_{GS} is +20 V and the recommended off state VGS is between -2V to -5V. Please carefully note that although the gate voltage swing is higher than the typical silicon MOSFETs and IGBTs, the total gate charge of the SiC MOSFET is considerably lower. In fact, the product of gate voltage swing and gate charge for the SiC MOSFET is lower than comparable silicon devices. The gate voltage must have a fast dV/dt to achieve fast switching times which indicates that a very low impedance driver is necessary.

Lastly, the fidelity of the gate drive pulse must be carefully controlled.

The nominal threshold voltage is 2.5V and the device is not fully on ($dV_{DS}/dt \approx 0$) until the V_{GS} is above 16V. This is a noticeably wider range than what is typically experienced with silicon MOSFETs and IGBTs. The net result of this is that the SiC MOSFET has a somewhat lower 'noise margin'. Any excessive ringing that is present on the gate drive signal could cause unintentional turn-on or partial turn-off of the device. The gate resistance should be carefully selected to ensure that the gate drive pulse is adequately dampened. To first order, the gate circuit can be approximated as a simple series

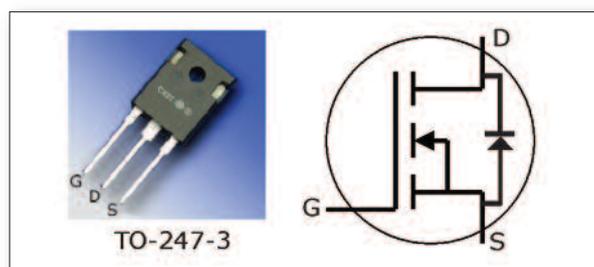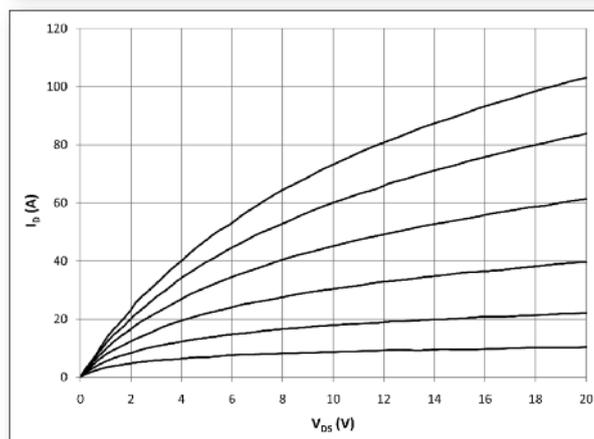**Figure 1: 1200V SiC MOSFET package and schematic**

Figure 2: Typical output characteristics at 25°C junction temperature of SiC MOSFET at V_{GS}=20V (upper curve), 18V, 16V, 14V, 12V and 10V (lower curve)
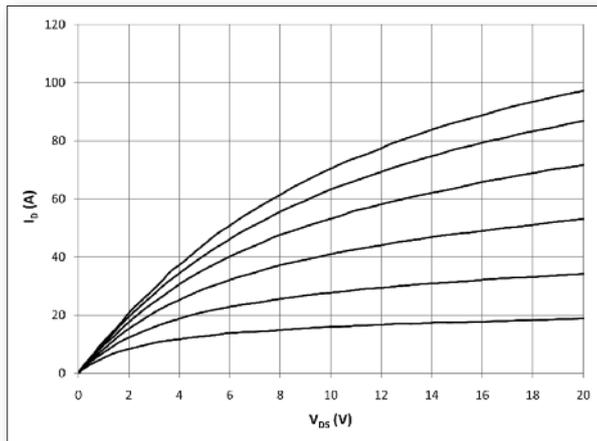
Figure 3: **Typical output characteristics at 125°C junction temperature of SiC MOSFET at VGS=20V (upper curve), 18V, 16V, 14V, 12V and 10V (lower curve)**
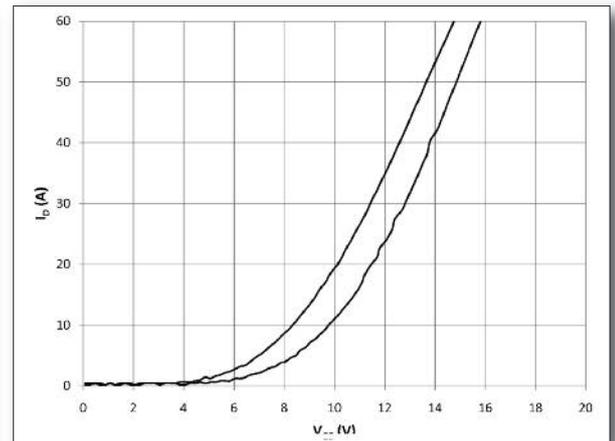

Figure 4: **Typical transfer characteristics at 125°C (upper curve) and 25°C junction temperature of SiC MOSFET**

RLC circuit driven by a voltage pulse as shown in Figure 5.

As shown, minimizing L$_{Loop}$ minimizes the value of RLoop needed for critical dampening and also minimized the rise/fall time. Therefore, it is strongly recommended that the gate drive is located as close to the SiC MOSFET as possible to minimize L$_{Loop}$. The internal gate resistance of the SiC MOSFET is 5Ω. An external resistance of 6.8Ω was used to characterize this device. Lower values can be used so long as the gate fidelity is maintained. If no external gate resistor is used, it is suggested that the gate current be checked to indirectly verify that there is no ringing present in the gate circuit. This can be accomplished with a very small current transformer as shown in Figure 6.

The 2-stage current transformer first stage consists of 10 turns AWG30 wire on a small high-permeability core such as Ferroxcube 3E27. The second stage is a small wide-bandwidth current transformer such as the Tektronix CT-2. Lastly, a separate source return should be used for the gate drive.

The used gate driver is an IXYS IXDI414. This device has a 35V output swing, output resistance of 0.6Ω typical, and a peak current capability of 14A. The external gate resistance for characterization of the SiC MOSFET was 6.8Ω. Careful consideration needs to be given to the selection of the gate driver. The typical application error is selection of a gate driver that has adequate swing, but output resistance and current drive capability are not carefully considered. It is critical that the gate driver possess high peak current capability and low output resistance along with adequate voltage swing.

A significant benefit of the SiC MOSFET is the elimination of the tail current observed in silicon IGBTs. However, it is very important to note that the current tail does provide a certain degree of parasitic
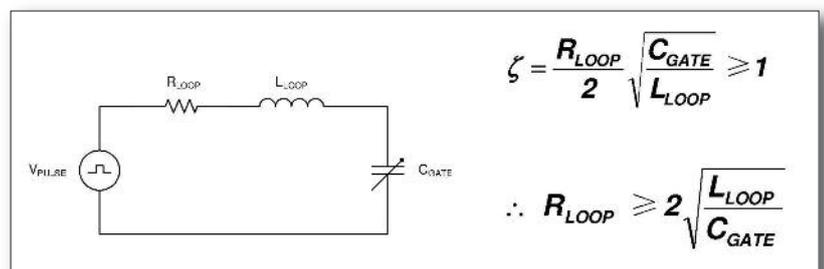

$$\zeta = \frac{R_{LOOP}}{2}\sqrt{\frac{C_{GATE}}{L_{LOOP}}} \geqslant 1$$

$$\therefore \; R_{LOOP} \geqslant 2\sqrt{\frac{L_{LOOP}}{C_{GATE}}}$$

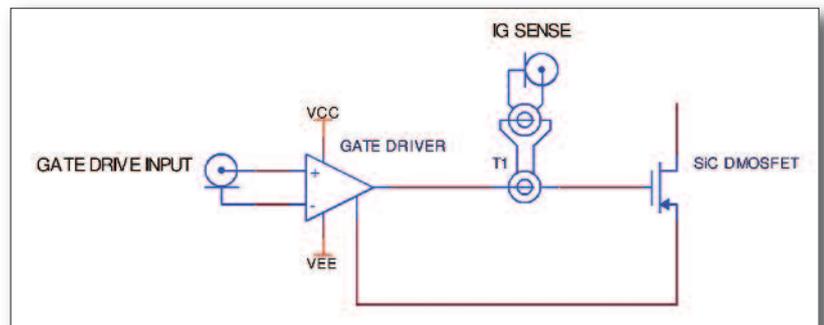Figure 5: **Approximated gate circuit**

Figure 6: **Recommended setup of a 2-stage current transformer for gate driving**

dampening during turn-off. Additional ringing and overshoot is typically observed when silicon IGBTs are replaced with SiC MOSFETs. The additional voltage overshoot can be high enough to destroy the device. Therefore, it is critical to manage the output interconnection parasitics (and snubbers) to keep the ringing and overshoot from becoming problematic.

Conclusions

The CMF20120D has definite system advantages over competing Si switching devices. However, its unique operating characteristics need to be carefully considered to fully realize these advantages. The gate driver needs to be capable of providing +20V and -2V to -5V negative bias with minimum output impedance and high current capability. The

parasitics between the gate driver and the CMF20120D need to be minimized (close location, separate source return, etc.) to assure that the gate pulse has a fast rise and fall time with good fidelity. The fast switching speed of the CMF20120D can result in higher ringing and voltage overshoots. The effects of parasitics in the high current paths need to be carefully assessed.

Literature

"First Commercial Silicon Carbide Power MOSFET Launched by Cree", PEE 1/2011, page 21-22

"Application Considerations for Silicon Carbide MOSFETs", PEE 3/2010, page 40-43

"Pros and Cons for Silicon Carbide MOSFETs, JFETs and BJTs", PEE 5/2009, page 19-22