Power Module Design for an Efficient Three-Level Utility Grid Solar Inverter

The race to achieve highest efficiency had engineers turning to innovative topologies and new components such as SiC to take the lead. In parallel, after years of dormancy, old but very innovative ideas such as the mixed-voltage NPC topology have been rediscovered and put to good use in many solar inverter applications. Surprisingly, all these efforts have focused on the power range up to 100kW, while standard two-level topologies with low switching frequencies continue to dominate in the range beyond 100 kW. The new power module design transcends the limitations associated with >100 kW power inverters to accommodate high switching frequencies and innovative topologies based on standard Si components.

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Parasitic effects such as stray inductance and diodes' reverse recovery characteristics are the main obstacles to achieve high switching frequencies for ultra high efficiency solar inverter applications ranging beyond 100 kW. The overvoltage spike caused by parasitic inductance limits the turn-off switching speed. And increased turn-on switching speed comes at a high price - losses and increased electromagnetic interference (EMI) caused by the freewheeling diode's reverse recovery characteristics. The new power module design described here takes advantage of advances in power modules - for example, the 3-level topologies used in low-power solar applications - and exploits this parasitic inductance to reduce turn-on losses. Parasitic inductance at turn-off can be bypassed with low-inductive transient current management. A special topology for paralleling MOSFET with IGBT is presented here to show how promising the prospects of this advanced new module design can be.

Standard 2-level inverters achieve around 95 % efficiency at 16 kHz, so a 200 kW inverter will suffer about a 10 kW loss. Power dissipation has to be reduced by 80 % to achieve the targeted 99 % efficiency. This can be done by minimizing switching losses in four 4 steps:

- Reduce the switched voltage with a three-level topology.
- Use a low inductive design that accommodates fast components.
- Achieve asymmetrical inductance, reduce turn-on losses and regenerate energy stored in the parasitic inductance.
- Capitalize on the benefits of advanced paralleling.

Why a three-level topology?

Three-level topologies are certainly known for reducing switching losses ($P_D = \int I_{CE(t)} \times V_{CE(t)} \times dt$), but this is not their only advantage. The reduced current ripple halves the output filter effort and losses at the same PWM frequency.

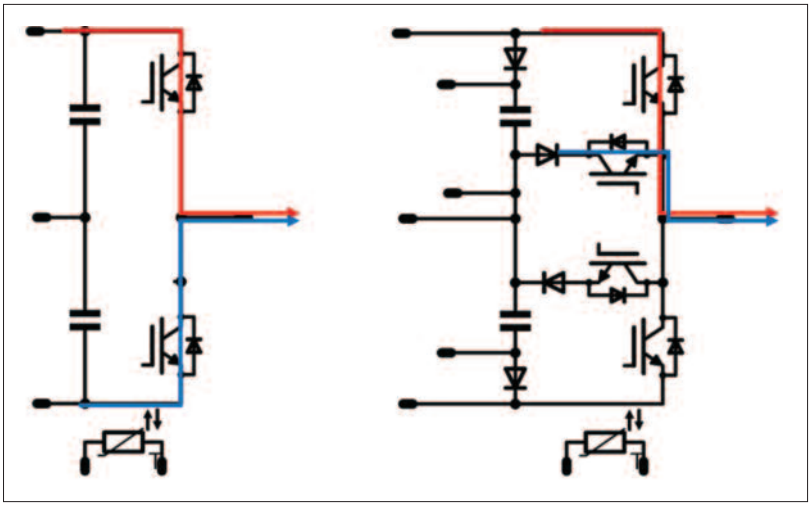
Reducing the switched voltage also reduces switching losses by 50 %. An additional reduction is possible because of the freewheeling diode's lower voltage rating. With the benefit of a mixed-voltage neutral clamped converter (MNPC) topology, the freewheeling diodes' voltage rating is just half that of a two-level half-bridge. The blocking voltage drops from 1200 V to 600 V (Figure 1). The 600 V diodes' reverse recovery charge is much lower, which reduces turn-on losses. The total turn-on losses are calculated as the sum of the diode's reverse recovery losses and turn-on losses in the switch, which are also influenced by the freewheeling diode's recovery characteristics.

All this reduces total losses by 50 % (turn-on and turn-off) with a 3-level topology, and by 30 % to 60 % (turn-on) with 600 V diodes, depending on the switch's characteristics.

Low inductance for fast components

While fast diodes reduce turn-on losses, require fast switches a low-inductive design that solves the problem of voltage overshoot at turn-off ($V_{CE(peak)} = V_{CE} + L \times dI/dt$).

High inductance precludes the use of fast components with high di/dt at turn-off.



LEFT Figure 1: Switched current and freewheeling path in a 2-level inverter (left) vs. a 3-level MNPC inverter during a positive half wave

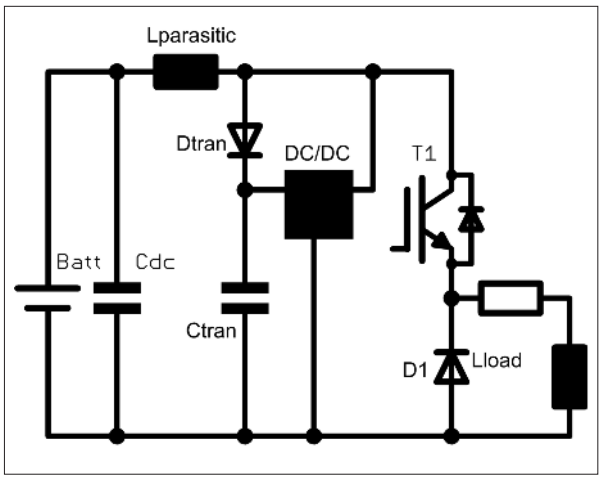


Figure 2: Asymmetrical inductance in a switching circuit with stored energy regeneration

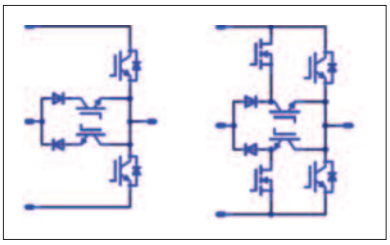


Figure 3: Mixed voltage NPC (left) and advanced paralleled NPC topology (right)

The overshoot dilemma increases with rising inductance (L) and switched current (I). Even lower inductance values are necessary to manage overcurrent and short-circuit problems. Reducing parasitic inductance also reduces voltage overshooting and turn-off losses. And it allows fast components to be used to accelerate turn-off, which is even more important to reducing switching loss. All this can reduce total turn-off losses by around 20 % to 60 %. Acceleration at turn-on also depends on the diode.

Regenerating Energy Stored in the Parasitic Inductance

The low inductive design and fast components already reduce switching losses, and the low-inductive environment also allows to exploit parasitic effects to further reduce switching losses and improve EMC. Inductance is very welcome at turn-on. However, ultra-low inductance is vastly preferable at turn-off – hence the term asymmetrical inductance.

The idea here is to make the most of parasitic inductance $L_{parasitic}$ at turn-on and avoid it altogether at turn-off. To this end, the diode D_{tran} consigns the energy stored in the parasitic inductance to the integrated capacitor C_{tran} during turn-off. The stored energy circulates in $L_{parasitic}$, D_{tran} and R_{tran} until it is dissipated in the parasitic resistor. Although we are able to relieve the semiconductor of switching losses with this circuit, some energy has to be dissipated in passive components. One way to increase overall efficiency is to regenerate energy stored in a DC/DC circuit (Figure 2).

The new asymmetrical setup's switching losses are lower. The overshoot at turn-off is minimized. Turn-off losses are lower. What's more, all switching losses are reduced. The circuit's reverse recovery behavior explains the lower turn-on losses. The reverse recovery current through diode D1 boosts the current of transistor T1 at turn-on. The current is reduced during recovery, but the additional energy stored in the parasitic inductance $L_{parasitic}$ causes an overvoltage at the transistor's collector, so the energy will flow into the capacitor. This reduces the reverse current in the diode. The voltage drops in the transistor, resulting in significantly reduced switching losses.

Advantages of the Asymmetrical Inductance include superior switching performance with standard components - increased turn-on inductance reduces peak current in the transistor, which is a major source of EMI. No laminated bus bars required - increased inductance in the DC input is now welcome and will further reduce loss at turn-on. This means the expensive laminated bus bars used for a low inductive connection with the DC capacitor bank are no longer necessary. Reduced voltage swing of onboard capacitors - these capacitors are not discharged during turn-on, so their voltage swing and dissipation is drastically reduced. The transient diode eliminates any ringing between the DC link and the onboard snubber capacitors. Asymmetrical inductance reduces switching losses by 10 % to 30 %, depending on the parasitic inductance, while extending the safe operating range at turn-off (RBSOA).

Advanced paralleling

The goal is to bring together the benefits of standard NPC (lowest switching losses) and mixed-voltage NPC (Figure 3 left) (lower static losses) topologies with a paralleled fast component (e.g. a MOSFET) and a component with low voltage drop (e.g. an IGBT) to create an advanced paralleled NPC topology (Figure 6 right). This special circuit allows a 1200 V IGBT to be paralleled with 600 V MOSFETs. Both the MOSFET and the IGBT are turned on simultaneously. The MOSFET is the faster device, so the current at turn-on flows to it. The IGBT turns on with low voltage. The voltage drop in the IGBT is lower, so then most of the current flows to the IGBT. The MOSFET's gate signal is delayed at turn-off. The IGBT turn offs, and then the MOSFET takes over the current and turn offs with a delay of 0.2 µs to 1 µs.

To get access to those advantages are some challenges to be solved. At parasitic turn-on the MOSFET turns off quickly, so the high dV/dt could send voltage into the paralleled IGBT's gate. It is already off, so this could trigger a parasitic turn-on. This

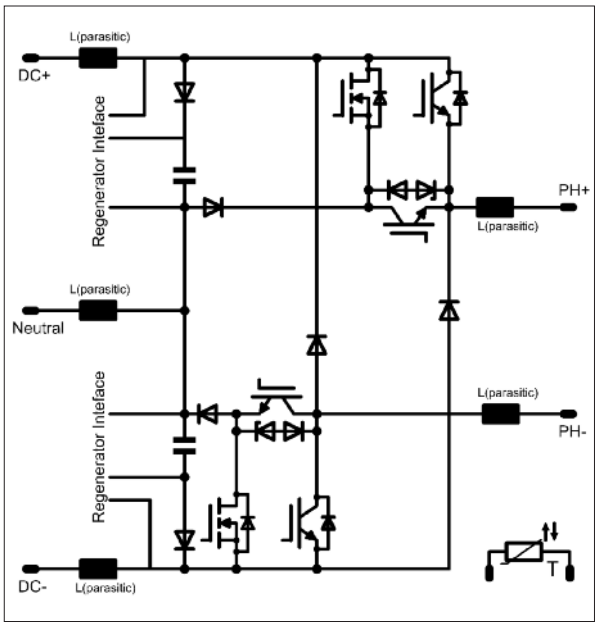


Figure 4: One phase of the 3-phase power module with advanced paralleled asymmetrical inductance, split output and regeneration interface

problem is remedied with a negative gate bias and/or a capacitor inserted between the gate and emitter.

Regarding IGBT tail current - current flows to the MOSFET after the IGBT switches off. The IGBT turns off at zero voltage, but it will conduct again if the space charge region is not fully rebuilt. Turn-off efficiency will suffer as a result of this tail current. This problem is fixed by setting an ideal delay time between the IGBT and MOSFET and/or selecting an IGBT with good zero-voltage turn-off behavior. Measurements show that the advanced paralleled NPC topology halves switching losses.

A power module with four efficiency improvements

Each of the four steps has been shown to be a viable improvement. And a module-based inverter solution proves how effective a combination of all four can be.

Figure 4 shows the inverter's circuit diagram (only one phase of three is shown). The inductance $L_{parasitic}$ represents the power module's stray inductance. The power module (Figure 5) incorporates all power semiconductors of the inverter, the snubber diodes and the snubber capacitors. The circuit converts DC voltage from the solar panel into a three-phase AC voltage for the public power grid. The inductors shown in the DC path ($L_{parasitic}$) represent the parasitic inductance in the DC power module's connection.

The three-phase inverter circuit and the output filter (inductor) convert DC current into a sinusoidal output current. The regeneration circuit connected to the inverter module regenerates the energy stored in the onboard capacitors.

Efficiency boost

The measured results serve to determine the efficiency of an inverter circuit. This calculation does not include losses of passive components such as the output filter and DC capacitors.

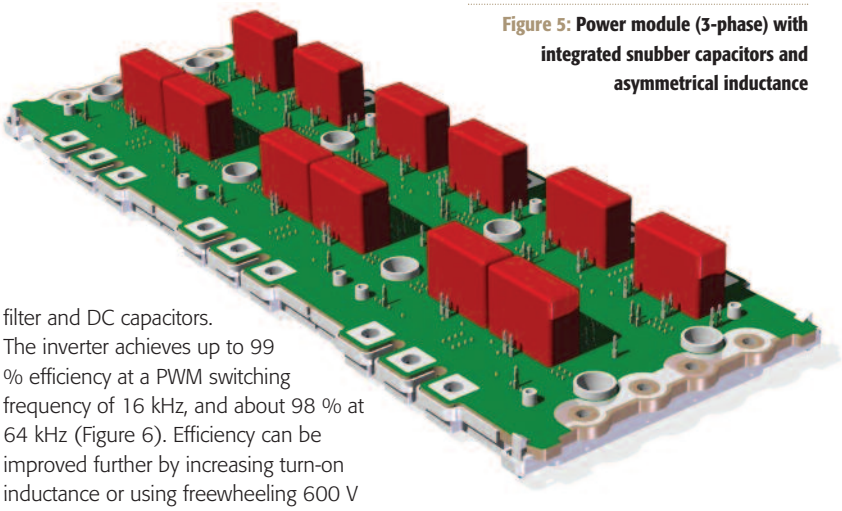


Figure 5: Power module (3-phase) with integrated snubber capacitors and asymmetrical inductance

The inverter achieves up to 99 % efficiency at a PWM switching frequency of 16 kHz, and about 98 % at 64 kHz (Figure 6). Efficiency can be improved further by increasing turn-on inductance or using freewheeling 600 V SiC diodes in the neutral path. It is expected that the version with SiC diodes will reduce turn-on losses by around 30 % to 50 % (Figure 7).

Conclusions

Conventional power designs can be improved by revisiting the fundamentals of power electronics.

Multilevel topologies have been with us for many years to satisfy widespread demand for higher efficiency. This type of topology reduces switching losses by at least 50 %. The low-inductive design ensures fast, reliable turn-off in high-current power modules and reduces voltage overshoot. Low inductive designs provide the platform for all other ideas about incorporating fast components, high transients and reduced switching losses in high-power applications. Asymmetrical inductance drives down switching losses, EMI and effort for inverter hardware. Low inductive bus bars are no longer necessary. A flexible, low-cost cable connection may used in the DC link. The parallel switch technology achieves highest efficiency at elevated switching frequencies of 50 kHz and beyond.

Further improvements with SiC freewheeling diodes in the neutral path is feasible

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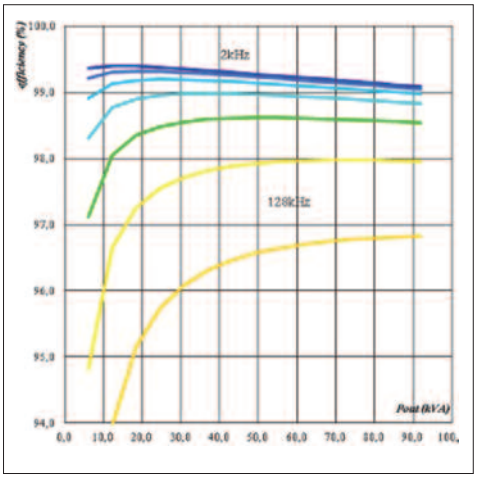
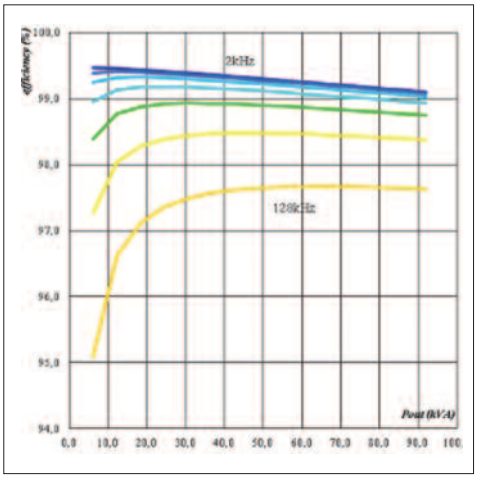


LEFT Figure 6: Advanced paralleled NPC - efficiency vs. switching frequency in steps from 2 kHz to 128 kHz: It doubles with each step – 2, 4, 8, 16 kHz (blue), 32 kHz (green), 64 kHz (yellow), 128 kHz (orange)



RIGHT Figure 7: Estimated efficiency with SiC diodes in the neutral