

An Effective Approach to Controlling of Multiple Voltage Rails

The process of powering-up the various voltage rails that accompany system-on-chips (SoCs), field-programmable gate arrays (FPGAs) and embedded modules in the correct order can be quite convoluted. Engineers therefore need to specify a suitable solution. As will be detailed in the following article, there are a multitude of ways in which modern sequencing technology can help to simplify the task.

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The contemporary processor-based designs upon which the embedded systems sector now relies all mandate that power is supplied at different voltages. As well as having different values, these voltage rails must be initiated in a specific sequence - the processor core, the related peripherals, the I/O buses (such as LVDS, I²C, SPI, etc.) and the memory resources all being attended to in turn. Through sequencing, the risk of large inrush currents that could potentially damage sensitive elements of the subsystem during the start-up process can be circumvented.

The trend towards increasing degrees of integration has meant that a greater proportion of an embedded system's functionality will generally be packed onto a single SoC device, in order to save board space and reduce bill-of materials (BoM) costs. Such SoCs need multiple power rails, each at the appropriate voltage level, to be applied to the associated pins. Those that are not SoC-oriented will often utilize programmable logic, with large FPGAs leaving engineers with similar (if not greater) power rail complexity to contend with. In some cases it may be necessary for this to be extended to other elements situated on the board - discrete devices (MOSFETs, IGBTs, etc.), sensors (CMOS imaging devices, magnetometers, etc.) or actuators (motor drivers, LED drivers, etc.) potentially requiring dedicated voltage lines.

More and more rails

Even a relatively simple embedded system implementation can have a considerable number of rails involved (over 10 not being uncommon today). Engineering effort will need to be allocated to ensure that the correct sequencing is adhered to - the output supplied by a given power

regulator having reached a sufficient level before regulators that are related to other voltage lines are activated. As it is more straightforward to measure timing in a precise manner than it is to measure voltage, often a time based approach is more effective - working on the principle that the value that is expected on a voltage rail will be attained in a predetermined period.

Though the time between the different rails being powered-up is normally very short (just a few milliseconds), it can potentially be much longer than this (several seconds in fact). For example, if some sort of electro-mechanical component within the system, such as a heater, needs to reach its optimum temperature prior to subsequent elements in the system being activated, or if the central processing unit has to complete a calibration procedure, then time will be taken up - and this needs to be recognized by the design engineer.

Where the discrete power converters that are incorporated into the system each respectively possesses enable pins and power-good outputs, engineers can use each power-good signal to ensure that the next converter in the sequence will only start when the preceding rail has attained an adequate value for that signal to continue to be asserted. If one or more of the converters does not have an enable input, engineers can achieve sequencing by using the turn-on signal to control the gate of a MOSFET placed in series with the output.

Under circumstances where there isn't any access to a power-good signal, engineers may need additional circuitry to provide the necessary assistance. Through this the output voltage of one power converter can be sampled to generate an enable signal for another power converter.

An alternative to voltage sampling is utilising timing circuitry. In either of these scenarios, however, a fairly large number of components is required - resulting in heavy BoM costs, substantial PCB real estate being used up and additional engineering resource needing to be allocated. Also are there issues associated with discretes providing a reverse sequence when the system is being powered down.

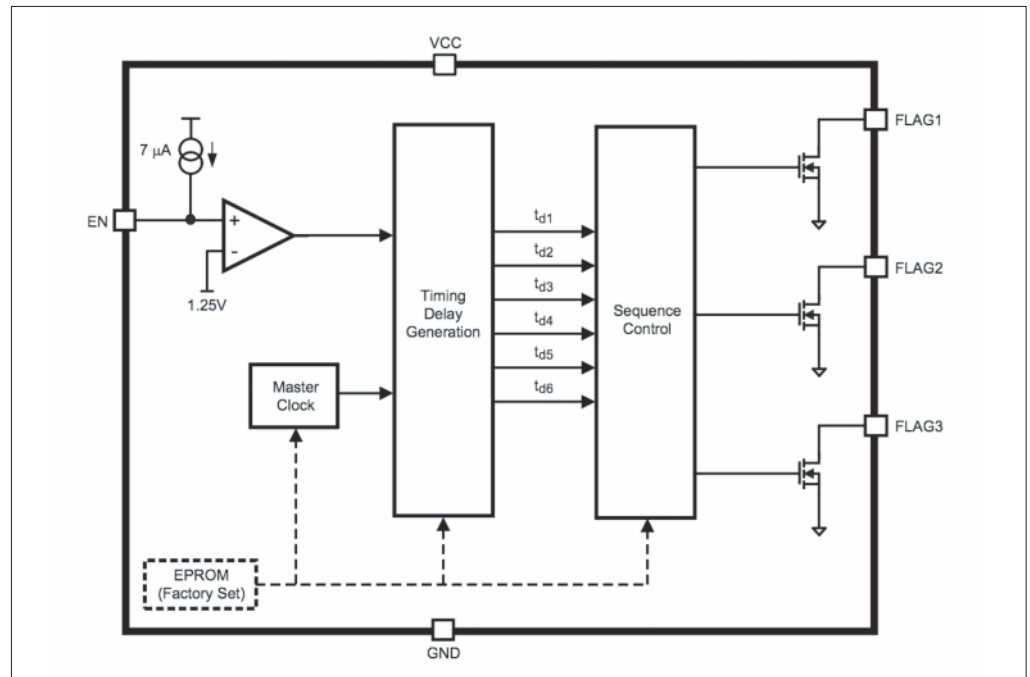
Rather than taking a discrete approach, engineers may find it more effective to look an integrated power-sequencing or PMIC-based alternative.

Integrated solutions

Offering straightforward implementation, Texas Instruments' LM3880 (see Figure 1) can be specified for power sequencing purposes (with the device's power-down procedure matching the same sequence and same time intervals as used in power-up, but in reverse). Thanks to its three open-drain output flags (which upon initiation of power-up are all held low), it has the capacity to generate enable signals to serve up to three individual voltage rails, with the option to cascade two sequencer ICs together in order to have six sequenced rails available. The PMIC incorporates its own precision enable input. This is connected to an internal comparator with a 1.25V reference. Through it engineers can arrange for the power-up sequence to begin once a logic signal is received, or when another voltage rail reaches a certain predetermined level. A delay can be included by attaching a capacitor to the enable input.

When the enable becomes valid, the first output flag is asserted after a preset delay (which is programmed into the EPROM during the OEM production process). An identical time period is then

Figure 1: Functional block diagram for the LM3880 from Texas Instruments



allowed to elapse before the second flag is set, and this is repeated once again before the third flag is set. Six different pre-set timing designations that span from 2 ms through to 120 ms can be chosen from.

Maxim’s MAX16029 supervisor device also has capacitor-adjustable time delay. It can be used to sequence up to four voltages rails via one single PMIC. The company also has sequencer devices in its portfolio that enable to set timing via PMBus interfaces. This means that a number of them can be daisy-chained together in order to address larger quantities of voltage rails.

By procuring sequencing technology in which multiple power source elements have been incorporated, engineers can benefit from marked reductions in board utilisation and overall system complexity. The TPS65916 PMIC from Texas Instruments’ has five configurable step-down converters integrated. These take care of powering the processor core, plus the various memory reserves and I/Os that are featured in a broad array of different microprocessor devices. By supporting adaptive voltage scaling, these converters are able to deliver power efficient operation that won’t impinge on the system’s power budget. The PMIC also contains five low voltage drop-out controllers to address low current or low noise domains. The power-up and power-down sequences can be configured by the engineer to suit their application via the one-time programmable memory.

Circumstances may dictate more

complicated sequencing will be required, with a greater breadth of voltage rails to take into consideration. In such cases the turn-on and turn-off sequencing must be managed with a higher degree of sophistication. Specifying a simple sequencer or a general-purpose PMIC may not be enough. What is needed instead is the full user-programmability of microcontroller unit (MCU).

The popular PIC16F1XXX family from Microchip (as shown in Figure 2) presents a power sequencing solution capable of dealing with a large number of voltage rails. Its user-programmable embedded firmware can be used to define the required timing. The device also offers ample provision for setting power-good criteria, as well as ramp-up and ramp-down periods. The 10-bit analogue-to-digital converter digitizes each rail 16 times and then calculates an average value (so that performance can be accurately

evaluated). The MCU’s diagnostic capabilities mean that if a supply fails the situation is rapidly flagged.

Conclusions

Ensuring that the appropriate sequence is used when powering-up/powering-down electronic circuitry is critical. Long term operational integrity can thus be maintained and system reliability is not in any way compromised. Solutions for this range all the way from basic sequencers right through to more feature-rich PMICs and fully programmable MCU devices. With a wealth of different options now on the market, it is simply a matter of assessing which sequencing method is best suited to the principal design objectives (whether that is maximizing performance, keeping the BoM down, dealing with space constraints, curbing system power consumption, etc.), then sourcing the necessary devices.

Figure 2: Microchip’s PIC16F1XXX family can support flexible power sequencing of numerous voltage rails

