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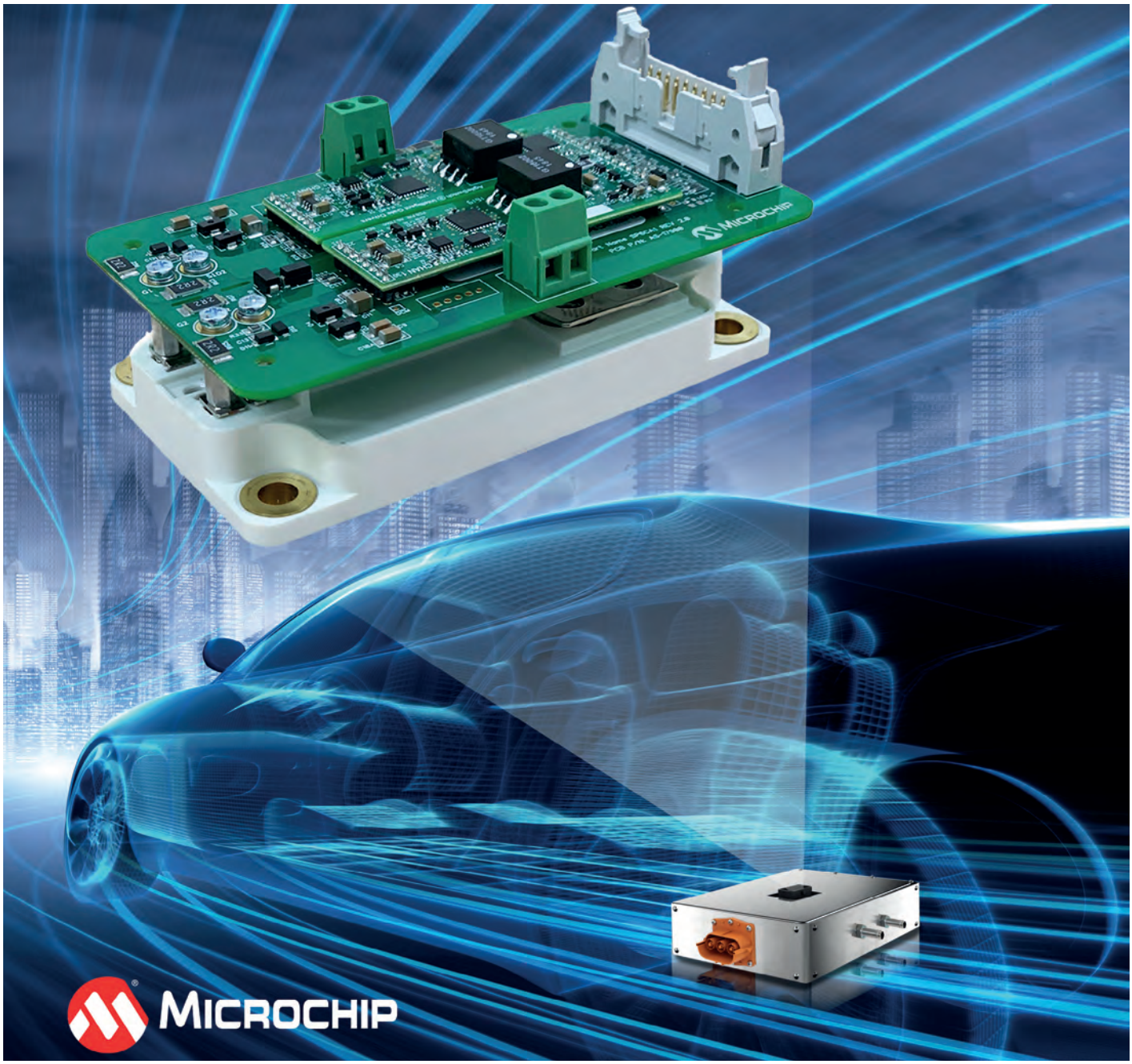
POWER SiC

Evaluating Three Key Pieces of a SiC Total System Solution



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FEATURE STORY

Evaluating Three Key Pieces of a SiC Total System Solution

Following a rapid expansion of SiC product options, the industry's next challenge is simplifying the design-in process for end users. Power system developers need holistic solutions that address not only typical design elements individually but which recognize the importance of their interactions. Put another way, aspirational SiC suppliers must not only demonstrate the performance and ruggedness of their SiC MOSFET technology, but must assist with design-in challenges by offering low-inductance power packaging and more sophisticated gate drivers to support, protect, and fine-tune system parameters. Careful consideration of these three key pieces is certain to simplify evaluation and design for those looking to capitalize on the disruptive system-level improvements made possible with SiC. More details on page 17.

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Covid-19 Slows Down WBG Growth Temporarily

The rapid evolution of the WBG compound semiconductor market between 2018 and 2019 has positioned both SiC and GaN as key materials within the power device market. There has been a remarkable shift of interest in SiC for automotive applications and in GaN for mainstream consumer applications. These applications will respectively drive the SiC and GaN power device market in the coming years, expects market researcher Yole Développement (Yole). But in the first half of 2020, the global COVID-19 outbreak has caused a significant slowdown of various end markets, especially the automotive and consumer segments, and thus has impacted the related power SiC and GaN market revenues.

Since the first commercialization of SiC diodes, the power SiC device market has been driven by power supply applications. Nevertheless, automotive is becoming the killer application, following SiC's adoption for Tesla's main inverters in 2018. Since then, different Tier 1-component makers, such as ZF and Bosch, and carmaker OEMs like BYD and Renault have recently made announcements on their adoption of SiC technology in some of their products. In the prospering SiC power market, the automotive segment is undoubtedly the foremost driver, and as such will hold more than 50% of total device market share in 2025. However, following the global Covid-19 outbreak, almost all automotive OEMs had to shut down and the supply chain faced significant disruption. In this context, Yole expect the power SiC market's growth to slow down to 7 % in 2020, with a significant impact in Q2-2020 and Q3-2020.

Arguably the most critical link in the power system chain, SiC MOSFETs must demonstrate robustness in several keys areas where they have traditionally been vulnerable. Like silicon MOSFETs, they too have been challenged with the problem of extrinsic defects such as impurities, charge states and other material defects near the oxide-semiconductor interface, which precipitate a variety of device instabilities and degradation mechanisms. Eliminating these risks requires that production-grade SiC MOSFETs demonstrate a stable threshold voltage, a reliable gate oxide, a robust intrinsic body diode, and ruggedness under avalanche conditions. Each attribute must be validated through qualification testing as parametric stability and lifetime can vary dramatically from one supplier to another. Careful consideration of these key pieces is certain to simplify evaluation and design for those looking to capitalize on the disruptive system-level improvements made possible with SiC (see our Cover Story).

In the power GaN landscape, Yole confirms a remarkable entry of several players into the high-volume consumer market, notably Power Integrations and Navitas. Many phone OEMs including Oppo, Vivo, Realme, and Meizu opted for GaN based inbox fast chargers, released with their flagships in the beginning of 2020. Samsung, Huawei, and Xiaomi chose GaN for accessory chargers. This represents a first milestone for power GaN devices in a high-volume consumer market. Driven by such consumer fast-charger applications, power GaN device market growth will be in the range of 170 % , with a market value of more than $700 million in 2025. However, due to the COVID-19 outbreak, smartphone production is estimated to drop 20 % in 2020. CUI recently launched GaN power adapters that are 32 % lighter than comparable Silicon-based power supplies, resulting in up to 250 % greater power density. The GaN adapters are also lighter and operate up to 96 % efficiency.

To date, a majority of the GaN power device development effort has been directed toward lateral devices, such as high-electron mobility transistors (HEMTs), fabricated in thin layers of GaN grown on other substrates. Some well-known issues of GaN HEMTs include current-collapse, dynamic on-resistance and inability to support avalanche breakdown. By fabricating power semiconductor devices grown on bulk GaN substrates, it is expected to realize the material limit potential of GaN, including true avalanche breakdown and create vertical architectures that do not suffer from thermal management issues with thin film surfaces and provide increased number of dice on a 4-inch GaN wafer. NexGen Power Systems Vertical GaN (see our Industry News) enables power supplies can meet the voltage needs of almost any application, from low voltage devices like electronics to high voltage products like electric cars and high speed trains. According to the company statements it typically lowers the cost of the power supply system by reducing passive components like inductors and capacitors. In data centres, Vertical GaN can enable a 20 – 25 % increase in compute density and a corresponding increase in revenue. Vertical GaN enables electric cars to drive up to 15 % farther while reducing cost by up to $1400. In solar system inverters it helps to generate more energy – up to a 50 % reduction in conversion losses! – at up to 20 % lower cost. Thus the company plans to enter full-scale production in 2020 at its $100 million fabrication facility in New York.

Thus the WBG journey continues with more innovative attempts in the years to come. We will keep our readers up-to-date!

Achim Scharf
PEE Editor

Strong Multi-Year Growth Ahead for Energy Storage

The global grid-connected energy storage market—which endured its first ever year-on-year decrease last year—is expected to rebound in 2020 despite ongoing impacts from COVID-19, according to IHS Markit.

The IHS Markit Energy Storage Service sees global installations growing by more than 5 GW in 2020 despite the disruption caused by the global pandemic. The growth highlights the increasing competitiveness of battery energy storage to provide critical capacity, especially in the United States, the world's largest market. "The fact that the energy storage industry is proving resilient and has resumed a growth trajectory during the pandemic and subsequent economic shock proves that the 2019 market retraction was an aberration. The 2020 rebound highlights the importance of the technology and the strength of the underlying market fundamentals.," says Julian Jansen, research manager at IHS Markit. The energy storage market has benefitted from a strong start to the year, with residential markets buoyant and large utility-scale pipelines being realized, as well as markets in the USA and China quickly rebounding from the drop 2019. Growth will continue beyond 2020. IHS Markit has increased its forecasts and now expects a fivefold rise in annual installations from 2019 to 2025, reaching 15 GW / 48 GWh. Annual grid-connected energy storage hardware revenues are projected to more than double (from $4.2 billion in 2020 to $9.5 billion in 2025), despite falling battery module prices, which are expected to fall 32 % during this timeframe.

Changing dynamics and strengthening fundamentals in several markets will drive most installations in the coming years. The United States will remain the largest market with growth driven by an ambitious round of state-level targets, a strong pipeline of solar-plus-storage projects capitalizing on the ITC (Investment Tax Credit) and increasing competitiveness of batteries as a source of firm capacity. China will see a resurgence in energy storage uptake as provinces begin to look to storage co-located with solar PV as a means of firming up increasingly high penetrations of renewable assets on the grid. China is forecast to install 6.5 GW through 2025 and be the second largest market throughout the forecast period. The outlook in Europe has strengthened as new opportunities develop in a wide range of countries. For example, a capacity auction in France will support 253 MW of energy storage by 2023.

Wholesale arbitrage is becoming a major driver for front-of-the-meter (battery) energy storage in Australia and the United Kingdom, signaling a turning point as merchant energy storage breaks into a new opportunity.

www.ihsmarkit.com

New Solar Energy Optics Technology Increases Output Power

Finnish technology company ICS has developed a unique technology platform and a film solution providing an up to 10 % increase in energy output for conventional solar modules – and even higher gains for more advanced applications.

The Solar Energy Optics (SEO) film solution is one of the key outcomes from comprehensive industrial research and development around light guide technology. "We have found a way to capture and very precisely redirect light beams," explains Kari Rinko, CTO at ICS. "Our SEO film technology is based on embedded cavity optics, which is not exposed to external influences or contamination and therefore lasts as long as the solar panel itself. The SEO film is as effective as if the optics would be mounted on the whole surface of the solar panel. We use an ultra-thin film produced in a cost-efficient roll-to-roll process. Thus, our technology is scalable and ready for seamless industrial adoption on a global scale enabling new sustainable energy goals for the whole photovoltaic industry."

The increased power output from the solar panels transforms the underlying economics for a solar park for the entire lifetime of the underlying panels. "The SEO film solution enhances the amount of light that is led into the solar cells," Rinko says. "The solar panels will get the immediate benefit, since more sunlight contributes to a more powerful solar panel." The SEO solution has been tested by independent third parties like the Fraunhofer ISE. Their tests concur with ICS' own experiments confirming a boost in the range of 5 – 10 % for conventional solar modules. One distinct feature is that the film layer is applied only on the surrounding rims, either onto the top or the bottom glass. Since it does not cover the entire surface of the solar cells, it offers economic benefits given the saving in material costs.

Rinko points out that the SEO technology focuses on controlling and redirecting more sunlight into the solar cells – not on the structure of the mono- and poly-crystalline Silicon cells themselves.

www.ics.fi

ICS – team members from left Jori Oravasaari, Kari Rinko and Jukka Backman

World's First Zero Carbon Lithium Extraction Project

EIT InnoEnergy, the European innovation engine for sustainable energy, has announced a partnership with Vulcan Energy Resources Limited (Vulcan), a start-up lithium exploration company, to produce the world's first completely carbon neutral lithium in Germany. The partnership is part of Europe's strategic industry initiative, the European Battery Alliance, aimed at building an independent, sustainable, and resilient battery industry in Europe.

The "Zero Carbon Lithium" project will be realized in the German part of the so-called Upper Rhine Rift, in the states of Baden-Wuertemberg and Rhineland-Palatinate. The region contains Europe's largest lithium resource and one of the largest worldwide. CEO of EIT InnoEnergy Germany, Christian Müller, said: "Batteries are a key technology of our time. Driven particularly by the demand of the e-mobility sector, Europe's share of global battery cell production is forecast to reach almost 15 % by 2024, overtaking the US and Asia excluding China. By using that momentum to accelerate the development of the European battery value chain, we are making our economy more resilient to future crises. The Carbon-neutral development of our own lithium deposits is a crucial building block for a sustainable and strong European battery industry and will bring us significantly closer to meeting our 2030 climate goals. By further investing in Vulcan, and the other lithium mining projects, Europe could cover most of its anticipated lithium demand from regional resources." Horst Kreuter, co-founder of Vulcan Energy Resources, said: "Our goal is to play an integral role in enabling a zero-carbon future by de-carbonizing the currently high carbon production footprint of lithium-ion batteries used in electric vehicles. We have therefore carried out a very thorough global search for the perfect location – and found it. Not only does the Upper Rhine region contain one of the largest lithium reservoirs globally, it is also within a few hours reach to many of the World's leading auto manufacturers, and many other industrial players, all of whom have a hugely growing demand for emission-free lithium."

Vulcan will pump hot lithium-rich brine up to the surface, then use the renewable heat to drive lithium extraction using its proprietary technique, with excess renewable energy as a saleable by-product that can be fed back into the grid. As a result, the carbon footprint of the production process could even be negative. The resulting lithium shall then be used in a number of ways, most notably in the production of lithium-ion batteries to meet the massive demand from the automotive and other sectors. Commercial operations are targeted to start to produce lithium hydroxide in time for the large increase in expected industry demand in Europe during the first half of the decade. Over time, production volumes are expected to massively increase.

www.eba250.com, www.innoenergy.com/office/germany/

New MPS EMC Testing Laboratories in Germany

Monolithic Power Systems (MPS) announced to open EMC testing facilities in Livonia/Michigan and Ettenheim/Germany in 2020/2021.

These new lab facilities will feature state-of-the-art EMC chambers for Radiated Emissions and Immunity measurements; shielded chambers for Conducted Emissions, Immunity Measurements, and EMC Engineering, and modern workplaces for pulse and electrical testing. MPS has been building on decades of experience in EMC-related topics to solve EMI problems during early design stages

with their customers. These new labs will allow anyone to gain access to fully compliant EMC testing equipment. "The further development of our EMC testing capabilities is a key milestone for MPS and a very important step to better serve automotive, consumer, and industrial customers in both the North

American and European markets. With these two new laboratories, anyone can benefit from our flexible lab scheduling, which will enable engineers to quickly and easily develop new products that fit their EMC requirements and help shorten design cycles and save costs," said Maurice Sciammas, Sr. VP, Sales & Marketing.

www.monolithicpower.com/en/support/emc-testing-laboratories.html

Formula-E Spurs Power Electronics Innovation

The Audi Sport ABT Schaeffler racing team, which has been supported by Würth Elektronik since the beginning of Formula E, has ended a season that was made more difficult by the pandemic. In the last races in Berlin from August 5 to 13, 2020, driver René Rast made a successful start to Formula E. Technology partner Würth Elektronik is already looking forward to the coming season. The new racing car FE07 is already being developed at full speed.

"From a technical point of view Formula E becomes more exciting with every season. More and more individual developments of the teams get into the racing cars. For the FE07, a separate powertrain is being developed for the first time - an exciting topic for us as a supplier of components for power electronics", says Oliver Opitz, Vice President of the Wireless Connectivity & Sensors Division and Technical Coordinator Formula E at Würth Elektronik eiSos. "Since the very first race we have been involved as technology partner. We see electric mobility as an important driver of innovation, whose sporty version we want to promote - as a kind of racing test laboratory, so to speak". The REDCUBE series of high-current connectors, which have been specially developed for the race track, has been in use in the car since Season 2. In addition, Würth Elektronik developed specific high-current high-voltage chokes and an innovative gate drive transformer for energy-saving, highly efficient electronics in electrical applications. The components are constantly tested under harsh conditions in the "Test Laboratory Race Track" in order to optimize them and adapt them to the requirements for a broad use in series applications in electric mobility. The company's product range includes EMC components, inductors, transformers, RF components, varistors, capacitors, resistors, quartz crystals, oscillators, power modules, Wireless Power Transfer, LEDs, sensors, connectors, power supply elements, switches, push-buttons, connection technology, fuse holders and solutions for wireless data transmission.

www.we-speed-up-the-future.com, www.we-online.com

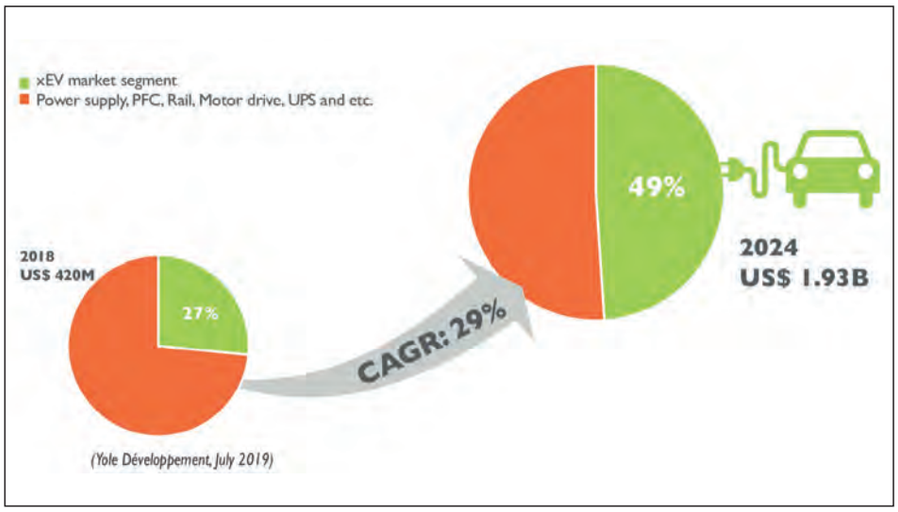
Formula-E driver René Rast in Würth Elektronik supported ABT Schaeffler racing car

SiC Drives Automotive Innovation

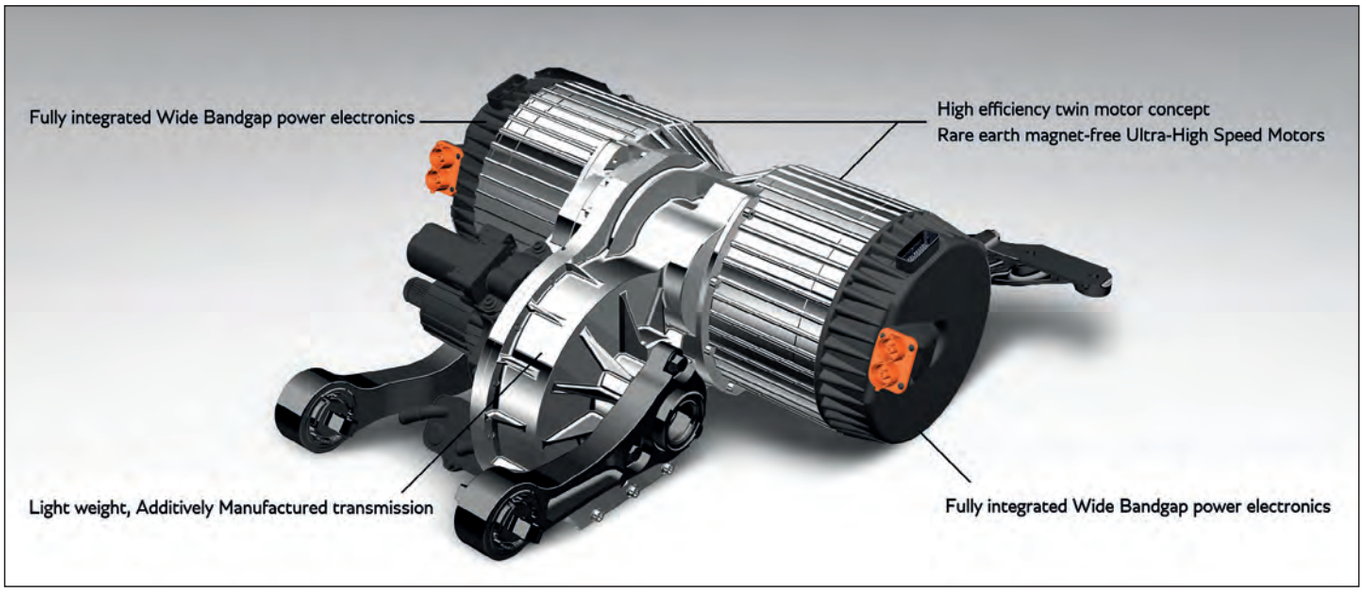
Market researcher Yole sees a prospering SiC power device market. The SiC power semiconductor market's value to approach $2 billion by 2024, with a compound annual growth rate (CAGR) of 29 %. The automotive market is undoubtedly the foremost driver, and as such will hold around 50 % of total device market share in 2024. Tesla adopted SiC for main inverters in 2018. Since then, different Tier 1-component makers, such as ZF and Bosch, and carmaker OEMs like BYD and Renault have made announcements on their adoption of SiC technology in some of their products. In the prospering SiC power market, the automotive segment is undoubtedly the foremost driver, and as such will hold more than 50% of total device market share in 2025.

In August 2020 UK-based Bentley Motors announced a three-year research study that promises to transform electric vehicle powertrains, utilizing a fully integrated, free from rare-earth magnet e-axle that supports electric vehicle architectures. This reinforces Bentley's ambition to lead sustainable luxury mobility and introduce the first fully electric Bentley by 2026. The study, titled OCTOPUS (Optimised Components, Test and simulatiOn, toolkits for Powertrains which integrate Ultra high-speed motor Solutions) follows an initial 18-month investigation that delivered a technological breakthrough in electric drive systems for high-performance vehicles. Building on the UK's leading electronics research, the resulting electric drive system exceeded the latest permanent magnet motor performance while simultaneously removing the need for both rare-earth magnets and copper windings, delivering a package both cost effective and recyclable at its end of life. OCTOPUS will take this leading-edge motor, SiC power electronics and packaging transmission design, adding next generation materials, manufacturing processes, simulation and test cycles to deliver a full e-axle powertrain with unique levels of integration by 2026. Commenting on the project, Stefan Fischer, Director of Powertrain Engineering at Bentley Motors, said: "We have made no secret of our ambition to lead the way in the delivery of sustainable luxury mobility. We have a clear roadmap to offer a hybrid option for every model by 2023, starting with the Bentayga Hybrid, and our next goal moves towards a fully electric Bentley by 2026. However today, there remains challenges and package constraints on the viability and flexibility of electric vehicle powertrains that are able to fully support EV architectures. With the industry, technologies and cars changing faster than ever before, research projects such as OCTOPUS are crucial to deliver innovative technologies and overcome challenges for the next generation of mobility solutions."

www.yole.fr, www.bentleymotors.com



SiC market evolution with a focus on automotive applications



Fully integrated e-axle for electric vehicles incorporating WBG (SiC) power electronics

High-Temperature SiC Module at High Power Cycling Operation

The PCIM 2020 Best Paper Award was given to So Tanaka from Japanese AIST (National Institute of Advanced Industrial Science and Technology) for a study demonstrating a SiC module operation after conducting a test of over 320,000 cycles at junction temperature of 200°C. This lifetime is one order of magnitude longer than a development target for automotive applications. This study focused on a thermal expansion coefficient matching layer made of an Fe-Ni "Invar" alloy with a CTE value close to that of SiC, a sintered copper joint and a copper wire for high temperature and high current durability improvement.

"In this paper we describe the lifetime extension by applying our CTE matching design concept to the top-layer structure above the chip to facilitate technology adoption in reliability-sensitive automobile and traction applications. Because the failures observed in previous studies were predominantly on the surface sides of the chips, chip surface packaging technologies to solve such technical hurdles are being developed and reported," So Tanaka explained in his presentation. The main attempts and results are shown here.

Fatigue-free module design

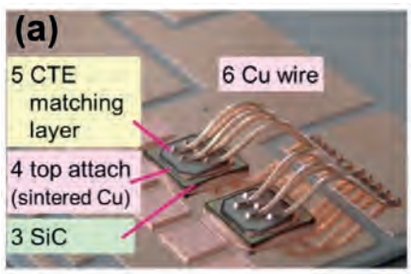
In this study, all component materials and their structures were precisely examined and designed to maintain their deformation within the elastic range at the operation temperature. The CTE differences relative to SiC were minimized to prevent mechanical fatigue failures during power-cycling tests (PCT) and temperature-cycling tests (TCT).

Metal alloy solders are widely used. Particularly because of its melting point, the processing temperature constrains the module assembly design. Therefore, for both the top and bottom sides of the chip, sintered Cu joints were adopted as the joint material. The sintered Cu allowed eliminating the constraint and drastically increased design flexibility. The chip surface packaging technologies described herein were realized using this joint material.

Cu wiring replaces the conventionally used aluminum (Al) wiring. This is because the Cu wire presents a smaller CTE (17 ppm/K) than Al (23 ppm/K) and is free of recrystallization and subsequent wire lift-off problems that are typically observed in Al-based wires after repeated thermal loading. Cu wiring is also essential for high current durability.

We considered the temperature swing conditions for 200°C operations from two aspects. One is based on an elevation from room temperature (25 °C). The other is during the power-cycling test. The swings for these two cases are 175 and 135 K, respectively. Second, from these, we estimated the CTE matching design criteria by taking into account the elastic limit of Cu, which is the major component material used in the module. The CTE differences of 8 and 10 ppm/K are obtained, respectively [Young's modulus of 129.8 GPa and yield strength of 180 MPa are used]. At dissimilar material junctions, such as SiC and Cu, the CTE differences are at least below the above mentioned values. This is a key design parameter for preventing mechanical fatigue failure.

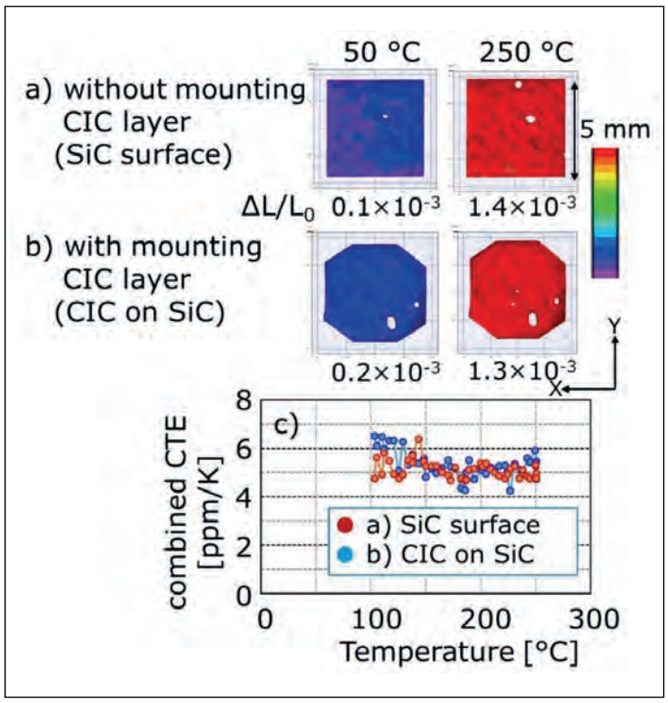
For the "bottom-layer" design, the component materials and structures of the lower layers below the SiC chip are considered. A metalized substrate and sintered Cu joint were optimized to minimize the CTE differences with SiC. For the substrate, the thickness ratio of the Si3N4 layer (bulk CTE = 2.7 ppm/K) to the Cu layers (17 ppm/K) is a key parameter. For the sintered Cu junction, its thickness was controlled to be more than one order of magnitude thinner than that of the substrate and the SiC chip. By virtue of this design, the CTE was dominated by the upper and lower layers, and it became equivalent to that of SiC by attaining the so-called "sandwich effect".



(c) Design Concept		conventional	bottom-layer design	top-layer design	
	Sample	A	B	C	D
6	wire	23 Al	23 Al	17 Cu	17 Cu
5	CTE matching layer	n/a	n/a	17 Cu	5 CIC (with Invar)
4	top attach			5 sintered Cu (*)	5 sintered Cu (*)
3	SiC chip	4 SiC	4 SiC	4 SiC	4 SiC
2	bottom attach	21 alloy solder	5 sintered Cu (*)	5 ditto	5 ditto
1	metalized substrate	9 conv. spec.	5 optimized thickness	5	5

The number in each cell is the CTE.
(*): sintered Cu with optimized thickness
n/a: not applicable
ditto: same as on the left

Summary of module structures. The component materials and their CTEs are listed. Sample A (conventional design with Al wire and alloy solder), B (bottom-layer design with sintered Cu and optimized metalized substrate), C (top-layer design with Cu layer) and D (top-layer design with CIC layer). Figures (a) and (b) are typical examples of our newly developed chip surface packaging technologies, including the SiC chip (#3), sintered Cu (#4), CTE matching layer (#5) and Cu wiring (#6). In each cell of (c), the width of the color bar corresponds to the CTE values (in units of ppm/K) and colors correspond to the states before (red) and after (blue) the developments



Surface deformation maps obtained (a) without and (b) with mounting the CIC layer, measured at 50°C and 250°C. The color legend in the upper images corresponds to the maximum deformation of 160 µm in the x-y directions. The combined CTEs measured up to 250°C are shown in (c)

For the "top-layer" design, the layers above the SiC chip are considered and realized by the application of our newly developed fatigue-free chip surface packaging technologies.

For this design consideration, the CTE matching between the SiC chip and the wiring material is one of the most crucial items. Consequently, one layer of an Fe-Ni alloy called "Invar," was installed between the chip and the wire. "Invar" exhibits uniquely low CTEs below a few ppm/K owing to its magnetic property. Invar is used in the form of a Cu/Invar/Cu trilayer structure, abbreviated as "CIC". The CTEs of this CIC structure can be adjusted by varying its thickness ratio. In this study, for matching its CTE to that of SiC, the CIC with a thickness ratio of a 1/3/1 was used and it has a CTE of 5 ppm/K.

Experimental results

Test samples used in this study are designed for 150 A / 1.2 kV half-bridge modules with a compact footprint of 50 mm × 62 mm. For the power- and temperature-cycling tests, the two SiC Schottky barrier diode chips (5 mm × 5 mm) were mounted in parallel. The conventional design sample assembled using a tin-based solder (Sample A) and the bottom-layer design sample (Sample B) were tested as references. Both top- and bottom-layer design were applied to Samples C and D with a 0.1-mm-thick CTE matching layer and 0.4-mm-diameter Cu wire. For Sample C, a Cu layer was used as the CTE matching layer for comparison.

To verify that the structures are fabricated "as designed," the surface deformations and their CTEs were measured at each module assembling process. In particular, before and after mounting the CTE matching layer on the SiC chip, these properties were evaluated by using the digital image correlation method, which is one of the powerful tools for analyzing the thermo-mechanical deformation of such electronic components.

The properties were measured during the heating and cooling sequences between 25 and 250°C. Approximately 20,000 locations on the chip surface were assigned and the displacements of each location were monitored relative to their initial locations. It should be noted that the obtained CTE values are the so-called "combined CTEs" that comprise the CTEs from the surface layer to the underlying overall structures.

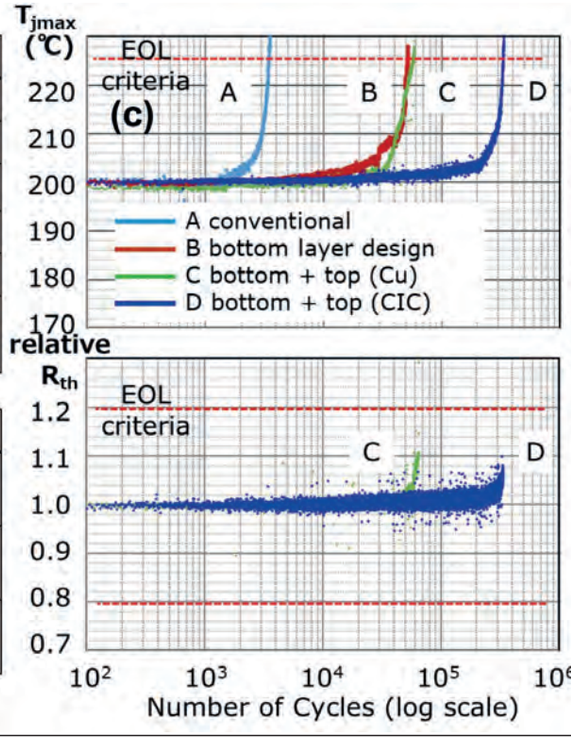
Prior to the power-cycling test the electrical and thermal resistances were evaluated based on the comparison of three structures: Sample B (without a CTE matching layer) and Samples C and D (with CTE matching layers). To eliminate the contribution of the wires, two separate pairs of wires were attached to the top and bottom of the chips

(a) PCT conditions

ton / toff (s)	1 / 13
Tjmin (°C)	65
Tjmax (°C)	200
ΔTj (°C)	135
I load (A)	125
EOL (end of life) criteria	ΔTj+20% Rth+20%

(b) TCT conditions

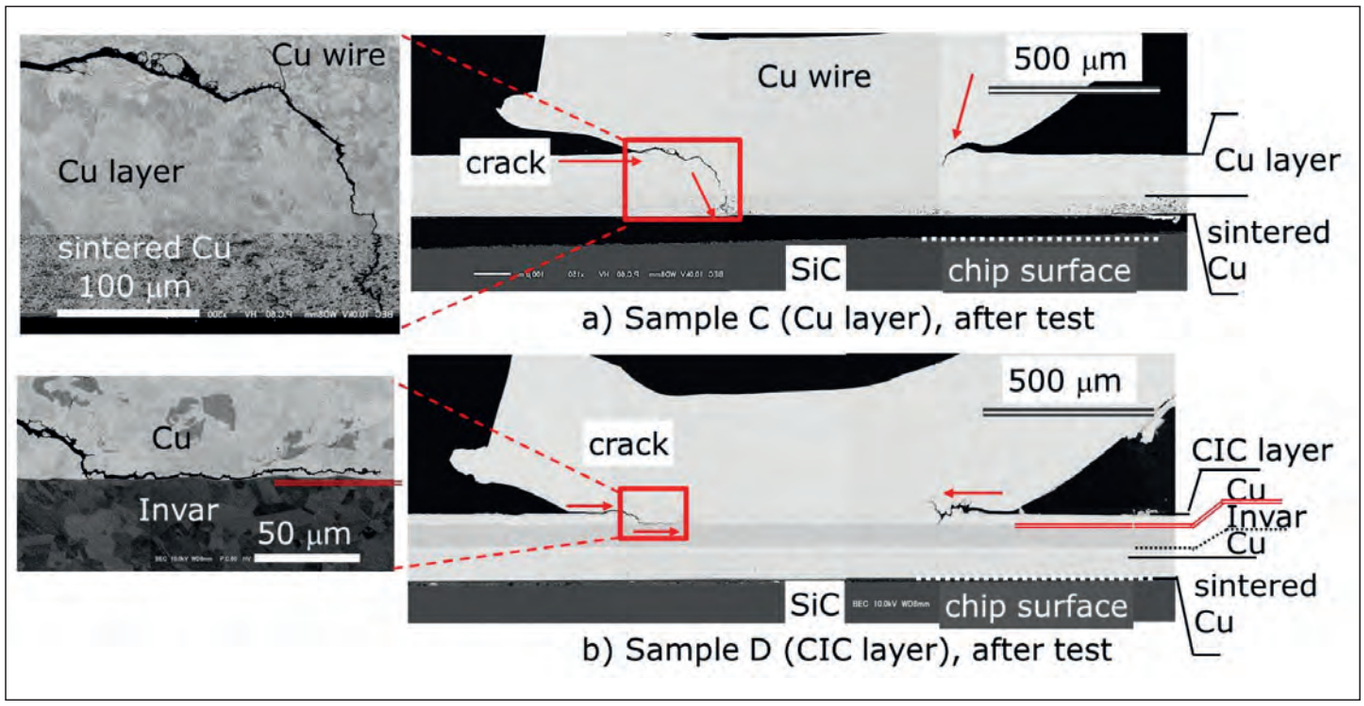
ΔT (°C) (low / high)	240 -40 / 200
temperature hold time (min)	30
EOL (end of life) criteria	Ron+10% Rth+10%



(d) PCT lifetimes (cycles)

A	3,200
B	52,000
C	58,000 (DUTs = 4)
D	334,000 (DUTs = 5)

Power- (PCT) and temperature-cycling test (TCT) conditions and criteria are listed in (a) and (b). The T_{jmax} and R_{th} trend data are shown in (c). The power-cycling lifetimes are summarized in (d). The PCT conditions are based on the IEC60749 standar



Longitudinal cross-sectional SEM images of Sample C (a) and Sample D (b). The arrows specify the positions where cracks are observed. The magnified images on the left show the crack propagation path in the Cu (a) and CIC (b) layers, respectively. The upper interface of the CIC layer (Cu/Invar) is marked by double solid lines in (b). The chip surfaces are marked by white dash lines. The images of (a) are flipped horizontally to maintain a consistent visualization

to construct a four-point probe configuration.

Electrical series resistances were defined by the on-state resistance measured at the forward bias condition. The resistances of Samples C and D are equivalent to that of Sample B, which corresponds well with our calculation results obtained using bulk values. The contribution of the CTE matching layer is estimated to be more than three orders of magnitude smaller than that of the R_{on} value of the diode device.

In contrast, the transient thermal resistance was measured and was found to be reduced by over 10 % when the CTE matching layers were applied (for Samples C and D), and the difference between those for Samples C and D was negligibly small. This is attributed to the fact that the junction area was enlarged at the surface sides owing to the favorable effect of the CTE matching layer applied to the SiC chip. The observed improvements in both electrical and thermal properties are expected to have an impact on the power-cycling capability.

Temperature-cycling tests were performed and completed when the bottom-layer design (Sample B). On-state resistance (R_{on}) and thermal resistance (R_{th}) were monitored during the test. After 1,000 cycles, these properties did not reach the EOL criteria, demonstrating that electrical and thermal paths of the components from the chip to the baseplate were in good condition.

Failure mode analysis

To specify the failure modes of Samples C and D, cross-sectional observations through a scanning electron microscope (SEM) were performed before and after the PCT. The analysis was conducted by focusing on the junctions at the top and bottom sides of the chips and on those close to the Cu wire.

Although no wire lift-offs were observed in both cases, cracks were detected at the toe (left) and heel (right) of the wire, marked by arrows in the figures. It was confirmed that such cracks were not observed before the test. From the detailed observations, clear differences of the crack propagation path are confirmed in two samples. In Sample C (Cu layer), the cracks pass through the two layers containing the Cu matching layer and sintered Cu, and they reach the chip surface. On the other hand, in Sample D (CIC layer), the cracks stop at the upper Cu/Invar interface and propagate horizontally, as marked by the double solid line. Note that these cracks stopped at this Cu/Invar interface with a limited length of approximately 100–200 µm.

These two samples exhibit similar delamination failure that occurs at the Al metallization layer at the chip surface, as indicated by the white dashed line. In Sample C, the entire Cu layer was lifted off from the chip surface. In Sample D, the CIC layer was not peeled off. However, degradation of the Al layer was clearly proceeded.

Typically, creeping of metals begins at a temperature approximately 0.4 times the melting point. Because Al has the lowest creeping initiation temperature among the major module component materials, it becomes the starting point for the delamination failure with high probabilities [Creep initiation temperature (0.4×T m): Al (100 °C), Cu (270 °C) and Ni (418 °C)].

On the contrary, no degradation was observed in the chip / metalized substrate / baseplate structure.

Conclusions

SiC power modules operational at the temperature of 200°C were successfully developed with fatigue-free design concepts. At a T_{jmax} of 200°C and a ΔT j of 135 K, the power-cycling lifetime was observed to be 334,000 cycles. Such a significant improvement resulted from the application of a

CTE matching CIC layer, sintered Cu joint, and Cu wiring on the surface of the chips. In particular, the CIC layer whose CTE value was designed to match that of the SiC chip had a synergetic effect in which it suppressed fatigue failures and formed strong bonds with the Cu wire. The reported results evidentially showed that the challenges associated with the 200°C operation of the SiC devices can be overcome. The proposed design concepts and newly developed fatigue-free chip surface packaging technologies are expected to provide a pathway to developed SiC power devices to the next stage; thus, the electronics and cooling systems for automotive and traction applications can be effectively redesigned and refined.

Literature

"SiC module operational at 200 °C with high power-cycling capability using fatigue-free chip surface packaging technologies", PCIM Europe digital days 2020, 7 – 8 July 2020 proceedings, pages 30 - 37

www.aist.go.jp

GaN Goes Vertical

Silicon power technology has enabled the explosion in consumer and industrial electronics for the past decade, but that technology has now stalled. Power conversion systems are a critical component of all electronics. The transformation of power systems from heavy, bulky and inefficient analog devices to compact, energy saving switching devices helped drive the growth of sophisticated electronic systems. Silicon power transistors were at the heart of those new generation systems. Vertical GaN™ in contrast creates three times the system power density of Silicon, making it ideal for applications where there are size and space constraints. At PCIM Europe digital days first results have been demonstrated.

NexGen Power Systems Vertical GaN™ enables power supplies can meet the voltage needs of almost any application, from low voltage devices like electronics to high voltage products like electric cars and high speed trains. According to the company statements it typically lowers the cost of the power supply system by reducing passive components like inductors and capacitors. In data centers, Vertical GaN™ can enable a 20 – 25 % increase in compute density and a corresponding increase in revenue. Vertical GaN enables electric cars to drive up to 15 % farther while reducing cost by up to $1400. In solar system inverters it helps to generate more energy – up to a 50 % reduction in conversion losses! – at up to 20 % lower cost. Thus the company plans to enter full-scale production in 2020 at its $100 million fabrication facility in New York.

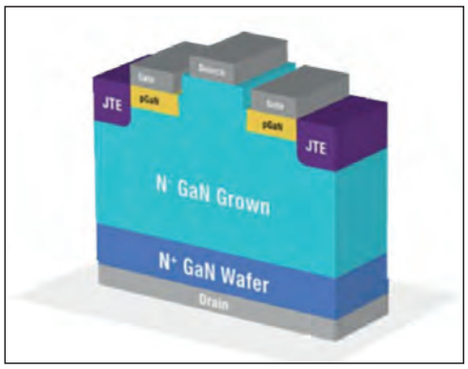
To date, a majority of the GaN power device development effort has been directed toward lateral devices, such as high-electron mobility transistors (HEMTs), fabricated in thin layers of GaN grown on other substrates. Some well-known issues of GaN HEMTs include current-collapse, dynamic on-resistance and inability to support avalanche breakdown. By fabricating power semiconductor devices grown on bulk GaN substrates, it is expected to realize the material limit potential of GaN, including true avalanche breakdown and create vertical architectures that do not suffer from thermal management issues with thin film surfaces and provide increased number of dice on a 4-inch GaN wafer.

Growth and fabrication

The growth of GaN on mismatched substrates such as Sapphire, Silicon and Silicon Carbide creates difficulties for vertical device structures and results in poor material quality with high defect densities. High performance vertical GaN transistors have been achieved through homoepitaxial growth on GaN substrates and through the development of processing techniques applicable to vertical p-n devices and their edge termination.

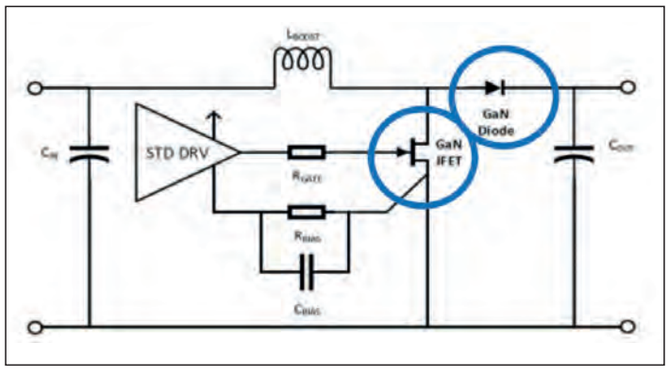
As the schematic cross section of the vertical GaN transistor illustrates the GaN layers comprising the p-type blocking layers and the vertical drift region were epitaxially grown by metal-organic chemical vapor deposition (MOCVD) on 4-inch bulk GaN substrates.

Imaging plan-view cathode-luminescence (CL) reveals that threading dislocation density in films grown over bulk GaN substrates is 10^{4} cm^{-2}, at least 4 orders of magnitude lower than for GaN films grown on Si or SiC substrates. The maximum breakdown is determined by the design of the drift layer doping and thickness. Wide trenches are etched in the channel region using Cl-based chemistry in an inductively coupled plasma (ICP) process. The p-region is realized by in-situ growth of Mg-doped p+ GaN epitaxial layer in



Schematic cross-section of the vertical GaN transistor on a GaN wafer

NexGen's $100 million GaN fabrication facility in New York



Application example: 100 – 400 V boost switcher at 1 MHz

the trenches on top of the n- type GaN epitaxial drift region. The n+ channel doping, its thickness and p+ GaN doping, is selected to realize a positive threshold voltage.

Source contacts are routed to create the source terminal and the gate contacts are routed to realize the gate terminal. The wafer is thinned, and metal contact created on the back side of the wafer to realize the drain terminal of the JFET.

Vertical GaN JFET operation

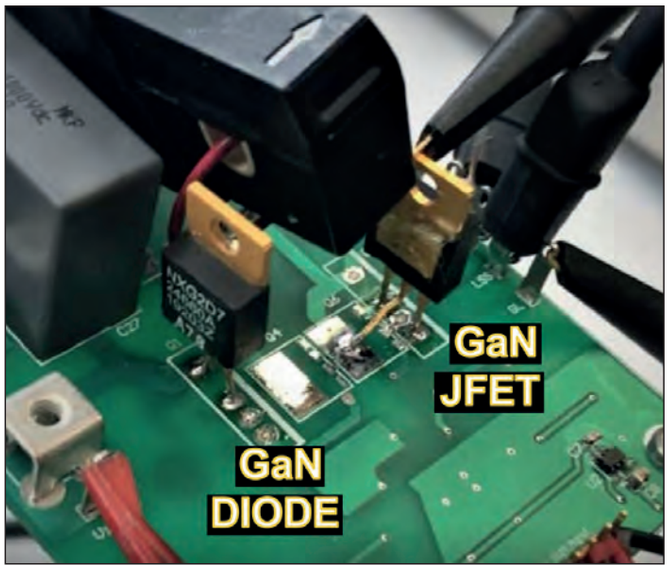
The NexGen Vertical GaN FET is a junction field effect transistor (JFET) in which the vertical n-GaN channel is sandwiched between two p-n junctions. The device's cross-section bears some resemblance with FinFETs as used in Silicon logic devices.

The bias difference between gate and source (V_{GS}) affects the extension of the depletion regions of the two p-n junctions into the n-GaN channel and controls the current between drain and source. When V_{GS} is below the threshold voltage (V_t), the JFET channel is closed. When V_{GS} is larger than V_t, the JFET channel opens and current can flow between source and drain. Normally-ON (Depletion Mode) and Normally-OFF (Enhancement Mode) devices can be produced by modifying device design parameters.

The magnitude of effective gate voltage above Vt ($V_{gt} = V_{GS} - V_t$) affects the depleted n-type charge in the channel and thus the $R_{DS(on)}$ of the JFET. At higher V_{GS}, the larger V_{gt} causes a less depleted n-type charge and hence a lower $R_{DS(on)}$. In this way, the drain current is controlled by the gate source voltage and shows the familiar FET I_{DS}/V_{DS} relationship. $R_{DS(on)}$ is also dependent on V_{GS} and increases when the voltage drop caused by I_{DS} along the source drain path is large enough to pinch the channel.

The Vertical GaN transistor construction, being essentially a majority carrier JFET device, does not create a parasitic body diode between drain and source as known from Si-SJ and SiC power MOSFET devices. Therefore Vertical GaN

Scope image of V_{GS}, inductor current, V_{DS}, F_{sw} = 900 kHz, V_{in} =150 V, V_{out} = 400 V and L=128 µH



NexGen GaN eJFET and NexGen GaN PN diode on PCB boost circuit

does not suffer switching losses caused by minority carrier/reverse recovery charge removal. In addition, the device structure allows current flowing in reverse direction in case of a reversal of the drain-source voltage. In this way the JFET effectively assumes the function of a freewheeling body diode without the disadvantages of additional reverse recovery switching losses.

The gate-source voltage necessary to reduce the depletion region and open the channel in enhancement mode devices will slightly forward bias the gate-source diode. This causes a small static gate current. The device is designed so that in normal operation only a few milliamperes of static gate current is flowing.

It should be emphasized that the gate diode current itself does not enhance or otherwise control the channel current and therefore should be regarded as symptomatic of the "parasitic" gate-source diode but not necessary for the transistor device operation.

It is possible to overdrive the gate for a short amount of time in order to draw - e.g. during switching transitions - much more drain current than in normal operation. The gate source diode is sufficiently robust to accommodate the larger peak gate currents.

The small device area of NexGen's 1200V Vertical GaN technology leads to much smaller device capacitances compared to 1200 V SiC devices at similar $R_{DS(on)}$ and drain currents. Vertical GaN-based devices are also smaller than comparable lateral GaN devices that have a much lower BV specification of 600 V.

C_{oss} (and consequently Q_{oss} and E_{oss}) is very small, greatly reducing turn-on losses. This is key to the high efficiency and high switching frequency operation of applications enabled by Vertical GaN JFETs. Also the gate-source to gate-drain capacitance ratio is engineered to eliminate half-bridge hard-switching device return-on, even in extreme dv/dt situations.

Application example

A ZVS boost circuit switching at 1MHz with a vertical GaN PN diode and a vertical GaN JFET has been shown as an application example. The JFET is driven by a standard Silicon MOSFET driver. Efficiency is >96 % at 1 MHz. The scope image demonstrates soft switching behavior of the Vertical GaN JFET and Gan PN diode in a 150 V to 400 V boost.

Literature

"Not All GaN Transistors are Built Equal: The Benefits of Vertical GaN-on-GaN"; Dinesh Ramanathan, Charles Coles, Wolfgang Meier, NexGen Power Systems, USA; PCIM Europe digital days 2020 proceedings, pages 880 – 883

https://nexgenpowersystems.com/

Power Adapters Slim Down with GaN

Easy portability and a slim or compact outline are great design goals for external power adapters. In practice, success is always limited by the need for thermal management (large heatsinks) to ensure reliability and relatively large filter components to stabilize and smooth the DC power at the output. Advanced GaN power-semiconductor technology reduce size, weight, and increase energy-efficiency advantages. **Ron Stull, Power Systems Engineer, CUI Inc., Tualatin, USA**

With the arrival of new power transistors based on GaN technology, unlike traditional Silicon-based devices, power adapters are set to become considerably smaller, slimmer, lighter, and generally less intrusive. This is great news for a huge variety of products ranging from laptops to gym equipment such as treadmills that are often positioned in rows comprising several units side by side. Smaller adapters can offer advantages such as reduced clutter, a more pleasant appearance, and easier portability.

What's special about GaN?

GaN (gallium nitride) is one of the emerging groups of so-called wide bandgap (WBG) semiconductors that also includes Silicon Carbide (SiC). After long development, enhancement-mode (normally turned off) GaN transistors that are ready to deploy in commercial power supplies are now available. Compared to Silicon devices, GaN transistors offer a more favorable combination of conduction losses in relation to device voltage rating, fast switching capability with low energy losses, high thermal conductivity, and high-temperature operation, at a price that is cost-effective for consumer and industrial applications.

At the forefront of advanced power supply development, CUI recently launched GaN power adapters that are 32 % lighter than comparable Silicon-based power supplies (Figure 1), resulting in up to 250 % greater power density. The GaN adapters are also lighter and operate up to 96 % efficiency.

The key to these advances lies in GaN's superior efficiency at high operating frequencies, which allows designers to specify a smaller transformer and smaller filtering components such as inductors and capacitors. Bulky heatsinks can also be avoided. These are typically the largest components in the adapter, so trimming or eliminating these can make a significant difference to the overall size and allow more freedom to craft the outline to achieve a desired look.

GaN boost to power supply performance

In any switched-mode power supply, transistors are either turning on, turned on, turning off, or turned off. In each state some energy is lost. An important goal for the power supply designer is to minimize the overall effect of these losses. The chosen transistor parameters, the converter topology, and the switching frequency are major factors that influence the result. As far as transistor selection can help, the parameter $R_{DS(ON)}$ (resistance from drain to source) heavily influences the losses when the device is turned on. Switching performance, on the other hand, is governed by the charge (Q_g) due to the capacitance of the transistor's gate region. The product of $R_{DS(ON)}$ and Q_g is an important figure of merit (FOM) for power transistors.

Transistor designers seek to create devices with low FOM that are attractive for use in switching power supply applications. However, optimizing the device for low $R_{DS(ON)}$ tends to come at the expense of increased Q_g, and vice versa. It's a balancing act that means the transistors with the best FOM, i.e low $R_{DS(ON)}$ and low Q_g, tend to be expensive. Moreover, as far as plain old Silicon transistors are concerned, the technology is nearing its theoretical limit. Engineering the FOM down to a lower number is increasingly difficult and costly while at the same time the

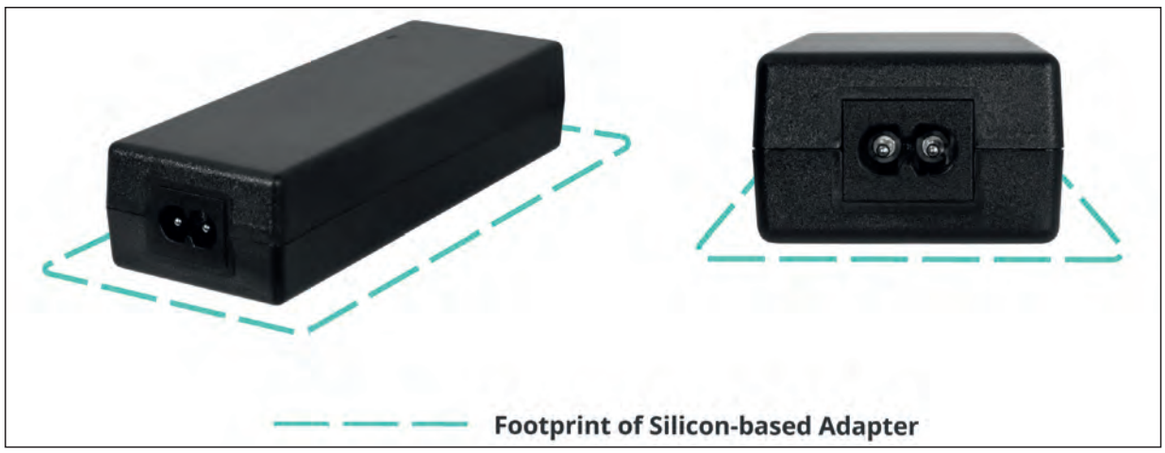


Figure 1: New power adapters built with GaN transistors are 33 % smaller than their predecessors

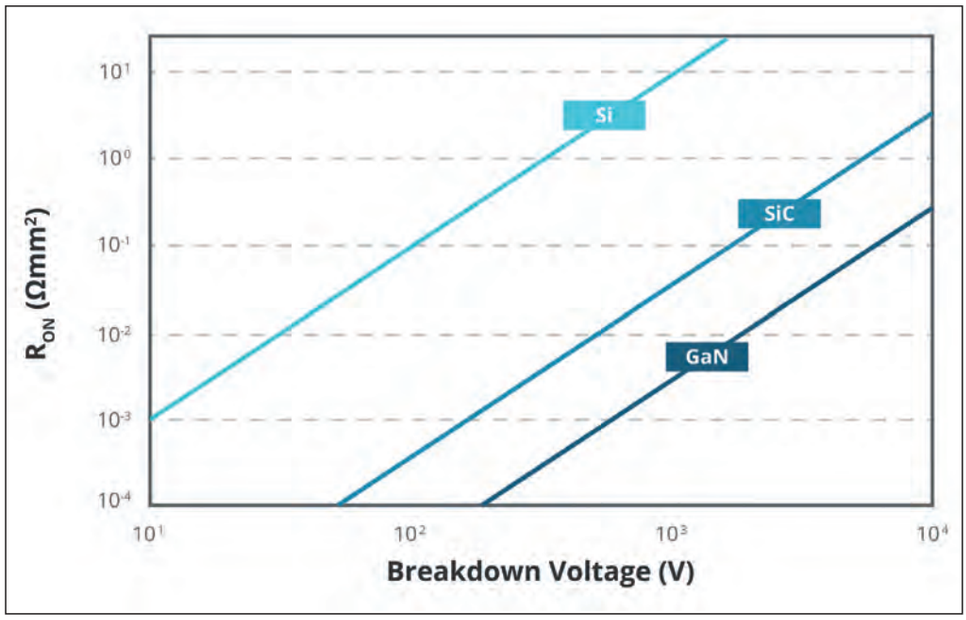


Figure 2: GaN transistors have much lower RDS(ON) in relation to voltage rating (breakdown voltage) than Silicon or SiC devices

potential improvements that can be achieved are diminishing.

GaN technology now introduces a "new deal" for device designers and – by extension – power-supply designers, too. GaN technology allows extremely low $R_{DS(ON)}$ in relation to the breakdown voltage of the device. For typical line-powered applications, GaN offers by far the most favorable combination of device voltage rating and $R_{DS(ON)}$ compared to Silicon and the other wide-bandgap technology in use today, Silicon Carbide (SiC), as Figure 2 illustrates. The switching losses of GaN devices are also naturally lower than those of Silicon devices.

By taking advantage of these characteristics of GaN transistors, power supply designers can save conduction losses thanks to the low transistor $R_{DS(ON)}$ while also using higher switching frequencies without incurring excessive switching losses.

At higher switching frequencies, shorter cycles allow filters comprising lower values of capacitance and inductance to store enough energy for effective smoothing of the output. Hence these components can be physically smaller. The transformer size can also be reduced. Moreover, because GaN has better thermal conductivity than Silicon, and devices can withstand higher operating temperature, the rating and hence the physical size of any heatsinks can also be reduced. In practice, a heatsink-free design is often possible.

Whereas conventional Silicon-based transistors are typically switched at frequencies in the 65-100 kHz range, GaN-based designs can operate at about 600 kHz at light loads, reducing to about 300 kHz for optimum efficiency up to full load.

GaN transistor behavior when turned off is also worth examining. In a conventional Silicon transistor, a parasitic diode in parallel with the main drain-source channel, called the body diode conducts a reverse freewheeling current when the transistor is reverse biased while turned off. The GaN transistor has no such parasitic diode, although freewheel current is allowed to pass through the main channel. The absence of body diode reverse-recovery charge lowers switching losses. Also, there is no diode turn-on noise hence electromagnetic emissions can be lower. In a half-bridge power stage, the fast switching capability allows the dead-time, during which both transistors are turned off, to be extremely short thereby minimizing power dissipation due to freewheel currents.

Meeting efficiency regulations

The efficiency of power adapters for commercial products is, of course, heavily controlled by ecodesign regulations that are in place in major markets worldwide. Today's adapters – whether Silicon or GaN based – must meet strict specifications on maximum power dissipated in standby mode and average operating efficiency, which is measured at various loadings from below 50 % to full load. Depending on the type of adapter and its power rating, the current US Level VI regulations call for maximum allowed standby power as low as 210mW and imposes minimum average efficiency requirements based on measurements at 25 %, 50 %, 75 %, and 100 % of full load.

The conventional Silicon-based units in CUI's portfolio satisfy the toughest ecodesign regulations currently in force worldwide. GaN-based products can surpass these requirements and hence will become increasingly in demand to meet new and tighter specifications in the future.

Into production

In the current timeframe, CUI's GaN strategy focuses on maximizing size and weight savings at comparable or better efficiency than Silicon-based products. The first GaN power adapters to enter production, the SDI200G-U with three-prong (C14) inlet and SDI200G-UD with two-prong (C8) inlet, achieve 210 mW no-load power consumption and efficiency of up to 96 %. Both units meet the current US DoE Level VI and EU Ecodesign specifications for average efficiency and no-load power as well as the more stringent, but voluntary, EU CoC Tier 2 directive.

Measuring 5.91 x 2.13 x 1.3 in. (150 x 54 x 33 mm), the new models have power density of 11.4 W/in³, which compares with 5.3 W/in³ for similar conventional silicon power adapters. At 560 g, compared to 820 g, they are also 32 % lighter.

Outlook for the future

CUI's SDI200G models are the first generation of power supplies to take advantage of the exciting new GaN technology and further models are planned. GaN transistors will also allow engineers to unleash the benefits of high-efficiency circuit topologies such as active-clamp flyback and bridgeless totem-pole power-factor correction in future designs. Moreover, as GaN is in its infancy, the long-term outlook promises significant improvements in device performance that will enable future generations of power products to offer even greater efficiency, reliability, and space savings.

Evaluating Three Key Pieces of a SiC Total System Solution

Following a rapid expansion of SiC product options, the industry's next challenge is simplifying the design-in process for end users. Power system developers need holistic solutions that address not only typical design elements individually but which recognize the importance of their interactions.

Kevin Speer, Microchip Technology, Phoenix, USA

SiC suppliers must not only demonstrate the performance and ruggedness of their SiC MOSFET technology, but must assist with design-in challenges by offering low-inductance power packaging and more sophisticated gate drivers to support, protect, and fine-tune system parameters. Careful consideration of these three key pieces is certain to simplify evaluation and design for those looking to capitalize on the disruptive system-level improvements made possible with SiC.

Robust and rugged SiC MOSFET

Arguably the most critical link in the power system chain, SiC MOSFETs must demonstrate robustness in several keys areas where they have traditionally been vulnerable. Like silicon MOSFETs, they too have been challenged with the problem of extrinsic defects such as impurities, charge states and other material defects near the oxide-semiconductor interface, which precipitate a variety of device instabilities and degradation mechanisms. Eliminating these risks requires that production-grade SiC MOSFETs demonstrate a stable threshold voltage, a reliable gate oxide, a robust intrinsic body diode, and ruggedness under avalanche conditions. Each attribute must be validated through qualification testing as parametric stability and lifetime can vary dramatically from one supplier to another.

To test the threshold voltage (V_{th}) stability of a SiC MOSFET, it is common practice to apply positive (p-HTGB) and negative (n-HTGB) high-temperature gate bias stresses to a statistically significant number of devices and simply compare the pre- and post-stress V_{th} of the population. As an example, p- and n-HTGB have been performed on independent sets of sixty-four 1200 V SiC MOSFETs for 1,000 hours. The average change observed in V_{th} was +59.6 mV following p-HTGB and -22.8 mV following n-HTGB. At this stability level, developers have a predictable threshold voltage around which they can make tighter, longer-term design choices.

High-reliability gate oxides are critical for all applications, especially those requiring long service lifetimes. To determine the

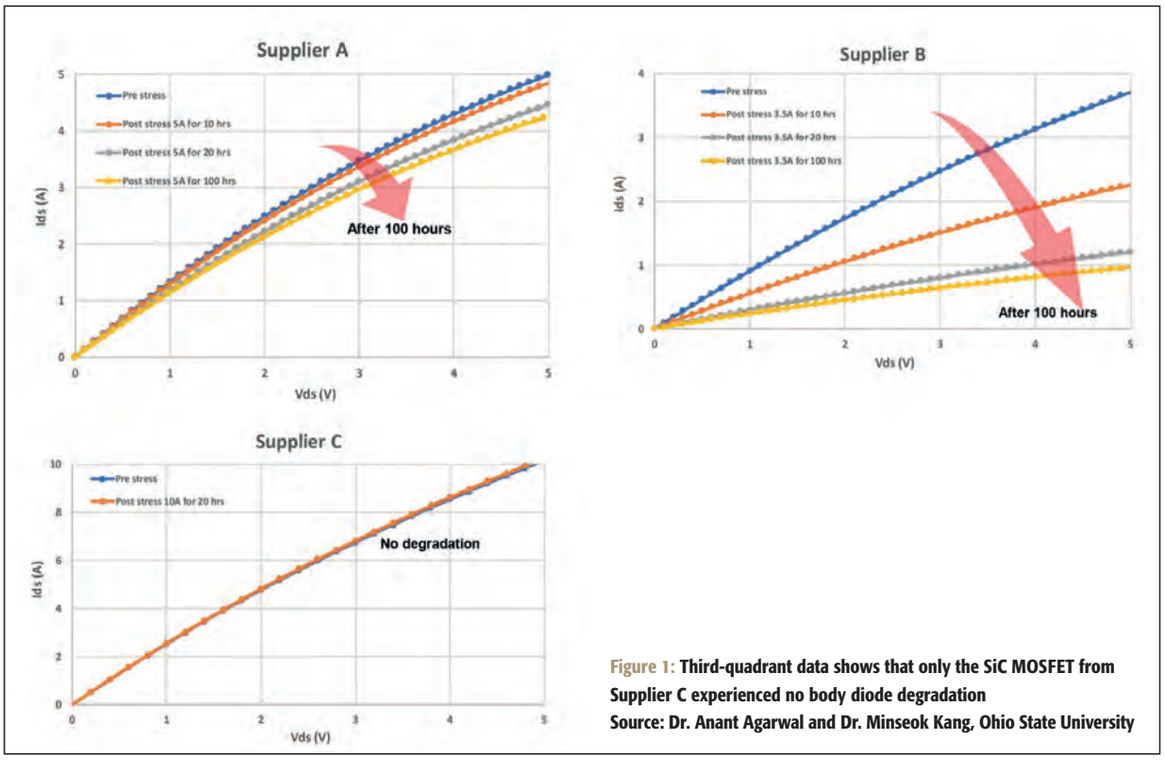


Figure 1: Third-quadrant data shows that only the SiC MOSFET from Supplier C experienced no body diode degradation
Source: Dr. Anant Agarwal and Dr. Minseok Kang, Ohio State University

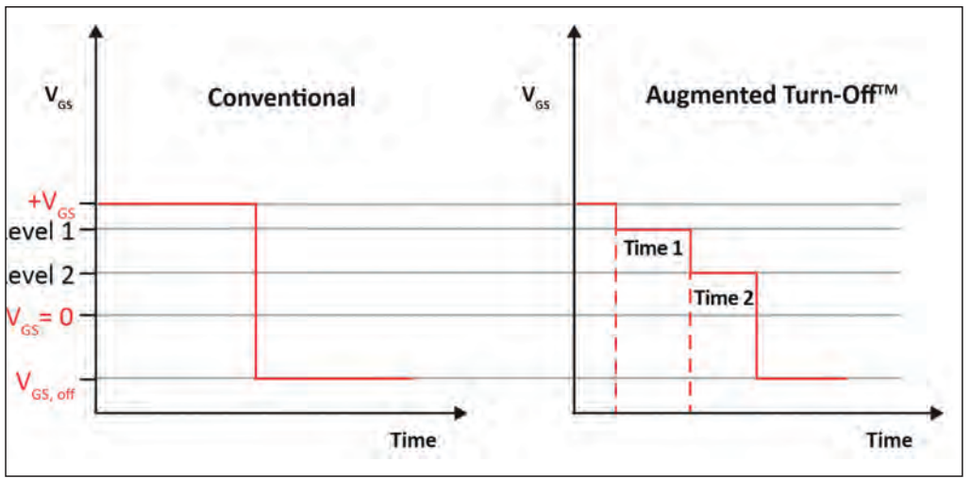


Figure 2: Digital gate drivers that use an augmented switching approach make a simple, straightforward task of identifying the optimal design points and quantifying their value to stakeholders

reliability of the subject SiC MOSFET's gate oxide, charge-to-breakdown (Q_{BD}) measurements were made on three populations of 1200 V SiC MOSFETs. All observed failures were intrinsic, indicating a high level of process maturity. Failure in Time (FIT) and Mean Time to Failure (MTTF) rates were calculated using a broader population of 192 devices. For p-HTGB, these values were found to be 20 and 5,618 years; for n-HTGB, the FIT was 93 with an MTTF of 1,233 years. End users should find encouragement that these results are consistent with time-dependent dielectric breakdown (TDDB) reports from multiple vendors.

The phenomenon of bipolar degradation in SiC p-n junctions has been heavily studied. Should this occur in the body diode of a SiC MOSFET, increases will be seen in both on-state resistance and the voltage drop across the diode during current commutation (revealed by a detrimental drift in third-quadrant output characteristics). Thankfully SiC MOSFET materials have matured, and the density of preexisting crystal defects has decreased in production-grade materials. Even so, each vendor's SiC MOSFETs must be evaluated. Ohio State University recently contrasted body diode degradation following 100 hours of stress at full-rated current (V_{GS} = -5 V) in 1200 V SiC MOSFETs from multiple vendors, revealing substantial disparities in post-stress on-state resistance. Only Supplier C showed no degradation (Figure 1). Complementary third-quadrant data on the same devices corroborated the presence (or absence, for Supplier C) of body diode degradation.

Another important parameter to assess is avalanche ruggedness, which is done with unclamped inductive switching (UIS). The MOSFET is fed a power surge while in its OFF state, which forces all current to avalanche in the die's periphery since the MOS channel is not enhanced. This differs from a short-circuit withstand test, in which the MOSFET is in an ON state and the current more uniformly distributes across the device's entire active area. To closely emulate real-life field conditions, SiC MOSFETs are subjected to repetitive UIS (R-UIS) pulses; parametric stability and oxide integrity are compared before and after 100,000 repetitive pulses at two-thirds rated current (per MIL-STD-750). V_{BR}, V_{th} and the body diode's V_F are unaffected by R-UIS, indicating excellent avalanche ruggedness.

Low-inductance power packaging

With confidence established in the SiC MOSFET, the next instrumental piece of a SiC total system solution is an optimized power package. An effective multi-chip module package should enable designers to leverage SiC's advantages rather than inhibit them.

There are numerous requirements to consider. Because the SiC MOSFET die is comparatively small, many of them must be paralleled to achieve a low on-state resistance. As well, the paralleled MOSFET die must switch with the same timing and uniform current sharing, which means ensuring both symmetry and low inductance through die interconnection schemes.

An example is Microchip's SP6LI package that inserts only 2.9 nH of stray inductance into the power loop, compared to 20+ nH of parasitic inductance in standard module packages. Power loop inductance is reduced by arranging DC link connections in strip line-configured bus bars . Substrate connections are symmetrically distributed and as close as possible to the semiconductor die. With respect to the gate-source loop, independent series gate resistor slots are used for each of the twelve available die spaces in the high- and low-side switch positions to optimize timing and current sharing. The independent gate resistors reduce parasitic inductance inserted into the gate-source loop, protecting against catastrophic shoot-through events while minimizing switching losses.

Flexible gate driver technology

A third critical piece required for a total SiC system solution is control. Once again, the fast switching capability of SiC MOSFETs puts a non-optimized system at risk of EMI failure and transient voltage spikes. A new class of gate driver technology is required that allows the designer to manipulate switching dynamics and arrive at optimal tradeoffs. Furthermore, the gate driver must provide rapid detection and response to surge conditions, since SiC MOSFETs have shorter withstand times compared to most Silicon IGBTs.

Using a patented technique called augmented switching (AS), the latest digital gate driver solutions make it possible to pause at a user-specified, intermediate V_{GS} for the desired duration to discharge the Miller capacitance before proceeding to the off-stage V_{GS} (see Figure 2). This contrasts with traditional approaches that take V_{GS} directly from the on-state level to the off-state level, offering the designer no escape route from the system's other, less avoidable pitfalls such as the parasitic inductance of the cable used to connect the load. Indeed, dramatic tradeoffs between voltage overshoot and efficiency may be realized with slight modifications in the Augmented Switching profile (V_{GS} levels and dwell time).

Figure 3 shows turn-off waveforms using two augmented switching profiles and a 1200 V SiC MOSFET module in a D3 (106 mm x 62 mm x 31 mm) package. One can observe that selecting a lower intermediate V_{GS} reduces switching losses where efficiency is a priority, while the use of a higher V_{GS} dampens V_{DS} overshoot and softens the oscillations of all three waveforms. Using the supplied software configuration tool, the gate driver's settings can be fine-tuned at all stages along the development path with the click of a

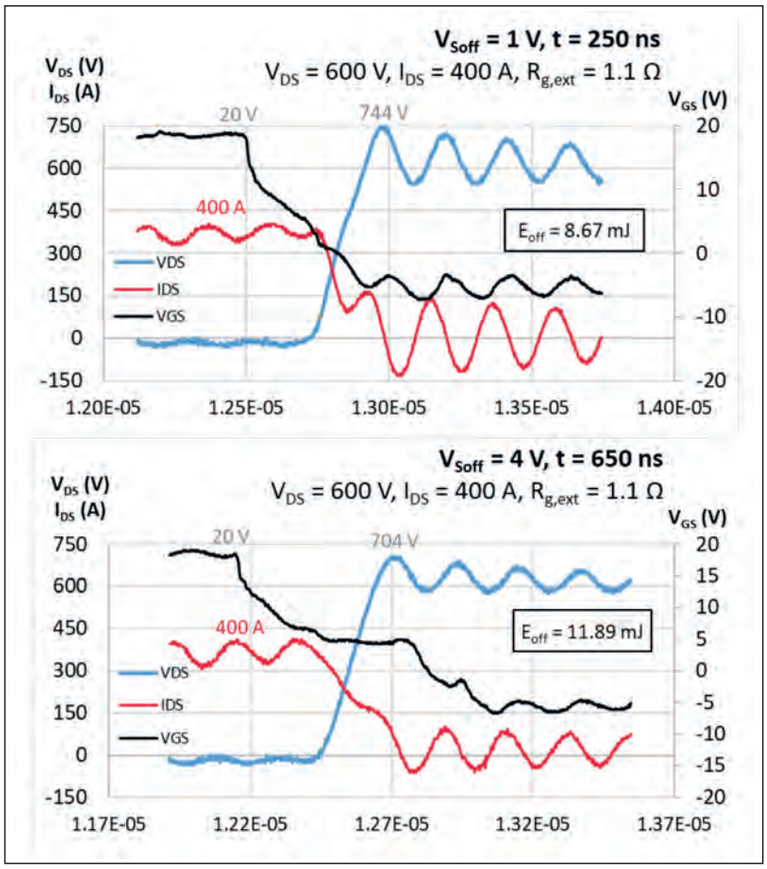


Figure 3: Turn-off waveforms showing the impacts of augmented switching on a SiC MOSFET module

mouse, as opposed to hours spent holding a soldering iron.

Digital gate drivers can also offer enhanced intelligence. For example, they can be used to trigger an entirely different turn-off profile in the case of a fault event to better ensure a safe ride-through. Incorporating AS methods into short circuit protection reinforces the use of a low R_g, as well as guiding the MOSFET through a softer, more controlled transition to the off state with reduced likelihood of avalanche. Still more configurable features include real-time diagnostic measures, such as DC link voltage and temperature monitoring.

As power electronics designers transition from silicon IGBTs to SiC MOSFETs they increasingly rely on component suppliers to provide the critical elements they need to create total system solutions. This includes a SiC MOSFET with proven ruggedness, an ultra-low inductance power package, and a new class of intelligent gate drivers built for ease of optimization. Each is a prerequisite for streamlining the SiC design journey from initial evaluation through field deployment.

Modern Clamping Systems for Tests of Power Semiconductor Devices with 15 kN Force

Power semiconductor devices have many parameters and characteristics that must be measured using specialized equipment. Design of such equipment must account for many factors such as reliability, flexibility, ergonomics, and attention to overall aesthetics. This article describes the steps of development and research carried out to design a clamping system for disc semiconductors and analyzes the encountered issues. A number of technical solutions were used to improve ergonomics, later proving their efficiency in real operation. **Alymov D., Gorodnichina A., Semenov P., Sytyi A., Kazarov A., and Verkhovets V; Proton Electrotex, Russia**

Today power semiconductor devices are the fundamental design elements of various equipment in many industries. Power electronics is constantly evolving and improving, therefore, requirements to the accuracy of measuring their main parameters are also increasing. The Automation Laboratory at the R&D Center of Proton-Electrotex JSC has developed a lineup of test equipment designed to measure parameters of power semiconductors meeting all requirements to accuracy, reliability and ergonomics. It is capable of measuring the following parameters for bipolar semiconductors:

- Parameters in open state: V_{TM}, V_{FM}, I_{TSM}, I_{FSM}, I_L;
- Blocking parameters: V_{RRM}, V_{DRM}, V_{DSM}, V_{RSM}, I_{DRM}, I_{RRM}, $(dVD/dt)_{crit}$;
- Gate parameters: V_{GT}, I_{GT};
- Thermal parameters: R_{th}, Z_{th};
- Dynamic parameters: Q_{RR}, $t_{q,tgd}$.

The test equipment (Figure 1) is a complex including a clamping system and individual measuring units installed in a 19" rack. Each block performs a specific function. Control is carried out using a HMI unit with a 17" capacitive touch screen. The software allows to make several successive measurements in automatic mode. The complex is serviced by one operator. The operator's responsibilities include selection of the measurement profile, installing the device under test in the clamping system and launching the tests with the "Start" button.

Figure 1: Newly test system for comprehensive measurements on bipolar power devices

The tester with the clamping system

Previously the company used test equipment with a number of drawbacks. To make a series of measurements it was required to switch from one test station to another resulting in much lower productivity. Each station occupied production area and required more operators. The operator had to manually adjust the equipment to the required test conditions before each measurement. The clamping systems were based on a pneumatic actuator with several disadvantages: insufficient force to clamp large diameter devices, the inability to dynamically change the speed and force of clamping.

To eliminate these main disadvantages, the Automation Laboratory has developed a state-of-the-art clamping system. The tester consists of two standard 19" racks with measuring units and a clamping system inside. This modular design made it possible to customize the equipment for a specific task by selecting the units needed in the tester. Besides, it made maintenance and repair of the equipment much more convenient significantly reducing the downtime. It is only needed

Figure 2: **Measuring and auxiliary units are designed for a standard 19" rack**

to disconnect the failed unit and replace it with a backup, then the complex is ready for continued operation. Automation of the measurement process minimized the influence of the human factor on the quality and reliability of measurements, while the work of the operator became less critical.

Ergonomics and aesthetics were also considered. Initially the clamping system was designed as a separate mechanism connected to the tester, but this configuration resulted in unused space in the rack above the clamping system. Some units need to be connected with the shortest possible conductors (cables and buses) to ensure precise measurements, so it was decided to include the clamping system in the tester and place the measuring units in the free space above it.

The operator's workplace includes a touch screen, clamping system and a table to put the devices. For convenience, the touch display is detached from the tester on a bracket, allowing the operator to adjust its position as needed. Several ergonomic improvements were made after a survey of operators from the manufacturing. A recess for leg space was made in the housing at the operator's workplace. It was also revealed that the clamping system provides insufficient lighting for the operator to control the process of clamping the system and to track wear of the contact surface. The clamping system was analyzed for the required lighting conditions and light sources were selected and installed both inside and outside the tester.

The measuring and auxiliary units (Figure 2) are placed in housings of various heights designed for a standard 19" rack. Light indicators on the frontal panel inform about the correct operation, while connectors and output buses are located on the rear. To increase the accuracy of measurements a bifilar arrangement of buses is used, both inside and outside the unit.

The clamping system included in the tester is designed to clamp disc diodes, thyristors and separate basic units. The device provides an even distribution of pressure across the entire area of the semiconductor's contact surfaces. It is a separate mechanism consisting of a frame, a drive, a misalignment compensation system and a control unit. The maximum force of 150 kN is enough to clamp large-diameter devices up to 150 mm.

Large-diameter devices have a weight of almost 3 kg. It is physically difficult for the operator to manipulate such a device, and having to use both hands increases the chance of damaging the surface of the device during installation and positioning. To measure the device in the hot state, the preheated device is installed in the clamp between two contact surfaces heated to 190 °C. In case of large-diameter devices this task becomes extremely difficult and dangerous. To resolve this issue, it was decided to equip the clamping system with a draw-out loading system. The lower contact surface automatically extends after the measurements are complete (Figure 3) allowing to easily install a large-diameter device or a device in hot state. The system is equipped with a sensor monitoring the position of the contact surface. If the surface is not properly retracted, the safety system will engage and an error will be shown on the display. For structures and semiconductors of small diameter with weight from 70 to 1000 g, it is much simpler and faster for the operator to install them in the clamp with one hand or tweezers, while the draw-out system will be unnecessary and take extra time. When needed, the draw-out system can be turned off using the touch screen.

To draw out the lower stand and to move the middle plate of the clamp it is necessary to disconnect the bifilar power line. A pneumatic contactor was developed and tested for this purpose. It provides reliable current flow without burning and sticking its contact surfaces.

Clamping system with extended draw-out

Poor contact surface of the clamping

Figure 3: **Draw-out loading system allowing to easily install a large-diameter device or a device in hot state**

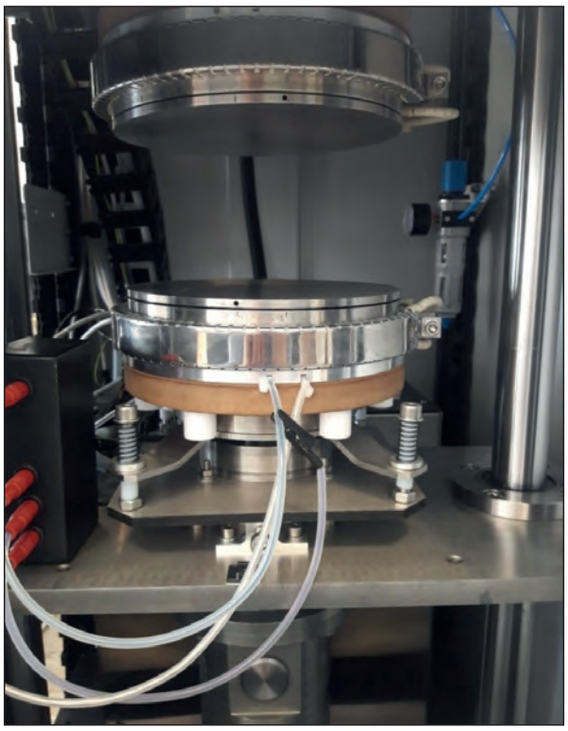


Figure 4: **The clamping system feature replaceable upper and lower contact surfaces**

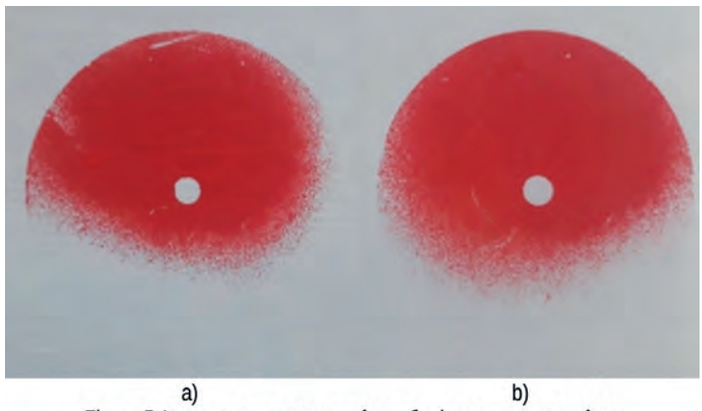
system (Figure 4) can damage the exterior of a semiconductor device and it would need to get scrapped. Therefore, the replaceable upper and lower contact surfaces have a high tolerance for flatness and a roughness of Ra 0.8. For convenience, the surface is quickly detachable, so that replacement of damaged or worn replaceable plates requires short downtime of the equipment. A worn replacement plate can pass grinding and then it can be used again in the clamping system.

For high-amplitude current pulses it is critically important to ensure even distribution of force throughout the contact surface of the semiconductor. Since the areas with concentrated force have minimal resistance and the current flows along the path of the least resistance, high current pulses can cause local overheating and failure of the device. To solve this problem, a system was created to compensate the misalignment of the contact surfaces, thereby increasing the uniformity of the force distribution and, thereby, the current flow through the contact surface of the device. The upper and lower contact surfaces are mounted on spring-loaded hinges. If the surfaces were not parallel before clamping, they get aligned due to spring-loaded hinges. To compensate for the plane-parallel movement that occurs during this alignment, the lower contact surface is mounted on a thrust bearing. This solution improves the distribution of force and reduces the likelihood of damage to the device. The contacts are connected to the power bus with highly flexible braided wire (6th class of flexibility). Using such a flexible connection provides free movement of the compensation system.

The initial design had a single hinge on the lower contact surface, but a large number of tests and trial operation demonstrated inadequate force distribution and a high chance of damage to small-diameter devices, so it was decided to add it to the upper contact surface too. Figure 5.1 shows the force distribution between the device and the contact surface of the clamping unit with one hinge, and Figure 5.2 with two hinges.

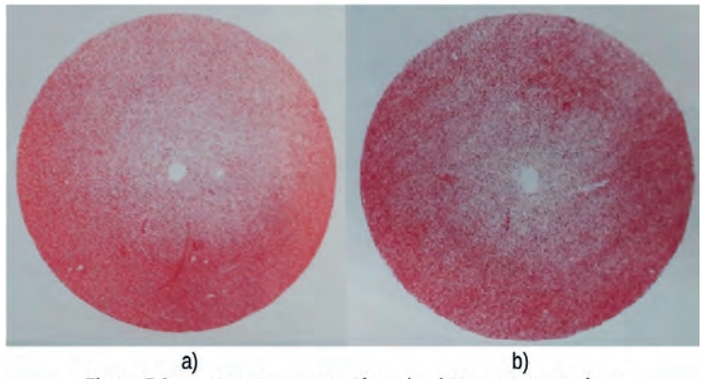
Force distribution between the contact surface and the semiconductor

The clamping system is equipped with a servodrive allowing to control the clamping speed and position of the lower contact surface. For higher productivity, the clamping is divided into stages. Initially the drive develops maximum speed, but then the speed is reduced before the moment of clamping to prevent impact and damage to the device under test. The clamping system has an electromagnetic brake that can maintain maximal force for a long period with high accuracy without putting the load on the drive, making it possible to



a) b)

Figure 5.1: a – upper contact surface; б – lower contact surface.



a) b)

Figure 5.2: a – upper contact surface; b – lower contact surface.

Figure 5: **Force distribution between the device and the contact surface of the clamping unit with one hinge (5.1), and two hinges (5.2)**

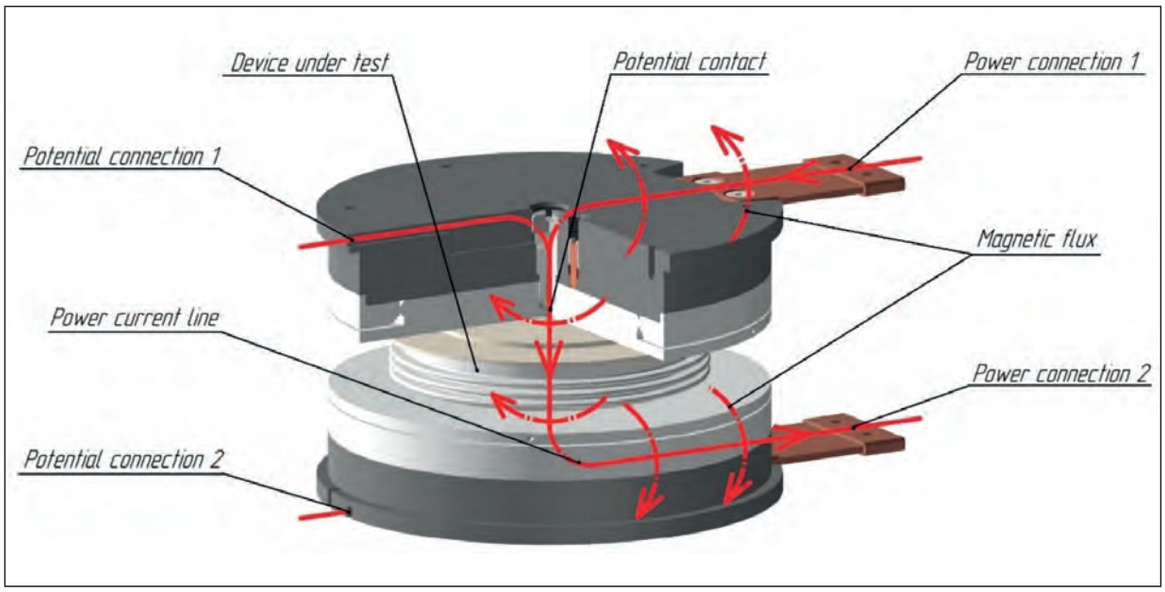


Figure 6: **The clamping system has a power current circuit that passes through the device under test and forms the primary winding of the parasite transformer**

carry out long-term measurements and significantly increase the drive's service life. The drive mechanism is based on a ball screw capable of developing high force and high accuracy of vertical positioning of the device.

The device is also equipped with a heating system to take measurements in the hot state. A ring heater around the contact surface was selected for this purpose since such arrangement does not affect the force distribution. Cartridge or spiral heaters require to make mounting holes in the base of the contact surface resulting in distorted force distribution. Flat heaters were excluded as they are not designed for heavy loads. The heating system is capable of reaching and maintaining a given contact surface temperature of up to +200°C. A temperature regulator and thermal resistance sensors are installed in the measurement zone to maintain and control the temperature.

The clamping system is equipped with potential contacts to measure static losses. They are located in the center of the contact surfaces. The first version had spring-loaded contacts that did not produce expected results. The contact operates at high temperature and experiences mechanical stress during installation. The self-made contact often failed due to sticking, burning and damage, so it was decided to increase reliability by using ready-made spring contacts. Several alternatives were reviewed for this purpose and a series of tests was carried out. The contacts were selected based on dimensions, thermal parameters and spring elasticity. The upper threshold of the operating temperature was at least +200°C. The spring elasticity was chosen based on the weight of the smallest device so that the spring elasticity did not exceed its weight, so a contact was chosen with spring force of not more than 0.8 N. After long-term operation of the selected contacts from several manufacturers to compare their reliability it was decided to use spring contacts made by INGUN.

For operator's safety, an optical safety shutter is installed to prevent access to the working area of the clamping system during testing. Its operation is based on a light curtain of infrared rays formed between the emitter and the receiver located on the same axis. If the beam gets blocked during the device clamping and measuring procedure, it sends a signal to the commutation unit which disconnects the measuring units by hardware and connects the tested device to protective ground, so that the accumulated charge cannot harm the operator. Then the signal is sent to the control unit of the clamping system and the clamping process is suspended. The whole process of stopping measurements and turning off the clamping system takes place in a split second. The emergency stop button located in front of the operator's workplace in easily accessible place works in the same way.

Design of the tester also accounts for the influence of the electromagnetic field loop that is formed when the current flows through the power buses and contacts of the clamping system. A bifilar arrangement of power buses and a material with a low magnetic permeability index were chosen to minimize its effect on measurements. Initially, steel 40X13 was used as the material of the contact surface resulting in transformation effect or the effect of electromotive force induced to the potential removal line. To understand how this effect occurs, consider the system and the principles of the transformer operation. It is based on the phenomenon of electromagnetic induction. This phenomenon arises from the presence of an alternating magnetic field; it is created in a magnetic circuit consisting of a flux guide with electric windings. One winding is connected to an AC source and is called primary, the other winding is used to remove voltage to power the load, this winding is called secondary. If an alternating voltage is applied to the primary winding, alternating current will flow through it, creating an alternating magnetic field around the winding and in the flux guide. It forms a magnetic flux, which passes through the flux guide and crosses the primary and secondary windings and inducing alternating electromotive forces in them.

The clamping system has a power current circuit that passes through the device under test and forms the primary winding of the parasite transformer (Figure 6). It is necessary to measure the voltage drop that occurs on the power semiconductor device when the power current flows. It is achieved using potential spring contacts located in the center of the upper and lower contact surfaces, which form the secondary winding of the parasite transformer together with the wires. The core of the parasitic transformer is formed by contact surfaces. The additional electromotive force occurs on potential

lines as follows. The power current flows through the device along the power circuit and an alternating magnetic field arises, the lines of which are directed according to the screwdriver rule. Accordingly, concentration of the magnetic field in the space between the buses is higher since the magnetic field created by the power conductors is added up. The magnetic field is much weaker at the point where the potential wires are located because it is farther from power buses. Using martensitic steel 40X13 with high magnetic permeability index as the contact node material enhanced the transformation effect. Therefore, it was decided to use D16T aluminum alloy as the main material of the contact unit, and to make the replaceable plate from austenitic 12H18N10T stainless steel. These materials have a low magnetic permeability index. Steel 12X18H10T is hard enough to use as a contact surface. The aluminum alloy D16T is not suitable for the contact surface, as it is a soft material. Using it results in traces remain on the contact surface in after several clamping operations, causing damage to the surface of the device.

Conclusion

To summarize, the test equipment developed and manufactured by the Automation Laboratory of Proton-Electrotex JSC meets the requirements of a wide range of consumers. Modular design of the testers allows the customer to select all the necessary parameters. Using components of well-known leading manufacturers ensure reliability of the equipment. Each case of negative feedback acquired during operation was followed by an in-depth analysis (FMEA – failure mode and effects analysis). This approach allowed to offer high-quality ergonomic equipment.

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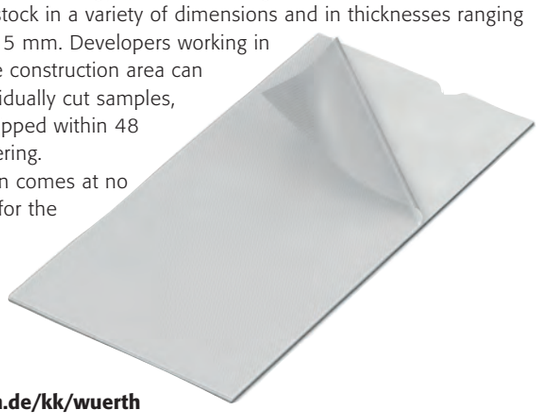

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New products of Proton-Electrotex

Proton-Electrotex continuously works to improve the current product line and develops new solutions in the field of power electronics.
So, the company is ready to present its latest developments:

- IGBT module MIHA housing with a base width of 62 mm and an increased rated insulation voltage of 9500V. The module has several configuration schemes: half-bridge, lower and upper chopper. A special feature of this design is a wide range of operating temperatures - from -55... + 125 °C.

The modules are designed for switching high-power loads and are used as part of converters and drives of small and medium-power electric motors.

- Press-Pack IGBT - module in tablet version with two-way cooling-the sealed design of the module housing makes it possible to work in explosive and aggressive environments. The module has a uniform pressure contact of the active elements, which improves the thermal cycle resistance; in emergency mode, it acquires a stable short-circuited state. The module is applicable for sequential switching circuits and has an operating temperature range - from -60... + 125 °C

The modules are used in flexible AC transmission systems (FACTS), static synchronized compensators (STATCOM), static reactive power compensators (SVC), high-voltage DC power lines (HVDC), wind power plants, voltage inverters for solar panels, railway transport, marine electric drive, electric drive of mining and transport machines.

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The modules are designed for use in energy converters, as well as in other DC and AC circuits of various power electrical installations.

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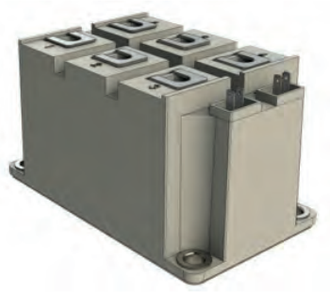
About Proton-Electrotex, JSC:

Proton-Electrotex is the Russian leader in designing and manufacturing power semiconductors including diodes, thyristors and IGBT modules as well as heatsinks, voltage suppressors, resistors and measurement equipment. The company is located in Orel city and ships its products through its partners and distributors all over the world. Please visit website www.proton-electrotex.com for more details about Proton-Electrotex and its offer of products and services.



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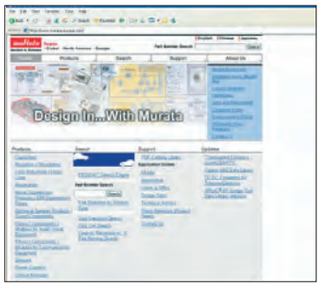

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