POWER
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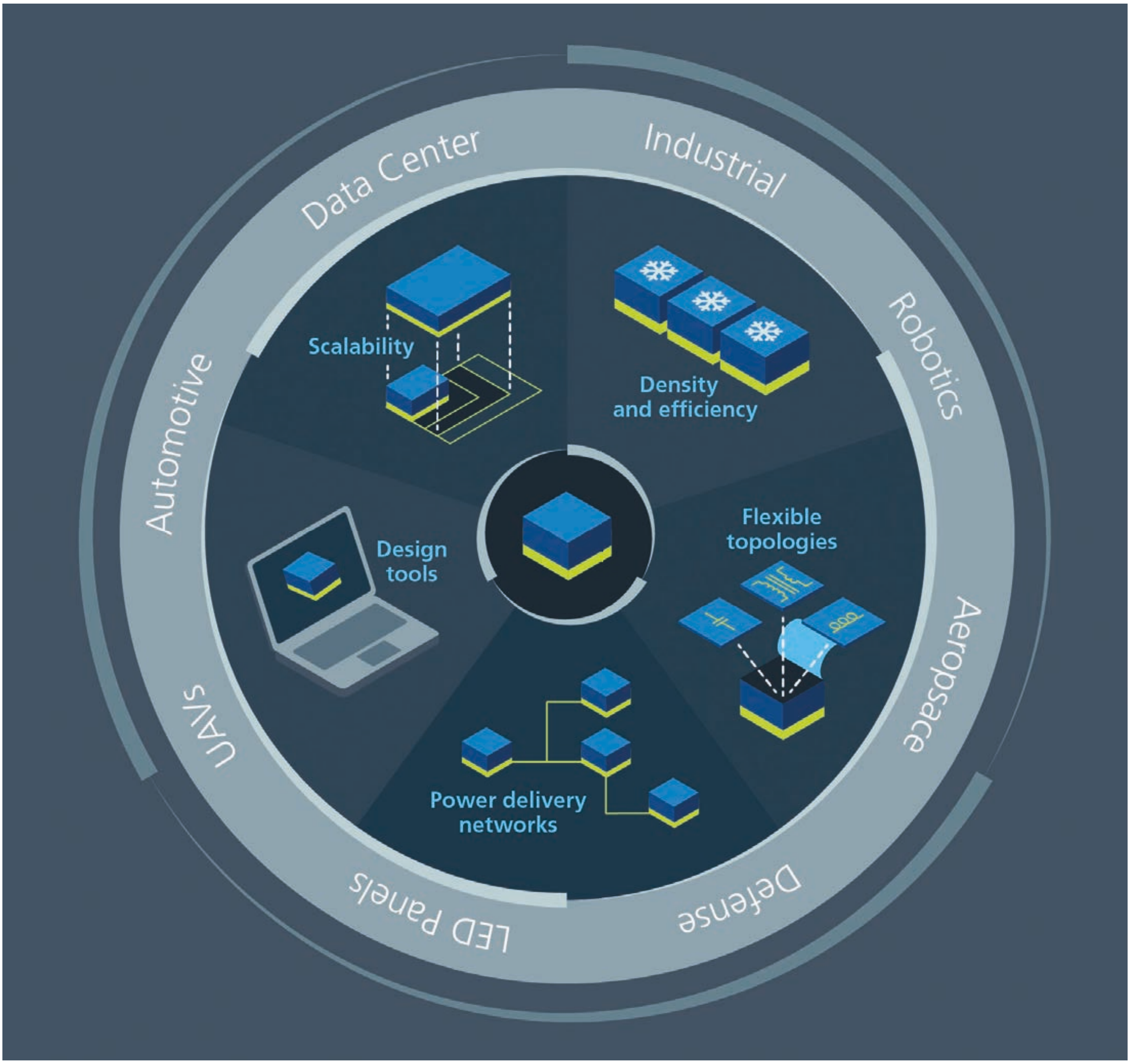
POWER DELIVERY NETWORKS
Power of the Module



THE EUROPEAN JOURNAL
FOR POWER ELECTRONICS
AND TECHNOLOGY

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Opinion | Research | Market News
Industry News | Power GaN
Power Converters | Power Converter Design
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FEATURE STORY

Power of the Module

Vicor has established a power module capability spanning product design, manufacturing, simulation and selection tools. This capability allows Vicor to enable power systems designers to quickly and easily deploy high-performance power delivery networks (PDNs), from the power source to the point-of-load (PoL) for end systems extending across many different industries such as (automotive, AI/data center, defense and aerospace, LED lighting, etc.). Vicor has innovated flexible switching topologies that can adapt to the various power conversion functions and needs. Topologies vary in their functionality, and one or more can be used within a power module. The Sine Amplitude Converter (SAC™) topology is one of the most common topologies and can be quickly configured to different power requirements, primarily by means of changes to the FETs and planer magnetics within the module design. The use of flexible switching topologies allows for quick development time and low risk for new power modules optimized to meet specific application needs. More details on page 17.

Cover image supplied by Vicor Corp., Andover, USA

PAGE 6

Research

PAGE 8

Market News

PEE looks at the latest Market News and company developments

PAGE 14

Industry News

PAGE 20

GaN in Space Applications

Gallium nitride power device technology enables a new generation of power converters in space operating at higher frequencies, higher efficiencies, and greater power densities than ever achievable before. GaN power devices can also exhibit superior radiation tolerance compared with Silicon MOSFETs depending upon their device design. **Max Zafrani, CTO, EPC Space; Alex Lidow, CEO Efficient Power Conversion, USA**

PAGE 24

Maximize Gains Using Miniaturized PoL Converters

System power requirements today are challenging, with designers needing to overcome issues such as multiple supply voltages, voltage sequencing, high transient load currents, and excessive heat. Rather than address these problems at the system power supply, it is more beneficial to introduce measures at the PCB (printed circuit board) level, meaning some form of point-of-load (PoL) converter is required. **Rolf Horn, Applications Engineer at Digi-Key Electronics EMEA**

PAGE 26

Flying Capacitor Topology for Ultra Efficient Inverter Applications

High efficiency and reduced effort for filtering are the main arguments for three-level (3L) topologies. Actually, there are several 3L topologies used in solar applications. The limitation of all Neutral Point Clamped (NPC) three-level topologies is the fact that a 150 Hz ripple has to be filtered with DC capacitors, which are independent on the frequency of the Pulse With Modulation (PWM). With high frequency and utilization of SiC semiconductors it is possible to reduce the size of the output filter, but, however, the DC-capacitors are still required as the same size. There is an alternative Flying-Capacitor (FC) concept in which the 150 Hz ripple is not present. The basic principle of three-level (3L) and four-level (4L) inverter concept is introduced here. **Michael Frisch, Director Product Marketing; Erno Temesi, Chief Engineer; Vincotech Germany and Hungary**

PAGE 33

Web Locator

Superior Precision That Fits in the Palm of Your Hand

Compact Digital-to-Analog Converters with 1-LSB INL

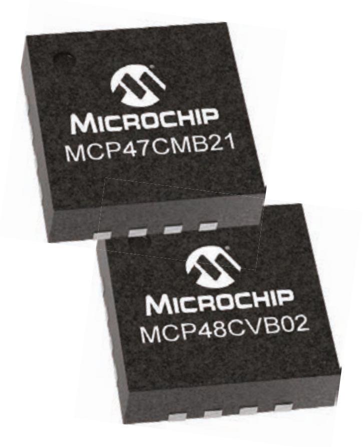
Don’t sacrifice size for performance. Our newest Digital-to-Analog Converters (DACs) deliver outstanding precision and accuracy in compact, integrated chips.

The MCP47/48CxBxx family of DACs combines high alternating current performance and better resistance matching, offering outstanding linearity of less than 1 Least Significant Bit (LSB). With low power consumption and a fast settling time, these solutions are ideally suited to handheld applications for medical, industrial and consumer use.

Supporting an extensive range of output voltage resolutions and integrated memory options, these new devices provide the same flexibility you’ve come to expect from Microchip’s DAC portfolio in a familiar design environment.

Key Features

- 1 LSB Integral Nonlinearity (INL) specification
- Supports 8-, 10- and 12-bit resolution
- Fast settling time of 16 µs
- Power down modes with power-on/brown-out reset protection
- Single and dual channel
- Integrated volatile or MTP memory with SPI or I²C compatible serial interface
- Compact package sizes: 16-lead 3 x 3 QFN, 10-lead MSOP and 10-lead 3 x 3 DFN



www.microchip.com/1LSBPrecisionControl

Battery Innovation Drives EV Penetration

Market researcher IHS Markit projects that electric vehicles (including battery, plug-in hybrid and fuel cell electric) will comprise 60-80 % of all new car sales in 2050. Automotive contractor Hexagon expect that EVs represent a third of the automotive market by 2025, but customers remain concerned about their range and need compelling reasons to buy at current prices, which is setting new expectations for the in-car experience and innovation. In response, carmakers plan to launch 400 new Battery Electric Vehicle (BEV) models by 2025 and manufacturers require efficient ways to develop EV platforms and models, but without prohibitive cost. Such disruption is unprecedented and is driving the need to build upon contemporary design and engineering processes that are the apex of 100 years' automotive advances, and employ new approaches that work in concert with manufacturing lines and suppliers to deliver the same quality and safety for new vehicles in unparalleled timescales.

Hexagon's 100%EV solutions will help the automotive industry to optimize the efficiency of electric powertrains from mechanical design and lubrication to precision machining, optimize the acoustics of the vehicle to avoid motor noise, to optimizing manufacturing and quality inspection to produce more efficient batteries and electric motors.

The increased EV market share (from 2.2 % of new car sales in 2020) will be driven by greater scale in manufacturing, as well as the continued improvement of batteries. One of such examples is Tesla. Total revenue grew by 39 % YoY in Q3 2020. The 3rd hird quarter of 2020 was a record quarter on many levels for Tesla. Over the past four quarters they generated over $1.9 billion of free cash flow while spending $2.4 billion on new production capacity, service centers, Supercharging locations and other capital investments such as a new fab in Germany. The capacity installed should be able to produce and deliver 500,000 vehicles this year. This was achieved mainly through substantial growth in vehicle deliveries as well as growth in other parts of their business. At the same time, vehicle average selling price (ASP) declined slightly compared to the same period last year as the product mix continues to shift from Model S and Model X to the more affordable Model 3 and Y. On September 22 at their Battery Day CEO Elon Musk described a path to reducing battery pack cost per kWh by 56 percent, enabling production of a profitable $25,000 vehicle. This, in Tesla's view, is a critical component to exceed cost parity with internal combustion engine vehicles. Additionally, due to a simpler cell manufacturing process, they believe capex per GWh of battery capacity should decline by 69 percent.

IHS Markit now projects that the average cost of lithium-ion cell cost will fall below $100 per kilowatt hour by 2023. Electric vehicle manufacturing has been the biggest driver for battery innovation since 2011, according to a new report published by the European Patent Office (EPO) and International Energy Agency (IEA). The industry's push to mass produce battery electric vehicles (BEVs) to meet growing consumer demand for greener vehicles, saw patent-filing activity for battery-related inventions soar to a record high of more than 7,000 in 2018. The battery innovation sector is maturing quickly and has grown exponentially between 2000-2018. Much of this is driven by significant investment in the development of BEVs for the mass market. Efficient and long-lasting electricity storage has been a barrier to the take-up of electric vehicles for many years, but recent improvements in the storage capacity of lithium-ion batteries have made BEVs more appealing to the motorist and more commercially-viable as a result. And the next step is ahead - Carbon Nanotubes can increase energy density of the batteries. IDTechEx has forecast the market for CNTs to grow from under $150 mio in 2019-20 to over $500 mio within the next decade. Most of this market movement is linked with the energy storage industry; the demand for lithium-ion batteries will boom over the next decade and CNTs are well-positioned to benefit from this. The nanotubes act as a conductive additive for either electrode in both current and next-generation lithium-ion battery designs, incorporation of a relatively small weight percent can have a significant boost to energy density. The enhanced conductivity is obvious, but the mechanical properties are also very important in providing anchorage that enables thicker electrodes, wider temperature range, or materials that give a higher capacity.

This all drives also the power electronics industry, since by the way Tesla uses SiC MOSFETs in the driver inverter of their Model 3. But in 2020 and certainly 2021 the industry has to deal with a so far unknown issue – the Covid-19 pandemic. The pandemic continues to have a significant impact on Infineon's target markets, according to the Q3 presentation, resulting in weaker demand in many product areas. But CEO Reinhard Ploss is seeing concrete signs of recovery within the automotive sector, which has been particularly hard hit in 2020. Due to the pandemic the PCIM and EPE conferences went digital, electronica 2020 will take place from November 9 to 12 with digital product presentations and a comprehensive program of conferences and speeches. The platform also offers an outlook on the future of the electronics industry. During the CEO Round Table, representatives from the world's leading semiconductor manufacturers such as Infineon Technologies, NXP Semiconductors and STMicroelectronics will discuss the current and future developments in the industry.

It will be interesting to see if this event can present a more impressive experience than the mentioned conferences. Sound quality was often too poor, and switching between platforms for paper presentations and online discussions were frustrating. And the next big event for the power electronics industry will be PCIM Europe 2021 in May and APEC 2021 now in June - planned so far as in-person conference in Phoenix/Arizona. In view of increasing Covid-19 infection numbers I believe both events could go digital.

Achim Scharf
PEE Editor

WBG-Like QJT Power Transistors On Standard Silicon Substrates

Bizen®, a new wafer process technology, has been verified by physical wafer results and calibration to deliver the same voltage levels, switching speeds and power handling performance of wide bandgap devices, claims developers Search For The Next (SFN) at the UK-based University of Nottingham Innovation Park. Industrial partner is UK-based Semefab, the collaboration started back in August 2017 leading to a substantial commitment from both sides until formally agreed in November 2018.

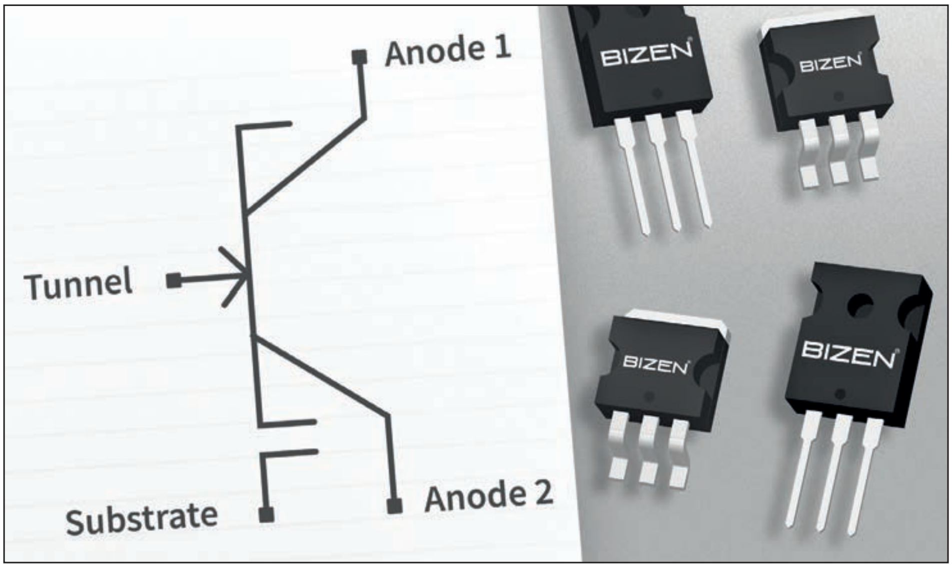
The first devices to use Bizen are members of the QJT (Quantum Junction Transistor) family which will include three parts rated at 1200V/75A, 900V/75A and 650V/32A, available in the industry-standard TO247 or TO263 power MOSFET packages. Of extreme significance is that these devices can be made using standard Silicon substrates on conventional, larger-geometry Silicon processing lines.

"To get this level of performance from traditional Silicon-based MOSFETs, the device size must be much bigger. 1200 V/75 A in a TO247 housing can be achieved using wide bandgap materials like Silicon Carbide, but this approach has other well-known issues. SiC, for example, takes much longer to process and has a significant manufacturing carbon footprint. Also, regardless of the roadmaps, SiC does not scale like Silicon, and the economic argument that SiC can match Silicon does not take into account the advances made possible by Bizen. By contrast, the data we have obtained from physical wafer tests proves that by using Bizen on Silicon substrates, our QJTs deliver the same performance as SiC or GaN. Yet the production equipment required to make a QJT is exactly the same as for a standard Silicon MOSFET, and the Bizen process adds no extra manufacturing complexity," explains David Summerland, CEO and founder of Nottingham-based Search For The Next (SFN) which invented the Bizen technology.

Already, one wafer run is being produced every month by Semefab, and initial analysis is very positive for both power and digital circuits. "We are working closely with Semefab to get products to market as quickly as possible – ideally by the end of the year. No special fab equipment is required, but we are making strategic investments in capital equipment to ensure that the prototyping and proving processes are completed without delay," Summerland expects. "This aggressive timescale is only possible because one of the key attributes of Bizen is that it reduces leadtimes from 15 weeks – which is typical for CMOS – to just 12 days. Bizen also halves thºe number of process layers required while equalling or bettering the speed and low power capabilities offered by current CMOS devices. Based on our initial results which have exceeded our expectations, we are already looking to contract with early adopters; on completion of signing, we will release the PDK to them."

"The new Bizen transistor architecture can wind back the Moores' Law clock by 10 years+, bringing many wafer fabs back into mainstream manufacture. Semefab and SFN are working flat out to make it a success," adds Semefab's CEO Allan James. Semefab have a track record of process development, process induction and volume foundry supporting Silicon based MEMS, CMOS, ASIC, Bipolar-Linear and discrete semiconductor device technologies. Founded in 1986, Fab1 produces a diverse process portfolio of 4" CMOS, ASIC, Bipolar-Linear and discrete semiconductor technologies. Fab1 fabricates precision analogue integrated circuits, JFET transistors, Bipolar transistors, Photo Diodes, Mixed Signal ASICs and supports the 'front-end processing' for many different MEMS technologies. In 2009 Semefab invested £15.2 million, creating Fab 2, for processing of 6" and 4" MEMS technologies and Fab 3 for 6" CMOS/Bipolar technologies. Fab 3 became operational in 2011.

"QJTs deliver the same performance as SiC or GaN on standard Silicon MOSFET production equipment," states David Summerland, CEO of Nottingham-based Search For The Next (SFN)



Bizen devices in different leaded housing


Bizen's Semefab manufacturing fabs

All three Fabs have completely autonomous services and facilities.

Separating the three Fab's ensures the integrity of Fab 3 for producing ultra low leakage junctions, high carrier lifetimes and high reliability MOS transistors. Semefab observes strictly one-way traffic from Fabs 1/3 to Fab 2 and can therefore produce MEMS devices with ultra clean junctions and transistors by starting their lives in Fabs 1/3 and completing their processing in Fab 2 which features heavy metal processing eg: gold and alkali ionic solutions eg: KOH. This ability to segregate processes ensures that Semefab is able to routinely produce MEMS devices with ultra clean semiconductor characteristics where necessary. Quality Management System meets BS EN ISO 9001:2015 Quality Management Systems - Requirements.

Quantum mechanics applied to a traditional bipolar wafer

Bizen applies quantum mechanics to a traditional bipolar wafer process. The result is a very rugged and reliable device with the heritage and pedigree of traditional bipolar Silicon technology. Bizen also reduces leadtimes from 15 weeks – typical for integrating MOS to create large scale integration CMOS – to less than two weeks, and halves the number of process layers; the new QJTs use these same eight layers and wafer process.

The process combines the advantages of bipolar with the disadvantages removed by quantum mechanics and allows fabrication of

- High performance signal BJT and diode.
- Power and signal Zener.
- Resistors Poly and well
- Capacitors Film and well.
- RAM and OTP Memory.
- IPU core.
- 650V High power BJT and diode.
- 650V High power Darlington power BJT.
- Full logic and analogue library.
- Three routing layers included in the eight default layers.

Wafer tests also show that the Bizen process exhibits an effective current gain of over 1 million. This will enable direct connection between the 1200 V/75 A QJT power transistor and a low voltage, low current CPU output port such as a PWM. "The QJT is the first power device on the Bizen family roadmap. This will shortly lead to the PJT (Processor Junction Transistor), an integrated Bizen device with its own processor which can also be produced on a manufacturing cycle time of eight days, heralding a new era of intelligent power devices," Summerland states.

SFN has also released other comparative performance metrics for a 1200 V/100 A part – also in TO247 – which is on its short-term roadmap. The losses at rated current will be one quarter (<300 mV) of those exhibited by the SiC device, and its input capacitance will also be four to five times less (< 1 pF).

https://www.wafertrain.com/

Feature	BIZEN	CMOS	BIPOLAR/TTL
Cost per area of silicon	✓ Low mask layers simple circuit	ⓧ High mask layers	ⓧ Complex circuit
Power per gate	✓ Low quiescent Lowest dynamic	✓ Excellent quiescent Climbing dynamic	ⓧ High quiescent Moderate dynamic
On Resistance	✓ Excellent. Half of mosfet	~ Good at full enh Moderate at low gate	✓ Excellent Half of MOSFET
Logic switching Voltage	✓ 400mV	~ 1.8V to 10V	✓ Less than 5V typ
Pulse current	✓ High	~ Moderate	✓ High
Temperature stability	✓ Excellent	ⓧ 5mV/C	~ Moderate Vbe 2mV/C
Drive Power	✓ Excellent	~ Good at high freq. DC Excellent	~ Moderate
Speed	✓ Fastest	~ Fast	ⓧ Fast but Not practical
ESD sensitivity & O/V	✓ Very Rugged	ⓧ Sensitive	✓ Very Rugged
Integration	✓ Highest	~ High, requires complementary devices	ⓧ Low, requires base resistors
Supply Voltage	✓ Self regulating	ⓧ VDD limit sensitive	ⓧ VCC limit sensitive

Right: Comparison of different semiconductor technologies

Most Of New Car Sales Will Be Electric

Electric vehicles will make up as many as 8 out of 10 new cars sold in 2050. But it will still be a long road before they dislodge gasoline as the predominant fuel in transportation, IHS Markit Vice Chairman Daniel Yergin expects.

Market researcher IHS Markit projects that electric vehicles (including battery, plug-in hybrid and fuel cell electric) will comprise 60-80 % of all new car sales in 2050. That increased market share (from 2.2 % of new car sales in 2020) will be driven by greater scale in manufacturing, as well as the continued improvement of batteries. IHS Markit now projects that the average cost of lithium-ion cell cost will fall below $100 per kilowatt hour by 2023. Nevertheless, gasoline-powered vehicles will still comprise two thirds of the 1.9 billion cars on the road in 2050 owing to the time it takes for the fleet to turn over. The average car in the United States remains on the road for almost 12 years. “At least for now, the demand for electric vehicles is largely coming not from consumers, but from governments whose evolving policies are shaped by climate concerns as well as by urban pollution and congestion,” Yergin observes. Failure to meet new government targets for lowering emissions “could cost European automakers as much as $40 billion in fines” over the next 5 years, he adds. “That is a strong signal that is coming from regulation rather than consumer demand.”

Electric vehicles also bring their own set of challenges, particularly in the supply chain of some battery materials, Yergin observes. Electric vehicle demand for lithium could rise 1,800 % by 2030 and would represent about 85 % of total world demand. Demand for cobalt, another essential element in batteries, could rise 1,400 %. And more than 50 % of global cobalt supply comes from one place—the Democratic Republic of the Congo.

The possible emergence of what he calls a “New Triad” (the convergence of the electric car, ride-hailing and car-sharing services, and self-driving autonomous vehicles) could disrupt oil’s century-long dominance in transportation. This would give rise instead to a new trillion-dollar industry, what he dubs “Auto-Tech.” The advent of Tesla broke “the logjam” that had held since the failure of Thomas Edison’s electric car to gain traction a century earlier, Yergin writes, and major automakers are hastening to catch up and deploy their own electric vehicles. “The world of autos - and their fuel suppliers - has become the arena for a new kind of competition,” he concludes. “It is no longer just about selling cars to consumers for personal use. No longer just automakers versus automakers, no longer gasoline brands versus gasoline brands. It has become multidimensional. Gasoline-powered cars versus electric cars. Personal ownership cars versus mobility services. And people-operated cars versus robotic driverless cars. At this point, there is still no global tipping point where the benefits of new technology and business models prove so overwhelming that they obliterate the oil-fueled personal car model that has reigned for so long.”

www.ihsmarkit.com

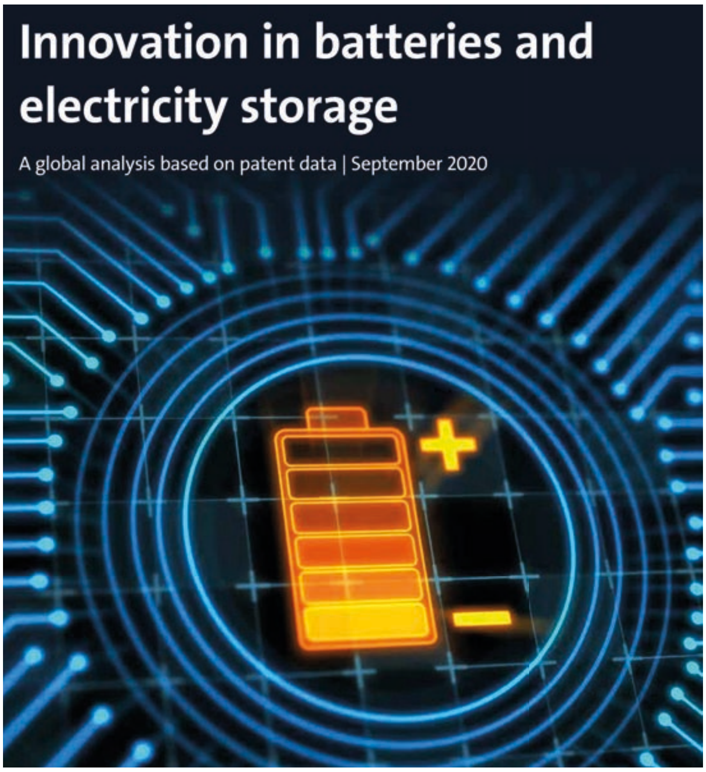
Electric Vehicles Accelerate Battery Innovation

Electric vehicle manufacturing has been the biggest driver for battery innovation since 2011, according to a new report published by the European Patent Office (EPO) and International Energy Agency (IEA). The industry's push to mass produce battery electric vehicles (BEVs) to meet growing consumer demand for greener vehicles, saw patent-filing activity for battery-related inventions soar to a record high of more than 7,000 in 2018.

The report entitled 'Innovation in batteries and electricity storage' shows that inventions in batteries accounted for nine in 10 electricity storage patents filed at the EPO between 2000 and 2018, far outweighing those related to other means of storage. A rapid acceleration in patent-filing activity related to the manufacture of battery cells and other cell-related engineering was also noted in the three years to 2018. From a global perspective, the report reveals that Asian companies in countries including Japan and South Korea, are leading the battery tech innovation race. In fact, a list of the top 25 applicants in battery tech for 2000-2018 includes just six companies in Europe and two in the US. In Europe, companies in Germany are leading the way in electricity storage innovation, filing 5,080 IPFs between 2000 and 2018, well ahead of those in France (1,354) and the UK (652).

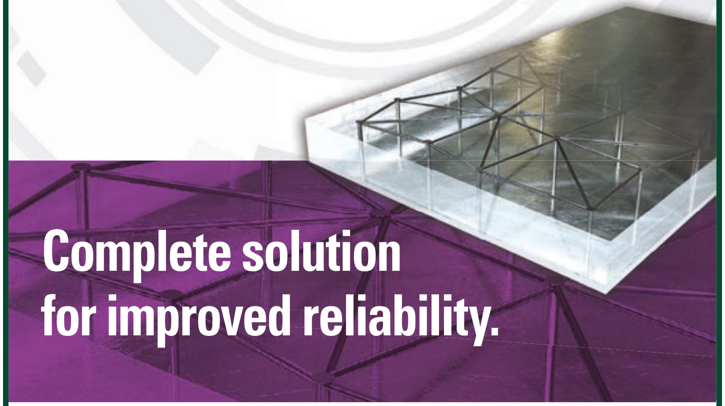
"The report reveals that the battery innovation sector is maturing quickly and has grown exponentially between 2000-2018. Much of this is driven by significant investment in the development of BEVs for the mass market. "Efficient and long-lasting electricity storage has been a barrier to the take-up of electric vehicles for many years, but recent improvements in the storage capacity of lithium-ion batteries have made BEVs more appealing to the motorist and more commercially-viable as a result. Innovation activity originating in the UK is the third-highest in Europe and there are some extremely exciting developments underway. Investment of £4bn in a new Gigafactory to produce batteries and electric vehicles and energy storage solutions is also fuelling R&D activity. We would expect the proportion of battery tech innovation taking place in the UK to increase in future data sets," stated Andrew Thompson, partner and patent attorney at European intellectual property firm, Withers & Rogers. The report can be downloaded at

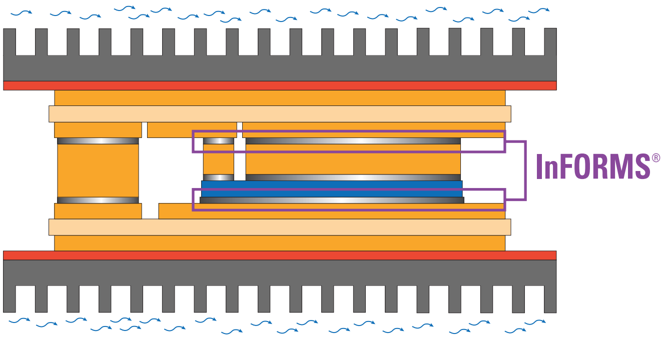
www.epo.org/



Innovation in batteries and electricity storage

A global analysis based on patent data | September 2020





Exploring 2020 EV Advancements

Electric vehicles (EVs) and the wider electric transportation has gone from strength to strength in the past decade. Over the next five years, a total of eight million drivers in the UK will switch to hybrid and electric vehicles (HEVs) according to CompareTheMarket, driving demand for robust charging infrastructure.

"EVs have proven themselves to be one of the top technological success stories of the early 21st century so far. In 2013, a mere 3,500 EVs were registered in the UK. By the close of the decade, this number had risen to approximately 255,000," Steve Hughes, managing director of REO UK reflects the market. "There are several factors steering this change. For automotive manufacturers, it's becoming cheaper to manufacture EVs due to reduced component costs, substantial developments in battery technology and wider availability of large-volume manufacturing for parts such as powertrains. According to Bloomberg NEF, the accelerating rate of these changes will make EVs cheaper upfront than combustion vehicles by as soon as 2022. Then of course there are the environmental factors, in terms of air pollution and carbon emissions. EVs are widely seen to be cleaner alternatives to conventional vehicles due to the substantial difference in carbon emissions from use, with EVs generating only 42 percent of the carbon emissions of a conventional vehicle. Although EV manufacturing has attracted criticism from detractors for producing more carbon emissions - 15 percent according to a report by The Union of Concerned Scientists - than their gasoline-powered counterparts, these differences disappear when EVs are in operation."

The growing adoption of EVs is an undeniable win for environmentalists, but it is something of a double-edged sword for energy systems operators and electrical experts going into 2020.

EV charging points are split into three main categories: slow, fast and rapid. Slow chargers, which typically are rated up to 3 kW, are best suited for home charging as they can take 6–12 hours to fully recharge. Fast charging units are rated either 7 kW or 22 kW depending on whether they are single- or three-phase. Rapid charging, as the name implies, is the fastest. Units are generally rated 43 kW for alternating current (AC) units or 50 kW and above for direct current (DC) chargers. Understandably, users want the fastest charging experience possible. It's for this reason that many automotive manufacturers are investing heavily in developing faster charging infrastructure, such as Porsche's electric pit stop that promises to suitably charge EV batteries in as little as 20 minutes.

"This trend for faster charging points comes as no surprise. It's very possible that slow charging points will largely disappear over the next few years in favour of 7 kW units. This will likely be a slow process as several EV models are only now moving to onboard chargers capable of effectively using 7 kW. Latest models of the Nissan Leaf, for example, have onboard chargers with a capacity of 6.6 kW, almost able to make full use of the 7 kW capacity of a fast point", Hughes expects. "If we imagine that hundreds of thousands of electric vehicles plug in to charge at units rated between 7 and 43 kW, it becomes apparent that grid infrastructure must be robust to handle the demand. However, it becomes more complicated when we account for the rectification that must take place to convert the AC power of many charging points to the DC required for EV batteries. This process introduces harmonic currents into the mains AC signal that, if left untreated, cause higher losses, signal interference and accelerated electrical component wear – none of which are ideal for any connected devices, let alone charging Evs. This is arguably the biggest challenge facing the adoption of EVs and the growing usage of EV charging infrastructure, and it's one that we explore in detail in our recent eBook R30. Unless these harmonic currents are accounted for and mitigated, the electrical grid will face a harmfully noisy electrical signal on top of sudden surges in demand."

Fortunately, electrical contractors can play a crucial role in minimizing the risk by ensuring that any EV charging projects include suitable harmonic filtration components in the surrounding infrastructure. For example, installing one of REO UK's mains line filters or harmonic filters ensures that harmful currents are attenuated and filtered out to avoid damaging the integrity of the mains power. The inclusion of filtering components seems like a common sense solution, yet it remains one that can make a significant difference in overcoming one of the fundamental challenges in EV adoption. In fact, the consideration of such harmonic mitigation strategies at a grid level will be a key trend in EV infrastructure over the coming years. "If we are to see eight million drivers make the jump to EVs in the next five years, we must begin to reinforce our infrastructure now to cope with demand. 2020 will be in a pivotal year in ensuring charging infrastructure is up scratch to meet user expectations, both in terms of charging speed and overall system reliability", Hughes concludes.

www.reo.co.uk

APEC 2021 Rescheduled to June

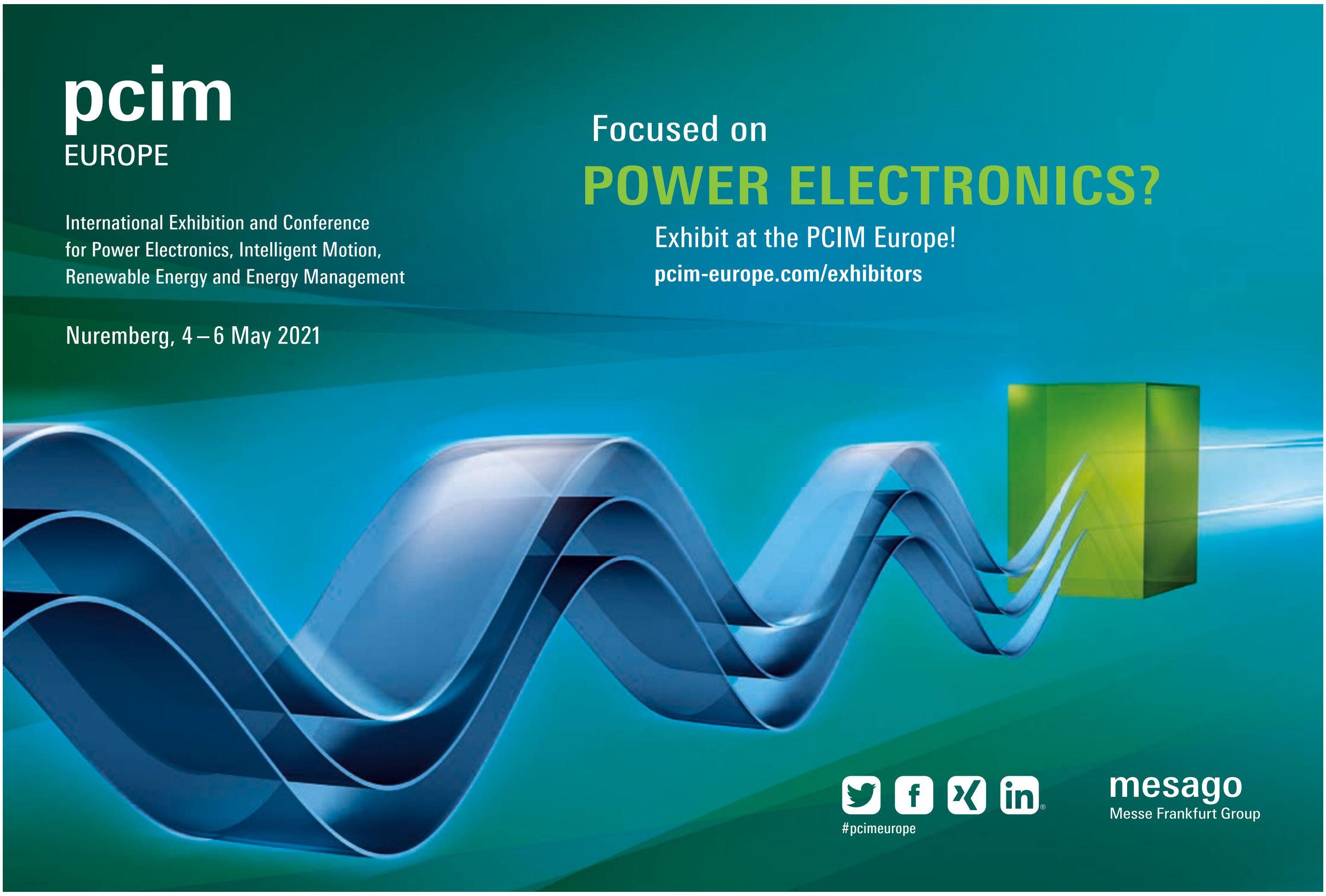
The 36th Applied Power Electronics Conference (APEC) previously scheduled for March moved to June - portals are now reopened for additional submissions for papers and seminars.

The APEC organizers and its sponsors, the IEEE Power Electronics Society (PELS), the IEEE Industry Applications Society (IAS} and the Power Sources Manufacturers Association (PSMA) announced on October 29 that the event will now be held from June 9-13, 2021. The conference had previously been scheduled to take place in March. The location of APEC 2021 will remain, as originally planned, at the Phoenix Arizona Convention Center.

The decision to change the dates of the conference was made after much consideration between sponsors, the city of Phoenix and other stakeholders. By moving to June, the leadership team believes that it will be in a better position to host a safer and more successful in-person event. The committee will continue to assess public health and safety matters in light of the ongoing COVID-19 pandemic and will make any further adjustments, if necessary, in a timely manner. With the change of dates, the organizing committee has reopened the submission process for Technical Papers, Industry Session Presentations and Professional Education Seminars. The revised submission deadlines are now November 23.

Already submitted abstracts to the conference will not need to re-submitted but may amended or updated. The annual APEC event traditionally takes place from Sunday through Thursday. Next year's rescheduled event will begin with Plenary Sessions on Wednesday and continue through Saturday. Detailed updates about the conference schedule, submissions, hotel and travel, other conference-related events, and registration will be posted to the conference website when they become available.

www.apec-conf.org



Hexagon Announces 100 Percent EV Initiative

Hexagon's Manufacturing division launched 100%EV, an initiative to drive innovation in e-mobility. In the wake of 37 countries announcing net-zero carbon targets by 2050, the automotive industry must now both meet legislative ambitions and develop winning models.

Electric vehicles are expected to represent a third of the automotive market by 2025, but customers remain concerned about their range and need compelling reasons to buy at current prices, which is setting new expectations for the in-car experience and innovation. In response, carmakers plan to launch 400 new Battery Electric Vehicle (BEV) models by 2025 and manufacturers require efficient ways to develop EV platforms and models, but without prohibitive cost. Such disruption is unprecedented and is driving the need to build upon contemporary design and engineering processes that are the apex of 100 years' automotive advances, and employ new approaches that work in concert with manufacturing lines and suppliers to deliver the same quality and safety for new vehicles in unparalleled timescales.

Hexagon's design, engineering and manufacturing technologies are employed by industry leaders such as Volkswagen and Bosch, and touch more than 75 % of vehicles produced today, from optimizing the efficiency of new EV powertrain design and production to quality inspecting new range-boosting batteries. Through 100%EV, Hexagon is focussing its combined technologies and expertise to help manufacturers integrate these processes and accelerate the global transition to EVs. “We believe the journey towards a cleaner and more sustainable 100% EV future can, and should, be accelerated through innovation. The automotive industry is rallying to meet the demanding deadlines for the rollout of EVs, but wrestling with the complexity of producing new vehicles that consumers want to buy,” says Paolo Guglielmini, President, of the company's Manufacturing division. “EV development is just getting started. There is a race to build better and more tailored models and we want to help companies think beyond contemporary practices and win market share. We believe such a rapid pivot can only be addressed through smart manufacturing technologies that support e-mobility development from concept to customer, making the journey toward 100% EV faster and more cost-effective.”

Hexagon's 100%EV solutions will help the automotive industry to optimize the efficiency of electric powertrains from mechanical design and lubrication to precision machining, optimize the acoustics of the vehicle to avoid motor noise, to optimizing manufacturing and quality inspection to produce more efficient batteries and electric motors. Hexagon's is headquartered in Stockholm employing 20,000 people in 50 countries at net sales of € 3.8 bn.

https://hexagonmi.com/eMobility

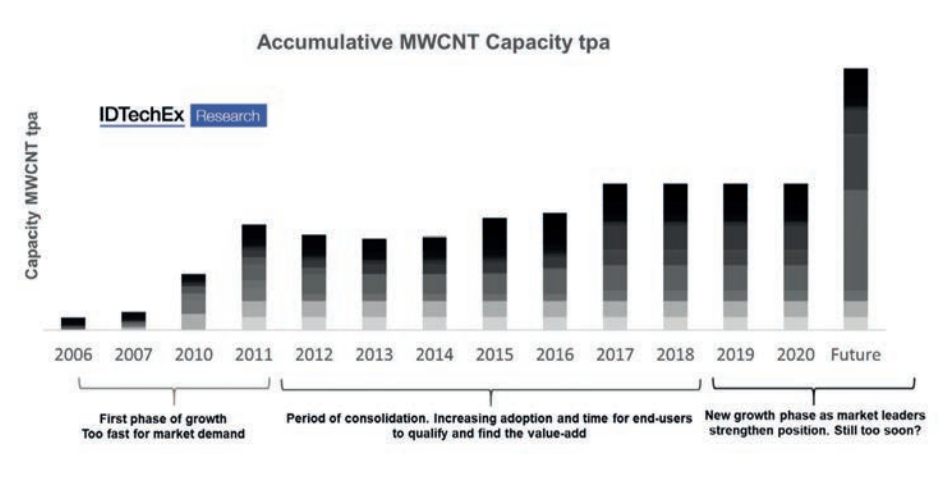
Carbon Nanotubes Increase Energy Density

Carbon nanotubes (CNTs) have been known for many decades, but the moment of significant commercial growth is just approaching. Through expansions, partnerships, acquisitions, and greater market adoption there are clear indicators that now is the time for true market success to be realized.

In the report "Carbon Nanotubes 2021-2031: Market, Technology, Players", IDTechEx has forecast the market for CNTs to grow from under $150 mio in 2019-20 to over $500 mio within the next decade.

Most of this market movement is linked with the energy storage industry; the demand for lithium-ion batteries will boom over the next decade and CNTs are well-positioned to benefit from this. The nanotubes act as a conductive additive for either electrode in both current and next-generation lithium-ion battery designs, incorporation of a relatively small weight % can have a significant boost to energy density. The enhanced conductivity is obvious, but the mechanical properties are also very important in providing anchorage that enables thicker electrodes, wider temperature range, or materials that give a higher capacity. How they are dispersed, used with or without a binder, and combined with other additives are all examined in extensive detail. Given the diverse range of properties, the market potential for MWCNTs extends far beyond lithium-ion batteries, with conductive polymers, ultracapacitors, coatings, thermal interface materials, and more all-seeing market uptake and detailed throughout the report.

www.IDTechEx.com/CNT



Cree Sells LED Business To SMART Global Holdings

Cree announced on October 20 that the Company has entered into an agreement to sell its LED Products business unit (Cree LED) to SMART Global Holdings, Inc. for up to $300 million.

Under the terms of the agreement Cree expects to receive an initial cash payment of $50 million upon closing and $125 million to be paid upon maturity of a seller note issued by SMART due August 2023. Cree also has the potential to receive an earn-out payment of up to $125 million based on the revenue and gross profit performance of Cree LED in the first full four quarters post-transaction close, also payable in the form of a three-year seller note. "We are pleased to announce the sale of our LED Products business to SMART, which represents another key milestone in our transformational journey to create a pure-play global semiconductor powerhouse," said Cree CEO Gregg Lowe. "This transaction uniquely positions us with a sharpened strategic focus to lead the industry transition from silicon to silicon carbide and further strengthens our financial position, which will support continued investments to capitalize on multi-decade growth opportunities across EV, 5G and industrial applications." Cree LED has one of the industry's widest portfolios of highly efficient LED chips and high-performance LED components and represents one of the strongest brands in the industry. SMART is a global leader in specialty memory, storage and high-performance computing solutions serving the electronics industry for over 30 years.

www.cree.com

GaN Semiconductors Reliability Tests

While GaN has the performance and cost to meet design requirements, GaN’s usage history is around ten years whereas Silicon’s is decades. Testing under severe conditions is required to qualify these products. And Testing-to-failure is required to verify failure modes and determine product lifetimes.

The power transistor industry is familiar with the qualification guidelines in the Joint Electron Device Engineering Council (JEDEC) standards written with Silicon transistors as the foundation. With GaN, device material is different and hence, the failure modes and mechanisms are different. Determining how and which testing guidelines within JEDEC and AEC-Q apply is part of the work the GaN industry has studied. Compounding this analysis is that mission profiles that model electronic system lifetimes are changing. For example, internal combustion engines requiring 8,000 hours of working life have increased dramatically for HEV/EV onboard chargers requiring >30,000 hours – nearly a 4X increase.

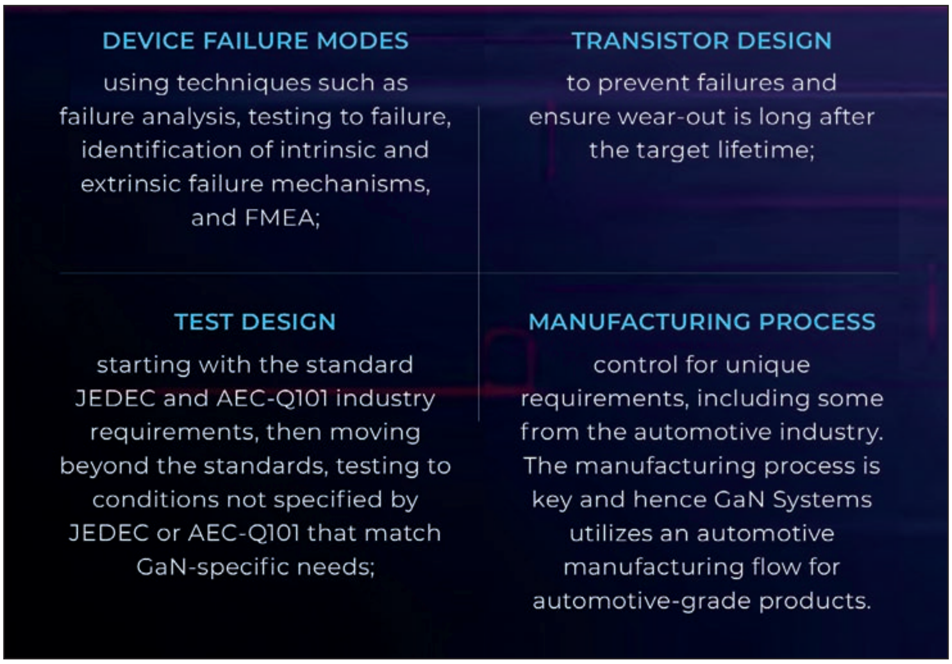
The expectation for the GaN industry is to demonstrate that electronic systems built with GaN inside have at least the same lifetime expectations as Silicon MOSFETS, and ideally, better lifetimes. The industry is making progress with working groups in the JEDEC JC70 committee chartered to define a set of tests, conditions, and pass/fail criteria for GaN power devices to ensure the reliability of customer systems under required mission profiles.

Several challenges arise

But not all failure mechanisms are the same for each of the suppliers and some suppliers may not have the expertise to know the failure mechanisms of their new devices. For those companies that do know the failure mechanisms and have the know-how to correlate failure mechanisms to tests, screens, and design requirements to ensure reliability, that knowledge is used as a competitive advantage. As a result, there is limited knowledge sharing - there is a competitive advantage for those suppliers who know and understand application mission profiles for their targeted segments. Some suppliers have different technology priorities resulting in biases – some have Silicon and GaN, some have GaN only, and some have Silicon, SiC, and GaN creating differing vested interests.

Test	Conditions	Sample size (parts x lots)							Failures
		GS66502B 200mΩ	GS66504B 100mΩ	GS66506T 67mΩ	GS66508B 50mΩ	GS66508T 50mΩ	GS66516B 25mΩ	GS66516T 25mΩ	
HTRB	T_j = 150°C, V_{DS} = 80%, t= 1000 hrs	77x3	77x3	77x3	77x3	77x3	77x3	77x3	0
HTGB	T_j= 150°C, V_{GS}= 100%, t= 1000 hrs	77x3	77x3	77x3	77x3	77x3	77x3	77x3	0
	T_j= 150°C, V_{GS}= -100%, t= 1000 hrs	77x3	77x3	77x3	77x3	77x3	77x3	77x3	0
H3TRB	T_j= 85°C, RH= 85%, V_{DS}= 100V, t= 1000 hrs	77x3	77x3	77x3	77x3	77x3	77x3	77x3	0
TC	-40°C to +125°C, 1000 cycles	77x3	77x3	77x3	77x3	77x3	77x3	77x3	0
HTS	T_a= 150 °C, t= 1000 hrs	77x3	77x3	77x3	77x3	77x3	77x3	77x3	0
IOL	ΔT_j= 100°C, 2 min on, 2 min off, 5k cycles	77x3	77x3	77x3	77x3	77x3	77x3	77x3	0
MSL3	T_a= 60°C, RH=60%, t= 40 hrs followed by 3x reflow cycles	77x3	77x3	77x3	77x3	77x3	77x3	77x3	0
ESD	HBM+CDM	30x1	30x1	30x1	30x1	30x1	30x1	30x1	0
Solderability	Dry bake (condition E)	10x3	10x3	10x3	10x3	10x3	10x3	10x3	0

650V products JEDEC qualification



DEVICE FAILURE MODES

using techniques such as failure analysis, testing to failure, identification of intrinsic and extrinsic failure mechanisms, and FMEA;

TRANSISTOR DESIGN

to prevent failures and ensure wear-out is long after the target lifetime;

TEST DESIGN

starting with the standard JEDEC and AEC-Q101 industry requirements, then moving beyond the standards, testing to conditions not specified by JEDEC or AEC-Q101 that match GaN-specific needs;

MANUFACTURING PROCESS

control for unique requirements, including some from the automotive industry. The manufacturing process is key and hence GaN Systems utilizes an automotive manufacturing flow for automotive-grade products.

Key elements of GaN Systems’ reliability strategy

As is typical with all global industry standards, consensus takes time and progress can be slow. GaN Systems works diligently with the JC70 committee to ensure a robust standard is produced. In parallel with the JC70 efforts, GaN Systems embarked on a collaborative approach to the lifetime and reliability challenge working with selected companies in the global automotive, industrial, and high-reliability (HiRel) markets. Together, GaN Systems and its team partners developed a qualification strategy and process to ensure that GaN power devices are reliable and robust in applications today and in future.

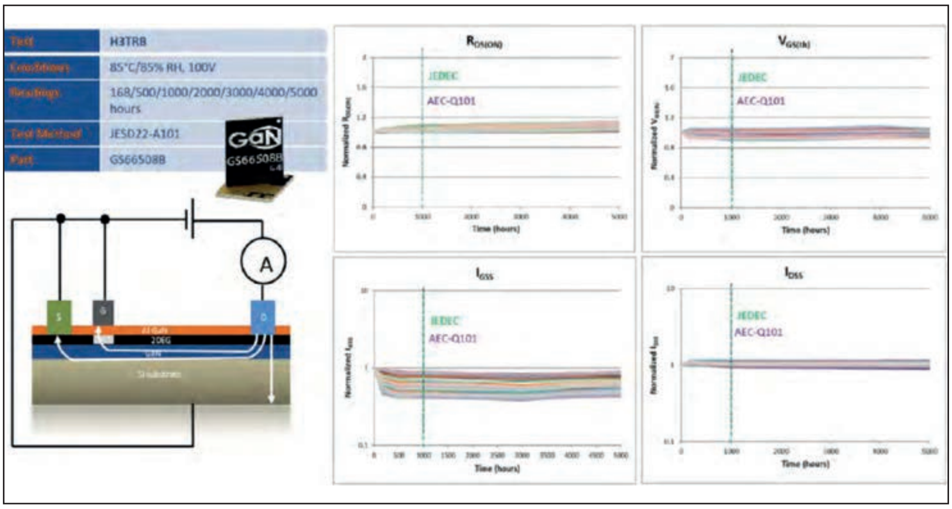
Testing methods

Qualification testing is a series of laboratory tests carried out under known stress conditions to evaluate the device under accelerated voltage, temperature, humidity, and other stress conditions. Qualification tests are performed to ensure that semiconductor devices perform as designed both before and after the stresses.

The results of the collaborative effort described include standard JEDEC and AEC-Q101 tests

Test	Conditions	Sample size (parts x lots)			Failures
		GS61004B 15mΩ	GS61008P 7mΩ	GS61008T 7mΩ	
HTRB	T_j = 150°C, V_{DS} = 80%, t= 1000 hrs	77x3	77x3	77x3	0
HTGB	T_j= 150°C, V_{GS} = 100%, t= 1000 hrs	77x3	77x3	77x3	0
	T_j= 150°C, V_{GS} = -100%, t= 1000 hrs	77x3	77x3	77x3	0
H3TRB	T_j= 85°C, RH= 85%, V_{DS}= 80%, t= 1000 hrs	77x3	77x3	77x3	0
TC	-40°C to +125°C, 1000 cycles	77x3	77x3	77x3	0
HTS	T_a= 150 °C, t= 1000 hrs	77x3	77x3	77x3	0
IOL	ΔT_j= 100°C, 2 min on, 2 min off, 5k cycles	77x3	77x3	77x3	0
MSL3	T_a= 60°C, RH=60%, t= 40 hrs followed by 3x reflow cycles	77x3	77x3	77x3	0
ESD	HBM+CDM	30x1	30x1	30x1	0
Solderability	Dry bake (condition E)	10x3	10x3	10x3	0

100V products JEDEC qualification



Extended duration testing example for H3TRB test

applied as a baseline as well as additional test methods implemented for the differences between Silicon and GaN. All tests were designed for both extrinsic and intrinsic failures and failure modes and mechanisms were identified using FMEA and test-to-failure methods. Extrinsic failure mechanisms are those caused by an error occurring during the design, layout, fabrication, or assembly process or by a defect in the fabrication or assembly materials. Intrinsic failure mechanisms are those caused by a natural deterioration in the materials or by the way the materials are combined during fabrication or assembly processes that are within specification limits.

To demonstrate design margin beyond JEDEC requirements, testing was extended beyond the standard JEDEC time durations. This extended testing duration demonstrates significant design margin. An example of the extended testing performance to the JEDEC JESD22-A101 test procedure for H3TRB performance show stable performance at 5X the required test duration for both JEDEC and AEC-Q101 test specifications. The joint efforts with industry leading experts in the automotive, industrial, and aerospace markets, GaN Systems has implemented an enhanced-JEDEC incremental test methodology.

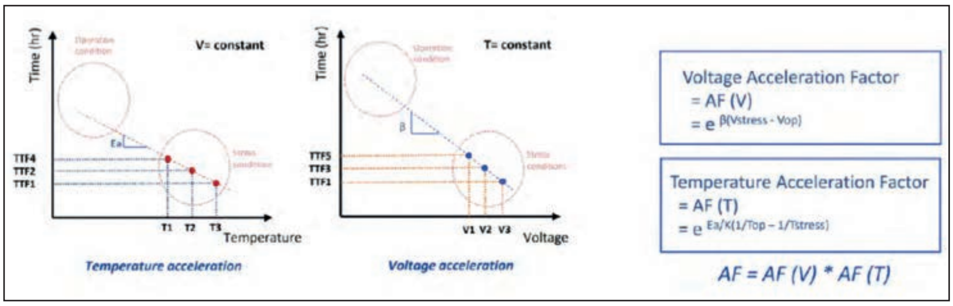
For automotive qualified GaN Systems products, a similar approach is followed consisting of completing the standard AEC-Q101 tests and then supplementing those with incremental tests to accommodate for the differences between GaN and Silicon. The enhanced-AEC-Q101 product reliability test methods were developed to properly evaluate the differences between GaN and Silicon transistors. Method implementation resulted from the knowledge and key learnings gained from collaborative partners who shared decades of experience of Silicon failure mechanisms only identified in field-based applications, sometimes years after technology release-to-market. Each test was then designed based on this input and specific failure mechanisms in the FMEA.

Lifetime testing

Qualification of GaN Systems transistors leads to the next natural customer question: How long will the system lifetime be with GaN Systems devices? To understand Lifetime requires comprehensive knowledge of the failure modes, failure mechanisms, the Mission Profile, and the design of the product.

Once the failure mechanisms have been understood, the selection of tests follow based on accelerating the failure mechanisms. GaN Systems starts with a design and a process FMEA, builds parts, step-stress testing, and parts-to-failure testing to define the lifetime models. Over the course of the past 12 years, design rules have been updated. The fabrication process and screening have improved with learning from the FMEA/Build/Test-to-failure process so that product lifetimes have increased with each successive product family.

Lifetime models show that a semiconductor component will perform in accordance with expectations for a predetermined period of time in a given environment. To be efficient, lifetime testing compresses the time scale by using high stress levels to generate failures. Once the lifetime under accelerated stress is obtained, an acceleration model is used to predict the product lifetime under normal application stress. Care must be employed to ensure the stress level is appropriate. The stress should accelerate the failure mode that is being examined, not other failure mechanisms.

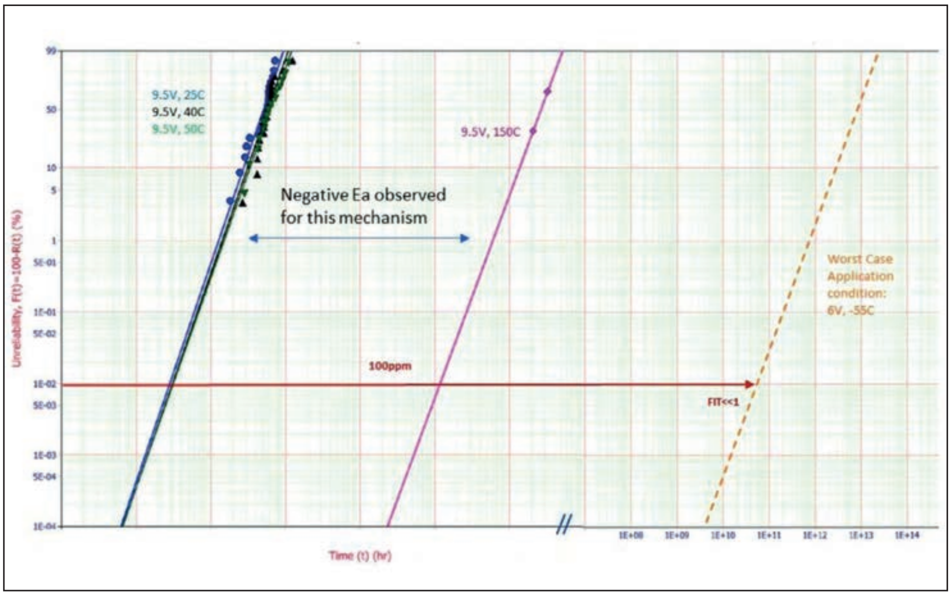


Lifetime acceleration factors

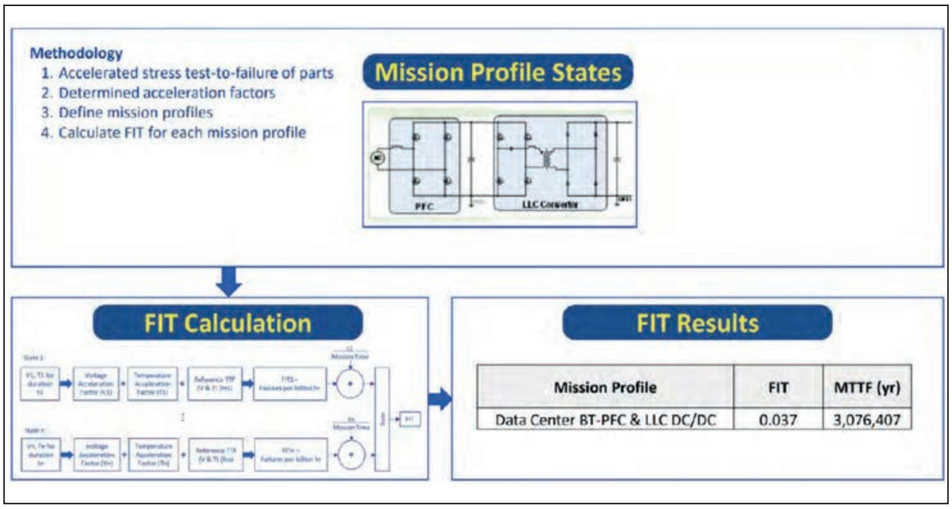
Lifetime models are a well understood methodology that include the use of voltage and temperature or other accelerants to calculate acceleration factors using Weibull plots and determine Failure in Time (FIT) under specific operating conditions (the mission profile).

In GaN Systems approach, a dominant failure mode is TDSB (Time Dependent Schottky Breakdown). TDSB's Weibull plot demonstrates the need to fully understand device failure mechanisms. Interestingly, this test to failure was performed at lower temperatures as this failure mechanism has a slight negative activation energy. That means the lower the temperature, the shorter the lifetime. That's the reason 6 V and -55°C were considered as worse case application conditions. The 9.5 V and 150°C line was added to reconfirm the negative activation energy.

A lifetime prediction of a data center power supply with GaN transistors in the bridgeless totem-pole PFC circuit and in the LLC DC/DC circuit has been carried out as an example. The inputs to the FIT calculation include the accelerated stress time-to-failure of the GaN Systems transistors, measured acceleration factors, and definition of the system operating mission profile states, including different operating voltages, temperatures, and durations. The FIT calculation is performed, and the results confirm that GaN Systems devices have very good lifetime for the data center application with a FIT result of 0.037 which is well under the benchmark of 1.0 by a factor of 27.



Example of TDSB Weibull Plots



Methodology
1. Accelerated stress test-to-failure of parts
2. Determined acceleration factors
3. Define mission profiles
4. Calculate FIT for each mission profile

Mission Profile States

FIT Calculation

FIT Results

Mission Profile	FIT	MTTF (yr)
Data Center BT-PFC & LLC DC/DC	0.037	3,076,407

Data Center Power Supply Mission Profile Example

Literature

"GaN Semiconductors Qualification and Reliability", GaN Systems White Paper, October 2020

www.gansystems.com

Power of the Module

Vicor has established a power module capability spanning product design, manufacturing, simulation and selection tools. This capability allows Vicor to enable power systems designers to quickly and easily deploy high-performance power delivery networks (PDNs), from the power source to the point-of-load (PoL) for end systems extending across many different industries such as (automotive, AI/data center, defense and aerospace, LED lighting, etc.).

Robert Gendron, VP of Product Marketing, Vicor Corporation, USA

This modular power component approach signifies a new standard within the power industry, addressing the increasing power needs of modern, high-performance end systems with a methodology that also provides other power system benefits such as reduced power system footprint, high efficiency and faster time to market.

The need for power modules

Power delivery networks are rapidly changing within many end systems across many industries today. The power requirements for these different systems vary widely from each other and require a wide portfolio of modules to enable the maximum flexibility for a modular power component methodology to be employed. The range of modular power solutions Vicor provides include:

- AC/DC and DC/DC modules
- Power levels from 50W to over 50kW
- Currents from a few amps to 1,000A+
- Voltages from sub 1V to over 1,000V
- Isolated and non-isolated converters and regulators
- Regulated and fixed-ratio converters
- Board-mount, chassis-mount and surface-mount power module packages

In addition to the above, there are also different control features such as telemetry, compensation and programability, plus any industry/safety certifications that can be required.

To effectively support different PDNs in different industries with an optimized solution, a comprehensive power module approach in needed. Utilizing power modules follows the practice and benefits of a mass customization capability. Mass customization enables the ability to offer unique PDNs optimized for different end systems while benefitting from common design and manufacturing processes. Common, scalable design and manufacturing processes also offer advantages in faster time-to-market, reliability, technology risk and cost management.

The key elements of this power module Approach are:

- Modular power component design methodology – the ability for the end designer to select, configure, optimize and source a unique power delivery network comprised of different power modules
- Power module design – the power modules themselves are assembled within a common manufacturing process and can easily be configured by utilizing:
- Flexible power switching topologies and control systems
- Configurable and scalable packaging

Modular power component design methodology

Multiple PDN designs are enabled by a large power module portfolio offering a range of functionality, scalability and performance. Selecting the optimized power modules for different power delivery architectures out of the portfolio and building the highest performing PDN is possible with the Power System Designer and Whiteboard tools (Figure 1). These tools provide an environment to analyze different architectures and modules optimized for overall performance, cost or size considerations. The modular power component design methodology—supported by a large power module portfolio and tools for selection and optimization—is the more visible element to the Vicor power module approach since customers use it to interface with Vicor daily. It is the second element of power modules, the power module design itself, that is not as visible to customers – but it is equally important to providing the benefits of mass customization.

Flexible switching topologies

Vicor has innovated flexible switching topologies that can adapt to the various power conversion functions and needs. Topologies vary in their functionality, and one or more can be used within a power module. The Sine Amplitude Converter (SAC™) topology is one of the most common topologies and can be quickly configured to different power

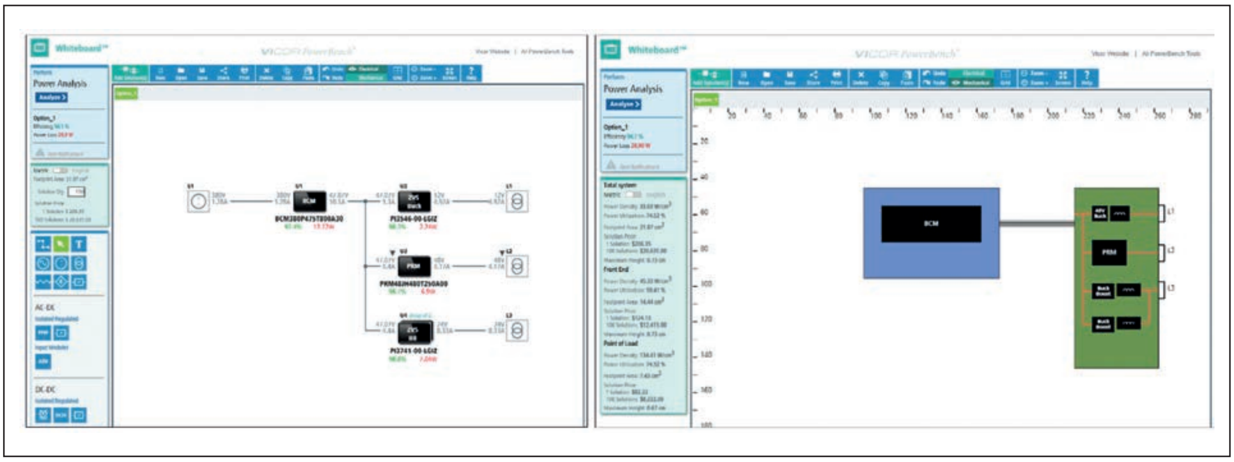


Figure 1: Example of a power delivery network designed and optimized using the Vicor Whiteboard tool

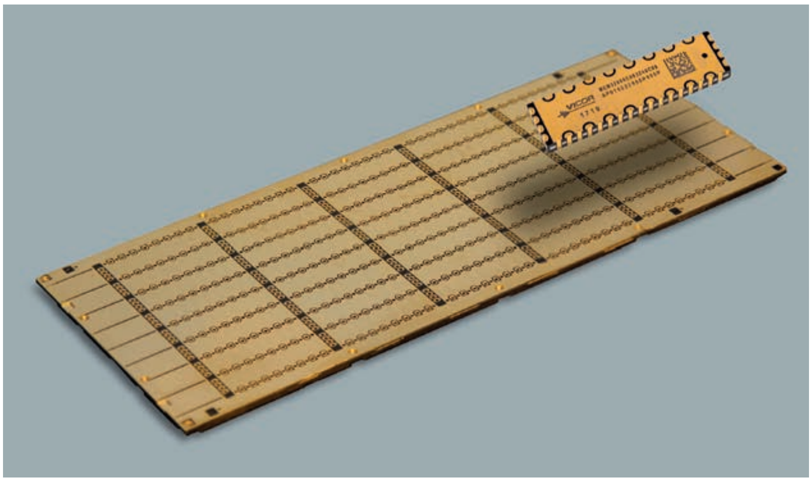


Figure 2: Panel fabrication process enabling configurable CM-ChiP packaging

requirements, primarily by means of changes to the FETs and planer magnetics within the module design. The use of flexible switching topologies allows for quick development time and low risk for new power modules optimized to meet specific application needs.

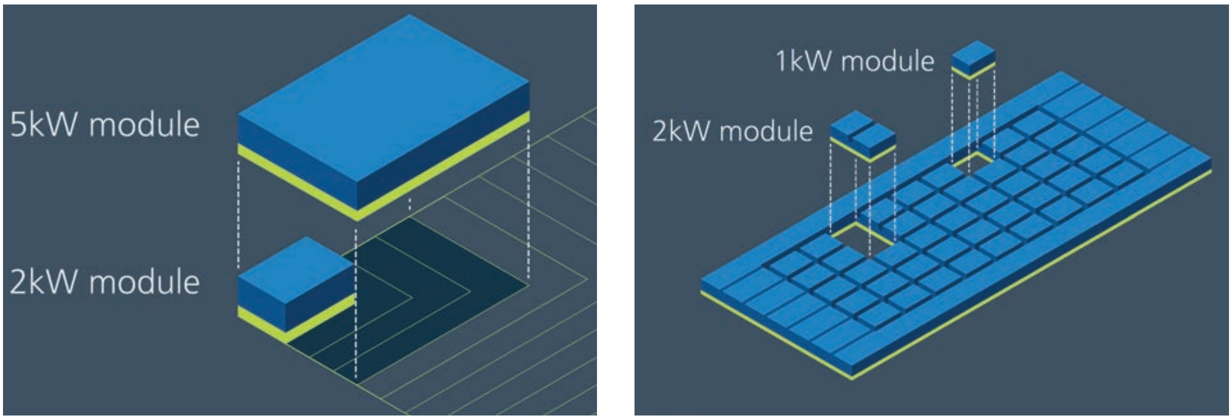


Figure 3: Scaling approaches with the panel fabrication process: linear scaling (a) and integer scaling (b)

Configurable and scalable packaging

Vicor developed the CM-ChiP™ common package technology to maximize power module density and thermal performance. The CM-ChiP package is a 3D package with an internal mid-plane substrate that enables component placement on both the top and bottom sides. Package thermal impedance is equal from the top and bottom sides of the package, allowing for dual-sided cooling if desired. Exterior plating options provide flexibility for shielding options and terminal connections, which include surface-mount, pinned and chassis-mount terminations. No tooling is required for different form factors or terminal connections. By using the CM-ChiP common package technology, a faster time to market and a higher level of performance predictability can be achieved in new power module designs.

The CM-ChiP is fabricated within a panel fabrication process, which is similar to a wafer fabrication process (Figure 2). Both processes enable multiple modules or devices to be fabricated from a single panel or wafer, standardized on a fabrication line. The panel can accommodate various module form factors with the largest possible module utilizing the full panel. A critical element to mass customization, the panel fabrication process shifts the manufacturing focus away from conventional fragmented, single-component package support and yield-enhancement efforts towards panel-level efforts that encompass all products.

Flexibility within the PDN architecture and design includes the ability to parallel most power modules for increasing system power demands. In addition, Vicor can increase module power delivery by scaling the power module itself to a larger size. Scaling can be accomplished by module linear scaling, increasing the power capability by modifying the core module design to a higher power level. Another scaling option is integer scaling where 2x, 3x, 4x power capability is possible by singulation of more than one base module from the panel (Figure 3).

Advanced modular power delivery network examples

When artificial intelligence (AI) processor power system designers wanted to maximize their processor performance on an AI accelerator card, they turned to Vicor. Power performance requirements for the processor called for the delivery of 500 A+ at a sub-1 V level (Figure 4). In addition, the power delivery network needed to fit within the industry-standard Open Compute Platform OAM card pushing the power density limits of

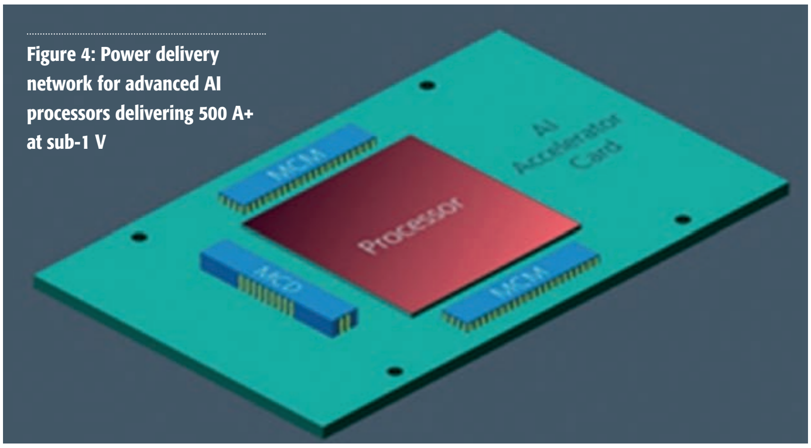


Figure 4: Power delivery network for advanced AI processors delivering 500 A+ at sub-1 V

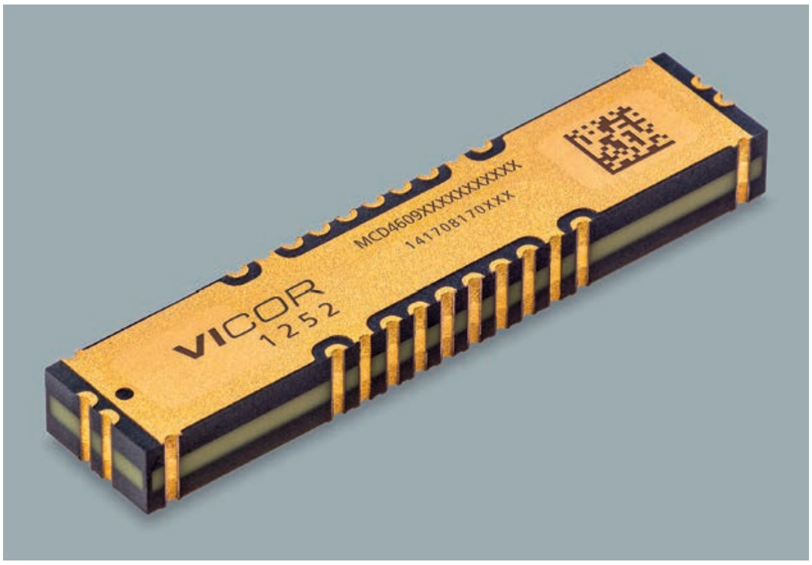


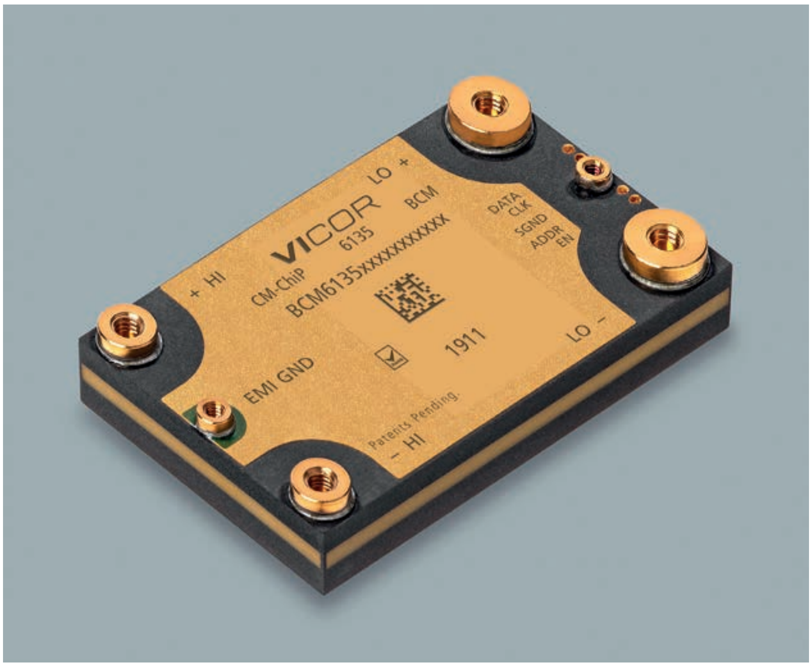
Figure 5: **MCM4609 power module for AI processor power delivery**

conventional multiphase buck regulators.

Vicor configured a SAC-topology-based module, the MCM4609 with a K-factor of 1/48, to fit within the north and south sides of the AI processor with dimensions of 46 x 9 x 3.2 mm (Figure 5). Each MCM4609 provides 325 A, or 650 A continuous in total at sub-1 V levels to the processor. The MCM4609s receive a drive signal from the MCD4609 module completing the power delivery network. The AI PDN provides unparalleled density and proximity to the processor minimizing PCB losses.

Similar to the AI processor need, when approached to develop a high-density electric vehicle (EV) battery PDN, Vicor was able to quickly configure a SAC-topology-based module to meet those needs (Figure 6). EVs require a 48 V rail to support non-motor loads within the vehicle from the primary battery in addition to requiring a chassis-mounted package. Conventional solutions to provide 48 V from the 800 V battery in an efficient and lightweight manner were limited.

Vicor therefore developed a SAC-topology-based module with a 1/16 K-factor within a larger CM-ChiP (compared to the AI MCM4609) to accommodate higher power and chassis mounting. The power module, BCM6135, provides 800 V_{IN} to 48 V_{OUT} at 80 A (or 3.8 kW of output power) conversion at over 97 % efficiency in a 61 x 35 x 7.4 mm CM-ChiP package (Figure 7). Additional power modules downstream of the BCM6135 support regulated 12 V and 48 V rails to complete the power delivery network (PDN) The high-density and high-efficiency attributes of the BCM6135 and downstream power modules enable a reduced weight and higher-performing EV battery conversion (Figure 5).



ABOVE Figure 7: **BCM6135 power module for EV battery voltage conversion**

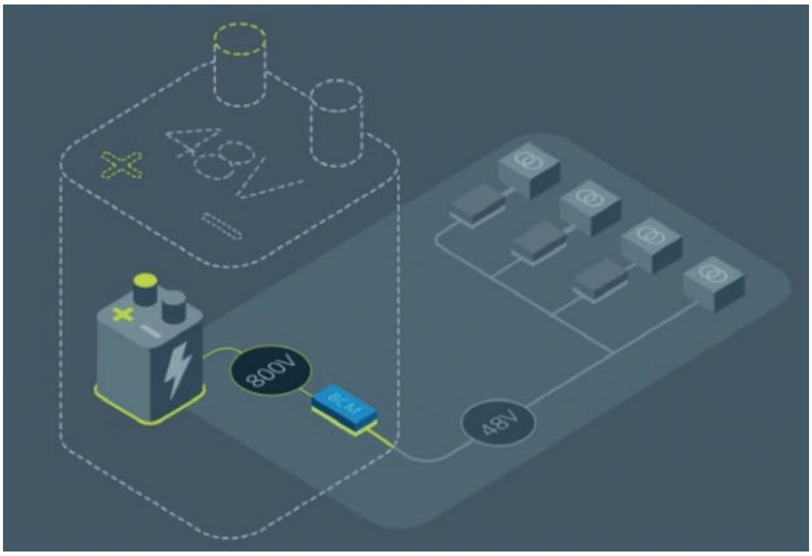


Figure 6: **Power delivery network for 800 V EV battery power conversion**

GaN in Space Applications

Gallium nitride power device technology enables a new generation of power converters in space operating at higher frequencies, higher efficiencies, and greater power densities than ever achievable before. GaN power devices can also exhibit superior radiation tolerance compared with Silicon MOSFETs depending upon their device design. **Max Zafrani, CTO, EPC Space; Alex Lidow, CEO Efficient Power Conversion, USA**

Here we discuss the capabilities of GaN devices which have been specifically designed for critical applications in the high reliability or commercial satellite space environments. Some of the failure mechanisms in GaN and how they impact radiation performance are explored. Lastly, the electrical performance of radiation hard GaN transistors is compared with the most popular radiation hardened (Rad Hard) MOSFETs in the market.

Radiation in space

There are three primary types of radiation experienced by semiconductors used in space applications. Regardless whether devices are being employed in satellites orbiting around our earth or incorporated in exploration satellites visiting the most distant parts of our solar system, all experience some form of high-energy radiation bombardment. These types of radiation are gamma radiation, neutron radiation, and heavy ion bombardment.

An energetic particle can cause damage to a semiconductor in fundamentally three ways; it can cause traps in non-conducting layers, it can cause physical damage to the crystal, also called displacement damage, or the particle can generate a cloud of electron-hole pairs that will cause the device to momentarily conduct, and possibly burn out in the process.

In eGaN devices, energetic particles cannot generate momentary short-circuit conditions because mobile hole-electron pairs cannot be generated. Thus, this article will focus on the first two failure mechanisms ? trapping and physical damage.

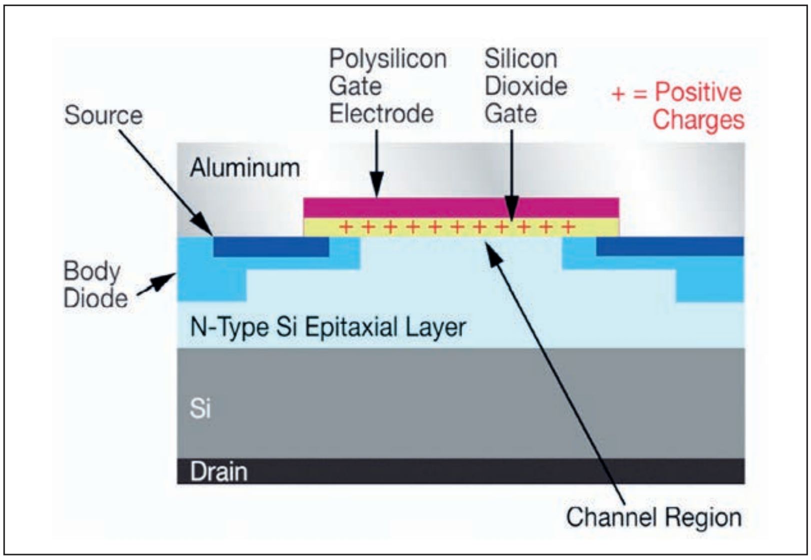
Gamma radiation in Silicon MOSFETs

Gamma radiation consists of high energy photons that interact with electrons. Figure 1(a) is a cross section of a typical Silicon MOSFET. It is a vertical device with the source and gate on the top surface and the drain on the bottom surface. The gate electrode is separated from the channel region by a thin silicon dioxide layer.

In a Silicon-based MOSFET, the gamma radiation knocks an electron out of the Silicon dioxide layer leaving behind a positively charged 'trap' in the gate oxide. The positive charge reduces the threshold voltage of the device until the transistor goes from normally off – or enhancement mode – to normally on, which is a depletion mode state. At this point the system will need a negative voltage to turn the MOSFET off. Typical ratings for rad-hard devices range from 100 kRads to 300 kRads. In some cases, devices can be made to go up to 1 MRad, but these tend to be very expensive.

Gamma radiation in enhancement mode GaN transistors

Enhancement mode GaN devices are built very differently from Silicon MOSFETs. As shown in Figure 1(b), all three terminals; gate, source, and drain, are located on the top surface. As in a



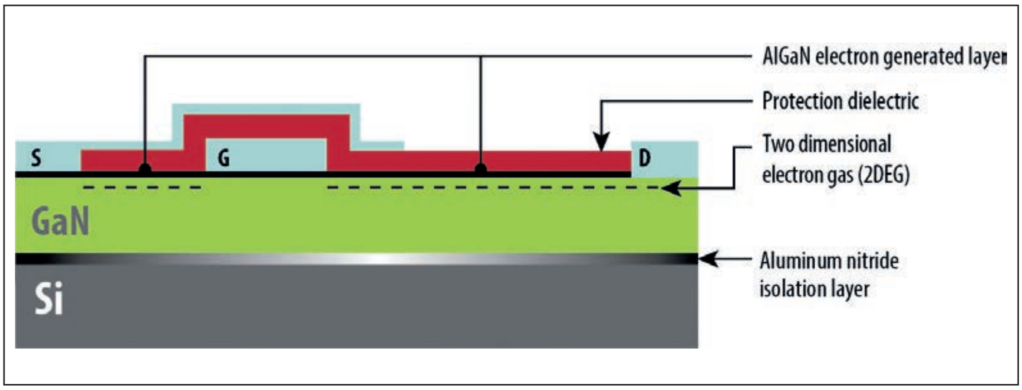


Figure 1 (above right): Cross section of a typical Silicon MOSFET (a) and cross section of a typical enhancement mode GaN (eGaN®) device (b) (right)

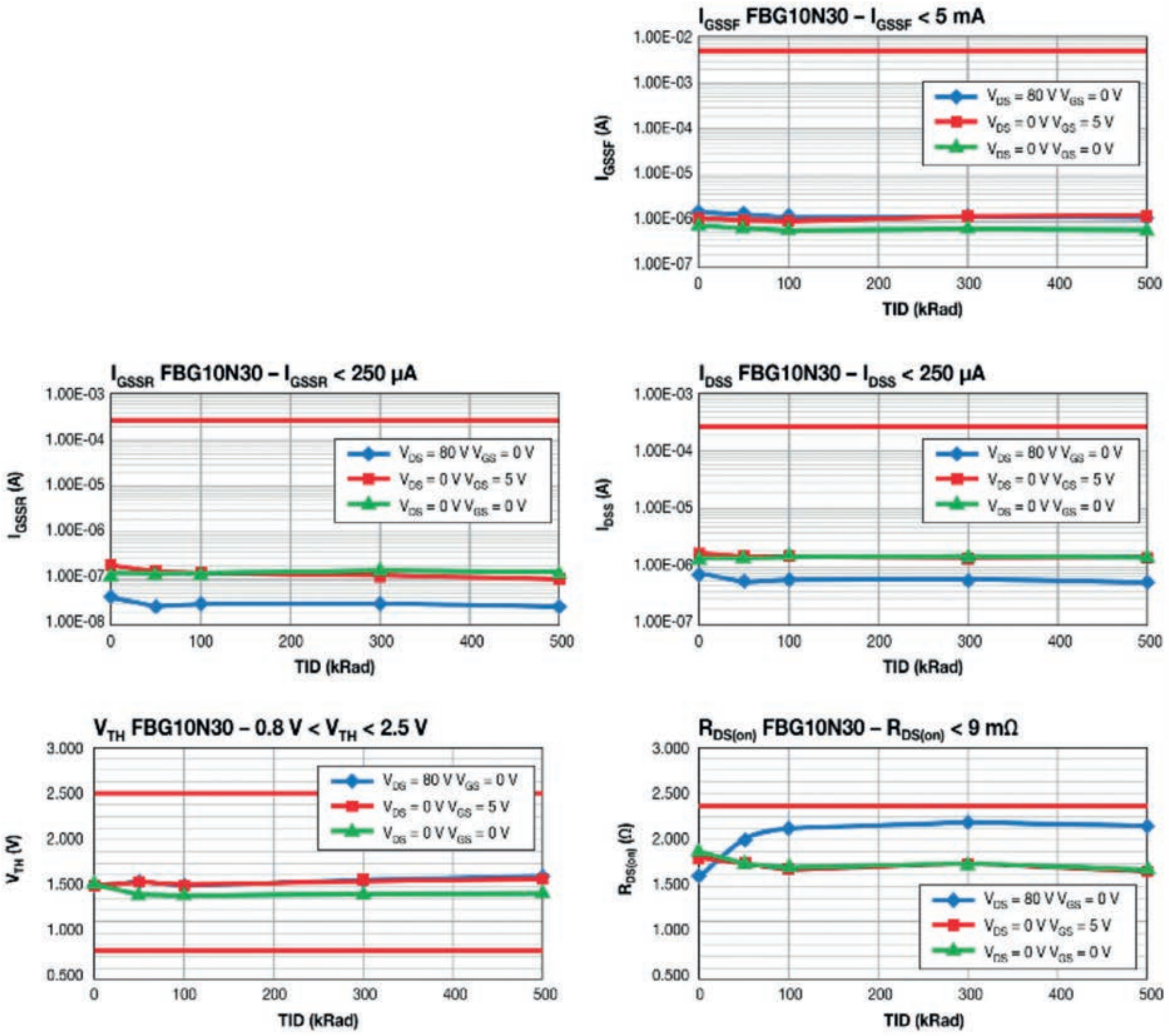


Figure 2: Results of gamma radiation testing of eGaN devices to 500 kRads

Silicon MOSFET, conduction between source and drain is modulated by biasing the gate electrode from zero volts to a positive voltage – usually 5 V. In enhancement mode GaN devices the gate is separated from the underlying channel by an aluminum gallium nitride layer. This layer does not accumulate charge when subjected to gamma radiation.

As an example of the performance of Rad Hard GaN devices, 100 V GaN-on-Si transistors were subjected to 500 kRad of gamma radiation. Throughout the testing, leakage currents from drain to source and gate to source, as well as the threshold voltage and on-resistance of the devices at various checkpoints along the way were measured, confirming that there are no significant changes in device performance. Since the initial testing, these same GaN devices have been subjected to 50 MRads, confirming that enhancement mode GaN devices built as in Figure 1(b) will not be the first part to fail due to gamma radiation in any space system. Testing results are shown in Figure 2.

Neutron radiation

The primary failure mechanism for devices under neutron bombardment is displacement damage. High energy neutrons will scatter off atoms in the crystal lattice and leave behind lattice defects. Figure 3 shows the impact of neutron radiation at doses up to 1 x 10^{15} per cm^2 impact of neutrons on the GaN crystal and the entire device structure is minimal.

The reason for GaN's superior performance under neutron radiation is that GaN has a much higher displacement threshold energy compared with Silicon. The displacement energy of a crystal is proportional to the bond strength of the crystalline elements. The bond energy between gallium and nitrogen is significantly higher than the bond energy between Silicon atoms in a Silicon power MOSFET.

Single Event Effects in Si MOSFETs

Single Event Effects (SEE) are caused by heavy ions generated by the impact of galactic cosmic rays, solar particles or energetic neutrons and protons. This can be simulated terrestrially by using a cyclotron to create beams of different ions. Two of the most common ions used to evaluate radiation tolerance of electronics components are Xenon, with a linear energy transfer (LET) of about 50 MeV·cm^2/mg, and gold, with an LET of about 85 MeV·cm^2/mg.

In a Silicon MOSFET there are two primary failure mechanisms caused by these heavy ions, single event gate rupture (SEGR) and single event burnout (SEB). SEGR is caused by the energetic atom causing such a high transient electric field across the gate oxide that the gate oxide ruptures. Whereas SEB is caused when the energetic particle transverses the drift region of the device where there are relatively high electric

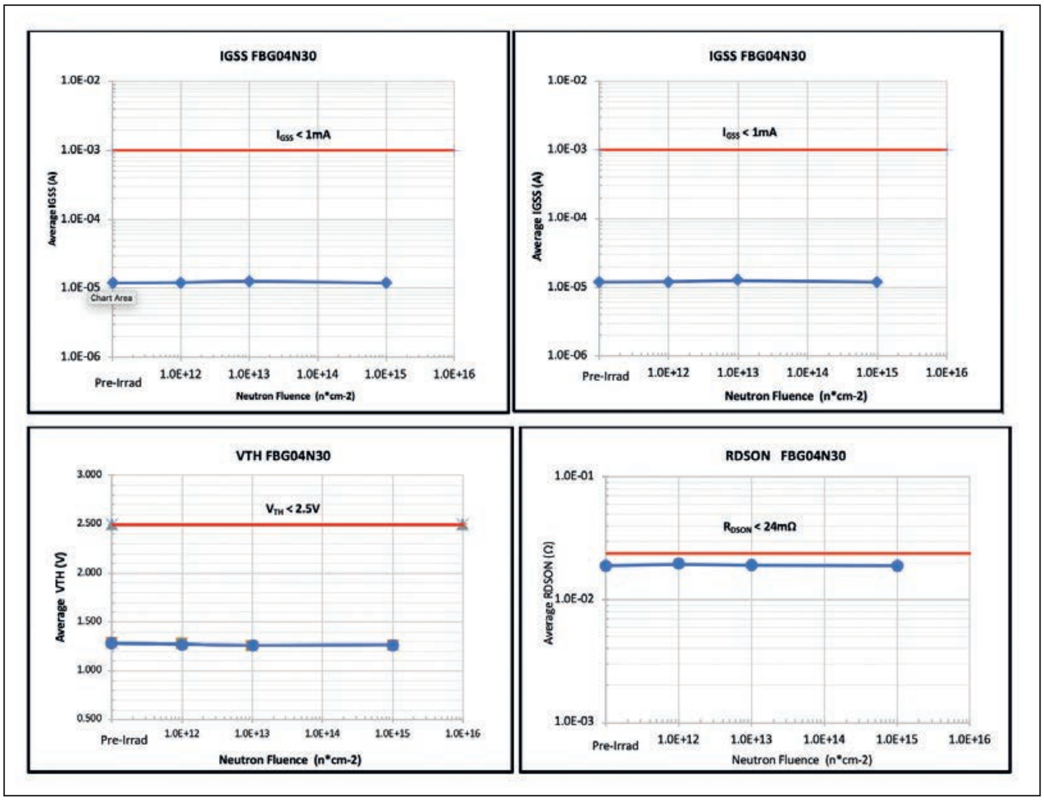


Figure 3: Impact of neutron radiation on eGaN devices at doses up to 1 x 10^{15} per cm^2

fields. The energetic particle loses its energy while generating a large number of hole electron pairs.

These hole electron pairs crossing the drift region cause the device to momentarily short circuit between drain and source. This short circuit can either destroy the device, which is a single event burnout, or the device can survive, appearing as a momentary short circuit that can cause damage to other components in the system. This latter case is call single event upset, or SEU.

Single Event in GaN devices

Since enhancement mode GaN devices built as in Figure 1 do not have a gate oxide, they are not prone to single event gate rupture. Also, since eGaN devices do not have the ability to conduct large numbers of holes very efficiently, they are not prone to single event upset.

The primary failure mechanism for enhancement mode GaN devices under heavy ion bombardment is caused by energetic particles crossing the drift region of the device where there are relatively high electric fields. The conditions are about the maximum conditions possible, with an 85 LET beam of gold atoms pummeling the device biased at the maximum data sheet limit. In testing, the gate leakage does not go up during bombardment. The drain-source leakage, however, does start to rise as the displacement damage from the heavy ions increases.

SEE Safe Operating Areas

Many specially produced enhancement mode GaN transistors have been tested for SEE under varied conditions. 40 V and 100 V product did not fail under any conditions up to full rated voltage and 87 LET. Figure 4 shows the results from several commercially available FBG20N18 200 V products and FBG30N04 300 V products. For the 200 V products, the first failures occurred at 85 LET and 190 V, as

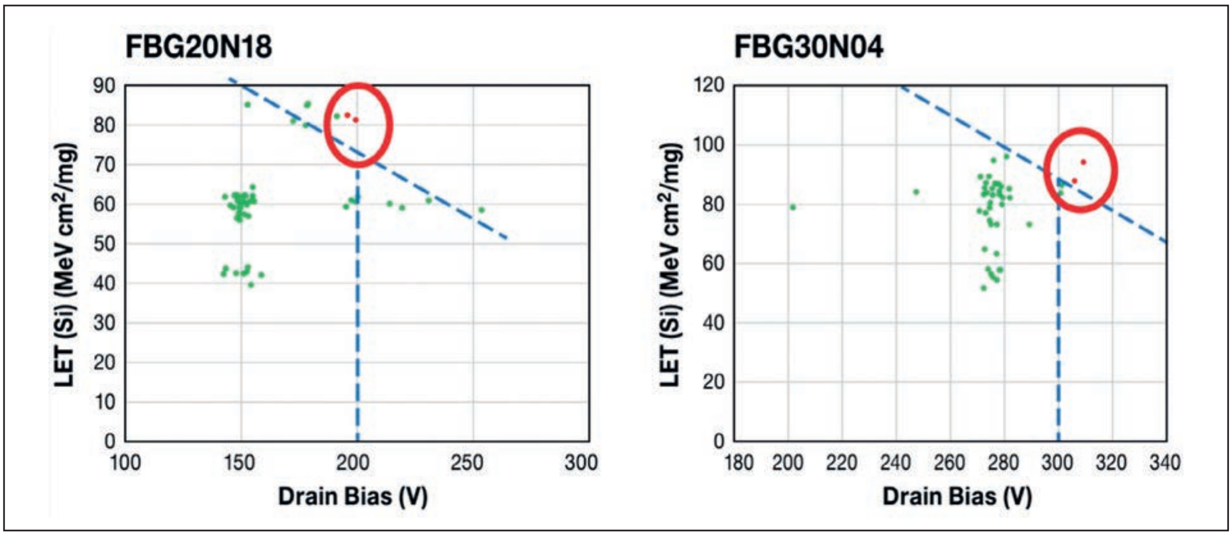
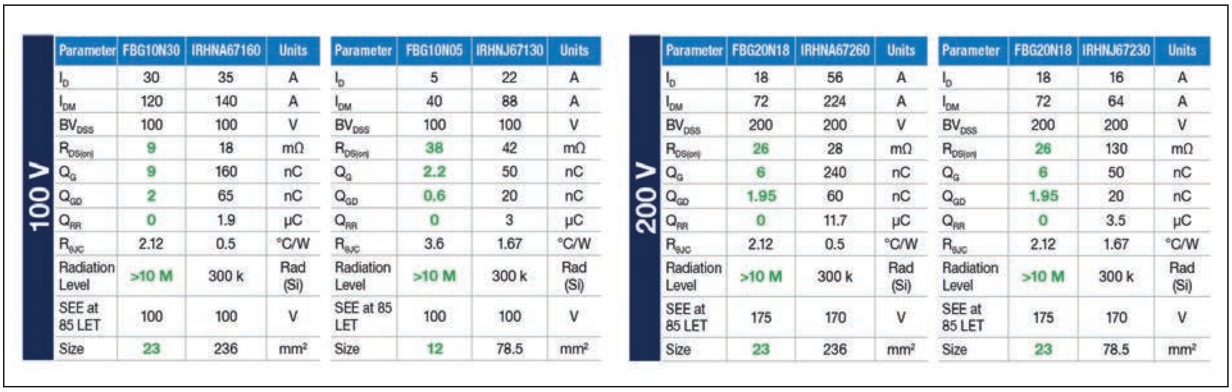


Figure 4: Results from several FBG20N18 200 V products (left) and FBG30N04 300 V products (right)



100 V

Parameter	FBG10N30	IRHNA67160	Units
I_D	30	35	A
I_{DM}	120	140	A
BV_{DSS}	100	100	V
$R_{DS(on)}$	9	18	mΩ
Q_G	9	160	nC
Q_{GD}	2	65	nC
Q_{RR}	0	1.9	µC
$R_{\theta JC}$	2.12	0.5	°C/W
Radiation Level	>10 M	300 k	Rad (Si)
SEE at 85 LET	100	100	V
Size	23	236	mm²

Parameter	FBG10N05	IRHNJ67130	Units
I_D	5	22	A
I_{DM}	40	88	A
BV_{DSS}	100	100	V
$R_{DS(on)}$	38	42	mΩ
Q_G	2.2	50	nC
Q_{GD}	0.6	20	nC
Q_{RR}	0	3	µC
$R_{\theta JC}$	3.6	1.67	°C/W
Radiation Level	>10 M	300 k	Rad (Si)
SEE at 85 LET	100	100	V
Size	12	78.5	mm²

200 V

Parameter	FBG20N18	IRHNA67260	Units
I_D	18	56	A
I_{DM}	72	224	A
BV_{DSS}	200	200	V
$R_{DS(on)}$	26	28	mΩ
Q_G	6	240	nC
Q_{GD}	1.95	60	nC
Q_{RR}	0	11.7	µC
$R_{\theta JC}$	2.12	0.5	°C/W
Radiation Level	>10 M	300 k	Rad (Si)
SEE at 85 LET	175	170	V
Size	23	236	mm²

Parameter	FBG20N18	IRHNJ67230	Units
I_D	18	16	A
I_{DM}	72	64	A
BV_{DSS}	200	200	V
$R_{DS(on)}$	26	130	mΩ
Q_G	6	50	nC
Q_{GD}	1.95	20	nC
Q_{RR}	0	3.5	µC
$R_{\theta JC}$	2.12	1.67	°C/W
Radiation Level	>10 M	300 k	Rad (Si)
SEE at 85 LET	175	170	V
Size	23	78.5	mm²

Table 1: Electrical performance comparisons of Rad Hard eGaN transistors against popular power MOSFETs

shown in the red circle on the left. The FBG30N04 300 V product failed at 85 LET and 310 V as shown in the red circle on the right.

Electrical performance comparison

In addition to the superior Rad Hard advantages of gallium nitride over Silicon, GaN has superior electrical performance as well. As an example, the electrical performance comparisons of 100 V and 200 V Rad Hard eGaN transistors against Rad Hard power MOSFETs are shown in Table 1.

The 100 V FBG10N30 packaged part has half the on-resistance compared to the Silicon MOSFET, yet is but one-tenth the size and has about one-twentieth the gate and gate-drain charges that determine switching speed. In addition, the radiation resistance is significantly higher.

At 200 V, the difference in electrical performance of the GaN transistors is even greater. Note that the GaN device listed on the left side of the 200 V section of Table 1 has similar on-resistance to its MOSFET counterpart, yet is one-tenth the size, and has about 30 times better switching performance while demonstrating superior radiation resistance.

Conclusion

In summary, GaN power transistors and ICs are the best choice for power conversion applications in spaceborne systems. Enhancement mode GaN devices have proven to be more rugged than Rad Hard MOSFETs when exposed to various forms of radiation. In addition, the electrical performance of GaN devices is many times superior to the aging Silicon power MOSFET.

Maximize Gains Using Miniaturized PoL Converters

System power requirements today are challenging, with designers needing to overcome issues such as multiple supply voltages, voltage sequencing, high transient load currents, and excessive heat. Rather than address these problems at the system power supply, it is more beneficial to introduce measures at the PCB (printed circuit board) level, meaning some form of point-of-load (PoL) converter is required.

Rolf Horn, Applications Engineer at Digi-Key Electronics EMEA

Numerous key trends have dominated the electronics industry in recent years, not least of which is the industry's shift away from centralized power systems, and even from decentralized or distributed power architectures (DPA). Instead, the latest preference is for intermediate bus architectures (IBA), where an isolated front-end DC/DC converter supplies multiple small non-isolated DC/DC converters (known as Point-of-Load/PoL converters) placed near the loads they are supplying (Figure 1).

In relation to the deployment of PoL converters, another set of trends has emerged, including the need for ever-greater performance levels, reduced costs, and system/component miniaturization. The latest electronic devices are not just faster and smarter, they are also considerably smaller, lighter, more power dense, and more efficient than previous generation products.

This factor has enormous ramifications for power supply design. In the first instance, every square millimeter of PCB real estate commands a high value, so the smaller the converter, the better. But there is another issue to consider here. PoL power supplies solve the challenge of high peak current demands and low noise margins required by high-performance semiconductors such as microcontrollers or ASICs, predominantly by being placed close to their point of use. Unfortunately, many designers end up leaving power supply considerations to the last minute due to their tight development schedules and complex boards. As a result, PCB space is frequently compromised, only leaving space for a miniaturized device.

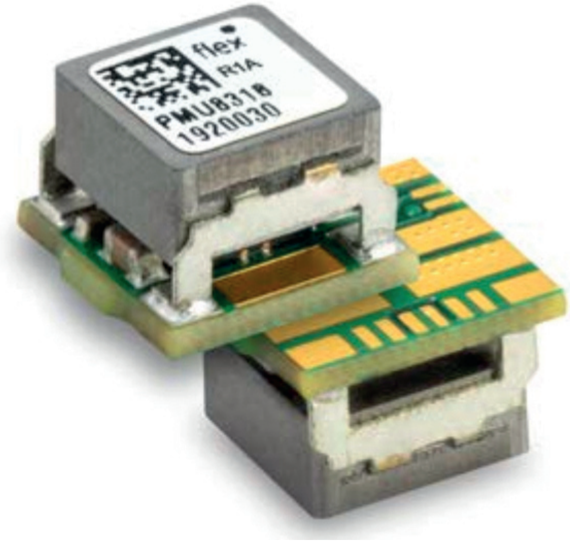


Figure 1: PoL converters such as the PMU8000 series offer an alternative to centralized power systems
Source: Flex Power Modules

Versatility for a multitude of applications

Another consideration is versatility. It is advisable to assess whether a PoL converter is suitable for both ASICs and FPGAs, for example. While most optimized PoL power supplies represent simple analog (not digital) solutions, the capability to serve FPGAs is important as they are gaining popularity among designers for a multitude of applications.

FPGAs offer many advantages over custom-designed ASICs, including lower cost, a wide range of sizes, and the potential to reconfigure circuits. However, although these benefits are highly appealing to design engineers, there is a problem. Each FPGA will require multiple DC voltage supplies. Often four, six or more DC rails will be needed, some at relatively high currents for the core, but many at much lower currents. Which is why diligent PoL converter selection is critical, especially as the latest high-density FPGAs (and ASICs) are becoming more sophisticated and demanding. In simple terms, performance, efficiency, quality and flexibility cannot be sacrificed in the name of miniaturization.

Yet with PCB real estate at a premium, there is no overlooking the importance of size. A key point is that small PoL converters are often low-profile and light enough to be used on the underside of a PCB, saving more space and increasing design flexibility. Compare this space saving concept to larger/heavier/taller PoL power supplies or individual isolated converters which can only be mounted on one side of the board, and the benefit is clear.

In addition, miniature PoL converters can be placed far closer to their loads, again presenting a number of key advantages. By way of example, DC/DC distribution losses will be minimized, while noise sensitivity and EMI emissions issues will be overcome. Furthermore, stray inductances can be reduced, enabling a quicker response to transients.

Deploying multiple PoL converters will also make it far easier to provide the various voltage supplies typically demanded by high-specification components on today's PCBs.

A further area that requires scrutiny is thermal performance. As power components become smaller and more densely packed, the potential for higher heat transfer is more prevalent. However, it is well established that power dissipation, and hence heat, must be kept to a minimum, to avoid temperature rises and potential unreliability, as well as the extra cost of removing any excess heat. The best advice, therefore, is to give the PoL converter's datasheet a detailed read, especially when checking the thermal performance and efficiency data. The information related to thermal performance is often provided as a 'derating curve', depicting how the maximum output of a converter depends on ambient temperature and cooling conditions (Figure 2).

The product's efficiency data is also found in a corresponding 'efficiency curve' in the data sheet and must be given a thorough review (Figure 3).

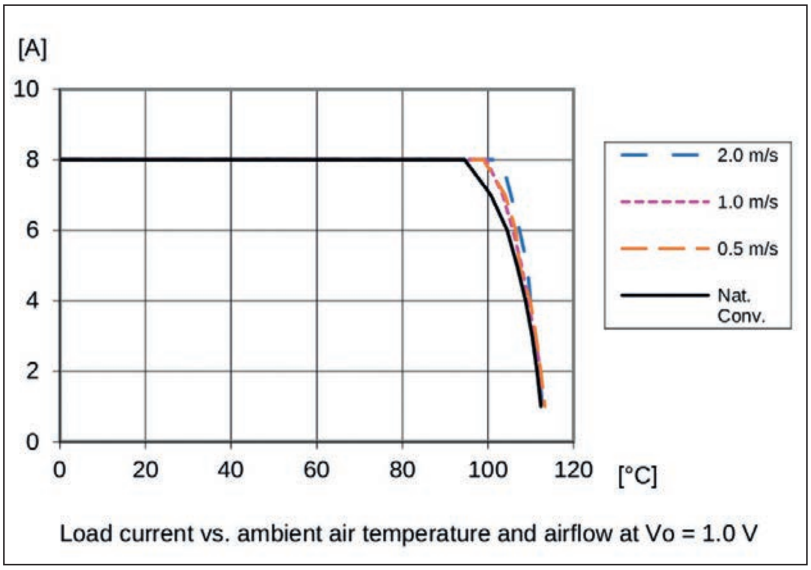


Figure 2: The PMU8418 product's (4.5-17 VIN, IOUT set point, 8 A) output current derating curve shows that current remains stable at 8 A with no airflow until the temperature value of +105°C is reached. **Source: Flex Power Modules**

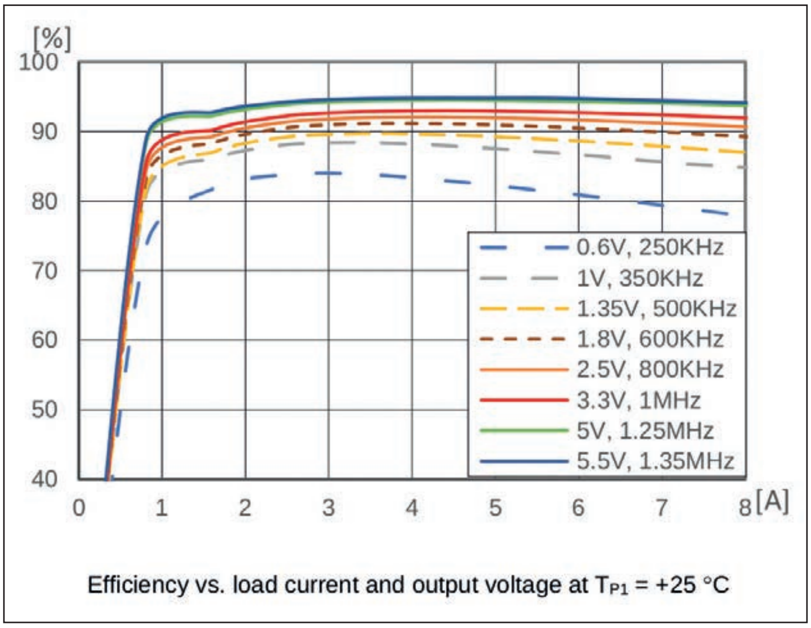


Figure 3: The efficiency curve must also be considered when choosing a POL. Shown here is the typical efficiency characteristics of the PMU8418 product (4.5-17 VIN, multiple VOUT and switching frequency levels shown, 8 A max) **Source: Flex Power Modules**

It is also recommended that system designers seek out additional functionality that can potentially increase performance. For instance, some regulators include a loop optimization feature that enables engineers to optimize their transient response for different capacitive loads, thus increasing flexibility in system design. Certain PoL solutions also provide a configurable soft start or tracking feature, which makes time sequence design easier and more flexible.

Miniature PoL converters such as the PMU8000 which are packaged in a standardized form factor in the market, can be applied on the top or bottom side of the board, making them a highly flexible solution for design engineers. One footprint covers current levels of 4 A, 6 A, and 8 A, which provides even more flexibility to system designers aiming to optimize power design. Moreover, the modules can also function in high temperatures (up to 105°C) and harsh environmental conditions. Here, the robust design means that the mean time between failure (MTBF) is specified at 171 Mhrs. The PoL regulators from Flex Power Modules are suited to a wide range of power conversion applications, including FPGAs, ASICs, network processors, CPUs and GPUs, across sectors such as ICT (telecom and datacom), industrial, test and measurement, IoT, railway, and medical.

Conclusion

In summary, miniature DC/DC converters are suitable for a wide range of applications on boards where space is at a premium. Such regulators are compact and cost-effective, and provide many generic project benefits, such as shorter development cycles, easier qualification efforts, design placement flexibility, higher quality levels, and development cost savings. To meet the ongoing demand for miniaturized PoL regulators, Flex Power Modules sells its compact product family through Digi-Key, which provides an excellent price/performance ratio in a small, low-profile, feature rich package. Efficiency is high at typically 95.3 %, while thermal performance is also exceptional, in part because the LGA design allows heat to be transferred down to the host PCB.

Flying Capacitor Topology for Ultra Efficient Inverter Applications

High efficiency and reduced effort for filtering are the main arguments for three-level (3L) topologies. Actually, there are several 3L topologies used in solar applications. The limitation of all Neutral Point Clamped (NPC) three-level topologies is the fact that a 150 Hz ripple has to be filtered with DC capacitors, which are independent on the frequency of the Pulse With Modulation (PWM). With high frequency and utilization of SiC semiconductors it is possible to reduce the size of the output filter, but, however, the DC-capacitors are still required as the same size. There is an alternative Flying-Capacitor (FC) concept in which the 150 Hz ripple is not present. The basic principle of three-level (3L) and four-level (4L) inverter concept is introduced here. **Michael Frisch, Director Product Marketing; Erno Temesi, Chief Engineer; Vincotech Germany and Hungary**

The Neutral Point Clamped (NPC) inverters are widely used in highly efficient solar, UPS and other power electronics applications. This topology (Figure 1) provides advantages in switching losses in a reduced size of the inductor. However, there is one disadvantage to be named, which is the voltage ripple of 3x line frequency (e.g. 3 x 50 Hz => 150 Hz) in the DC bus. This results in an additional effort for DC capacitors to filter the ripple.

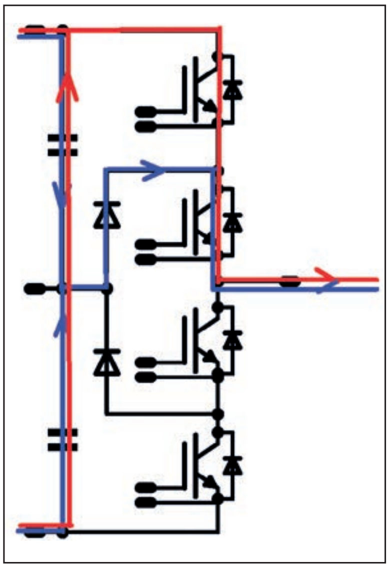


Figure 1: **NCP inverter topology**

DC voltage ripple at NPC inverters

In symmetrical loaded three-phase systems the power is constant.
$P = P_1 + P_2 + P_3$ ($P_{1,2,3}$ = power of the three power lines)
$P(t) = V_{(peak)} * I_{(peak)} * \sin^2(\omega t)$
The lines are shifted with $2\pi/3$.

The total power is:
$P_{tot} = V_{(peak)} * I_{(peak)} * [\sin^2(\omega t) + \sin^2(\omega t+2\pi/3) + \sin^2(\omega t+4\pi/3)] = 1.5 * V_{(peak)} * I_{(peak)} = \text{constant}$

This is also valid for NPC. The problem is that NPC uses a third level which has to be built up by capacitors, and the charge-discharge cycle is only balanced after one sine wave of the grid frequency or 1/3 of a sine wave in the three-phase system. This leads to a ripple with 3x line frequency of usually 150 Hz.

Principle of FC inverters

Compared to NPC inverters, there is no additional external voltage level than DC voltage required, the additional level is generated in the circuit itself. The basic topology is shown in Figure 2. The capacitors are charged in order to provide the voltage for the three levels:

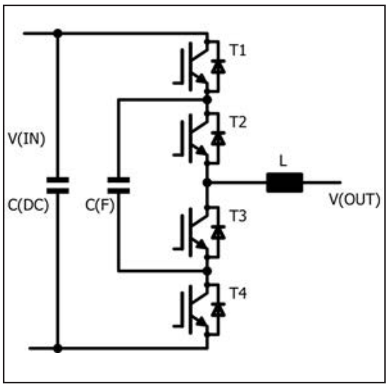


Figure 2: **Topology of 3L FC Inverter**

1. V(DC+):	Vdc
2. V(FC):	1/2x Vdc
3. V(DC+):	0 V

In case of 1200 VDC voltage C(F) is charged with 600V C(F1)).

The three levels are: V(DC+) = 1200 V, V(FC) = 600 V, V(DC-) = 0 V. The switching sequence is controlled in a way that the FCs are kept on the same voltage. The capacitor is charged and discharged within the defined voltage limits in the operation.

Excitation in Level 1 and freewheeling in Level 2: During the excitation the upper switches T1, T2 are turned on. For the freewheeling one of the two switches is turned off. For a balanced system the switches are alternating. In every freewheeling cycle a different switch is turned off.

The switching frequency in the switches is only half of the frequency at the inductor. This leads to identical load and losses in all switches. The optimum for all switches regarding static losses and switching losses is the same. This is also valid in reactive power and reverse power direction.

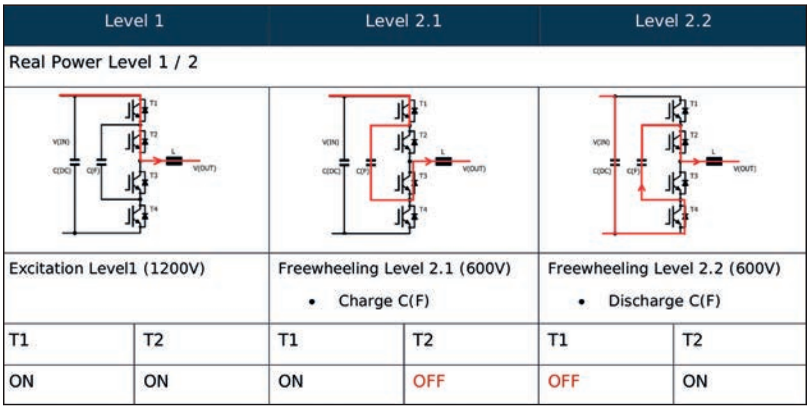
The switching sequence of a 3L FC inverter and charging / discharging status of the FC is shown in Tables 1/2.

Every first freewheeling cycle is charging and every second is discharging the FC. The capacitor is in average at the same voltage. In long term the asymmetry in the circuit might cause an imbalance of the capacitor voltage. The target voltage is 1/2 of the DC voltage.

Here is a simple logic for balancing - the target voltage of the FC is half of the DC voltage:

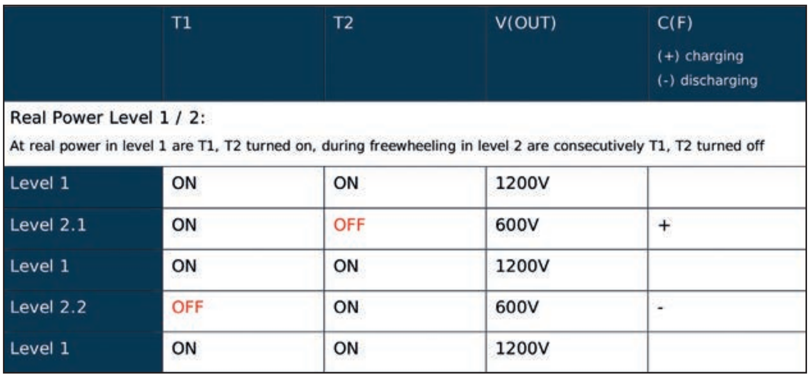
- If V(FC) < 1/2x V(DC) => charge FC, use Level 2.1 for freewheeling => turn off T2
- If V(FC) > 1/2x V(DC) => discharge FC, use Level 2.2 for freewheeling => turn off T1

It is also possible to use the same PWM



Level 1		Level 2.1		Level 2.2	
Real Power Level 1 / 2					
Excitation Level1 (1200V)		Freewheeling Level 2.1 (600V) • Charge C(F)		Freewheeling Level 2.2 (600V) • Discharge C(F)	
T1	T2	T1	T2	T1	T2
ON	ON	ON	OFF	OFF	ON

Table 1: The switching sequence of a 3L FC inverter



	T1	T2	V(OUT)	C(F) (+) charging (-) discharging
Real Power Level 1 / 2: At real power in level 1 are T1, T2 turned on, during freewheeling in level 2 are consecutively T1, T2 turned off				
Level 1	ON	ON	1200V	
Level 2.1	ON	OFF	600V	+
Level 1	ON	ON	1200V	
Level 2.2	OFF	ON	600V	-
Level 1	ON	ON	1200V	

Table 2: Switching sequence of a 3L FC inverter and charging / discharging status of the FC7

sequence as for a standard NPC inverter and just assign the turn-off signal to the right switch according to this logic.

For the balancing the charging status of the FC is required. The following information is needed for a proper controlling of the voltage in the FC:

- V(FC) < 1/2x V(DC)
- V(FC) > 1/2x V(DC)

This is possible without an expensive isolation amplifier. In Figure 3 it is shown that with a voltage divider and a differential amplifier it is possible to compare the voltage of the DC capacitor and the FC, and to provide the data if the voltage in the FC is above or below the target. A simple optocoupler is able to send the information to the microcontroller.

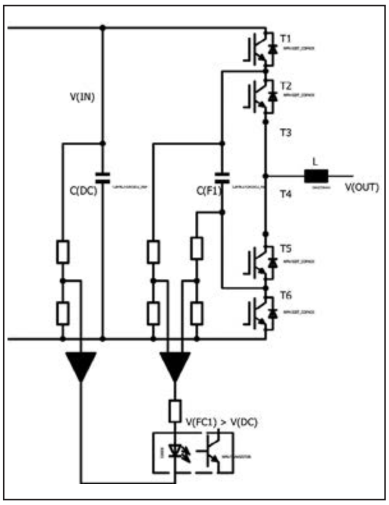


Figure 3: Voltage detection in 3L FC inverter

Principle of 4L FC inverters

Here the four-level Flying-capacitors are further discussed. The basic topology is shown in Figure 4.

The capacitors are charged in order to provide the voltage for the four levels:

1. V(DC+): Vdc
2. V(FC1): 2/3x Vdc
3. V(FC2): 1/3x Vdc
4. V(DC-): 0V

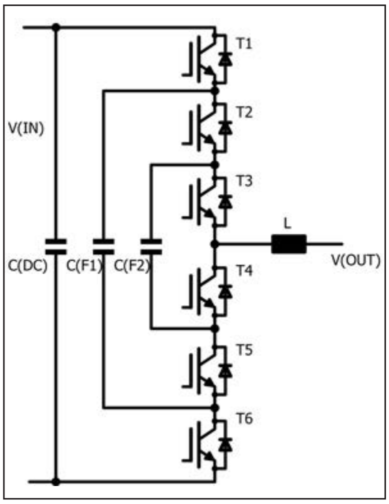


Figure 4: Topology of 4L FC inverter

In case of 1200V DC voltage, the capacitors are charged with 800 V C(F1) and 400 V C(F2).

The four levels are: V(DC+) = 1200 V, V(FC1) = 800 V, V(FC2) = 400 V, V(DC-) = 0V.

The switching sequence is controlled in a way that the FCs are kept on the same voltage. The capacitors are charged and discharged within the defined voltage limits in the operation.

At real mode, in the positive half-wave there are two different sections of switching, the sinusoidal grid voltage $V_{(t)} >$ 1/3x VDC and $V_{(t)} <$ 1/3x VDC:

1. $V_{(t)} >$ 1/3x VDC:

Excitation in level 1 and freewheeling in level 2. During the excitation the upper switches T1, T2, T3 are turned on. For freewheeling one of the three switches is turned off. For a balanced system in every freewheeling cycle a different switch is turned off.

2. V(t) < 1/3x VDC:

Excitation in Level 2 and freewheeling in Level 3. During the excitation two of the three upper switches are turned on. For freewheeling only one. To avoid additional switching losses we have the additional frame condition to change the switching status only for one switch at one time. The result is that the PWM frequency is reduced to 1/3 per switch, but all three switches are involved (Figures 5/6).

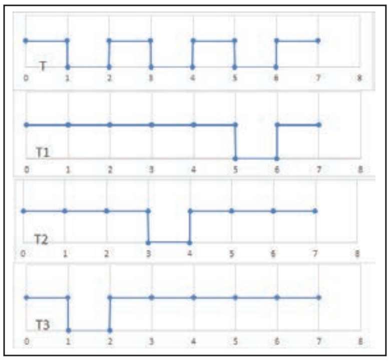


Figure 5: FC gate signal level 1, 2

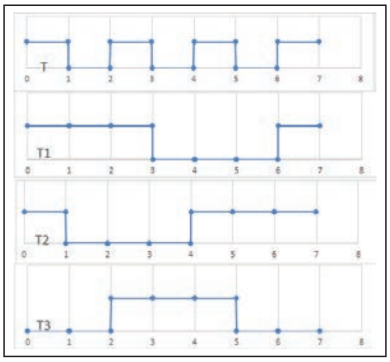
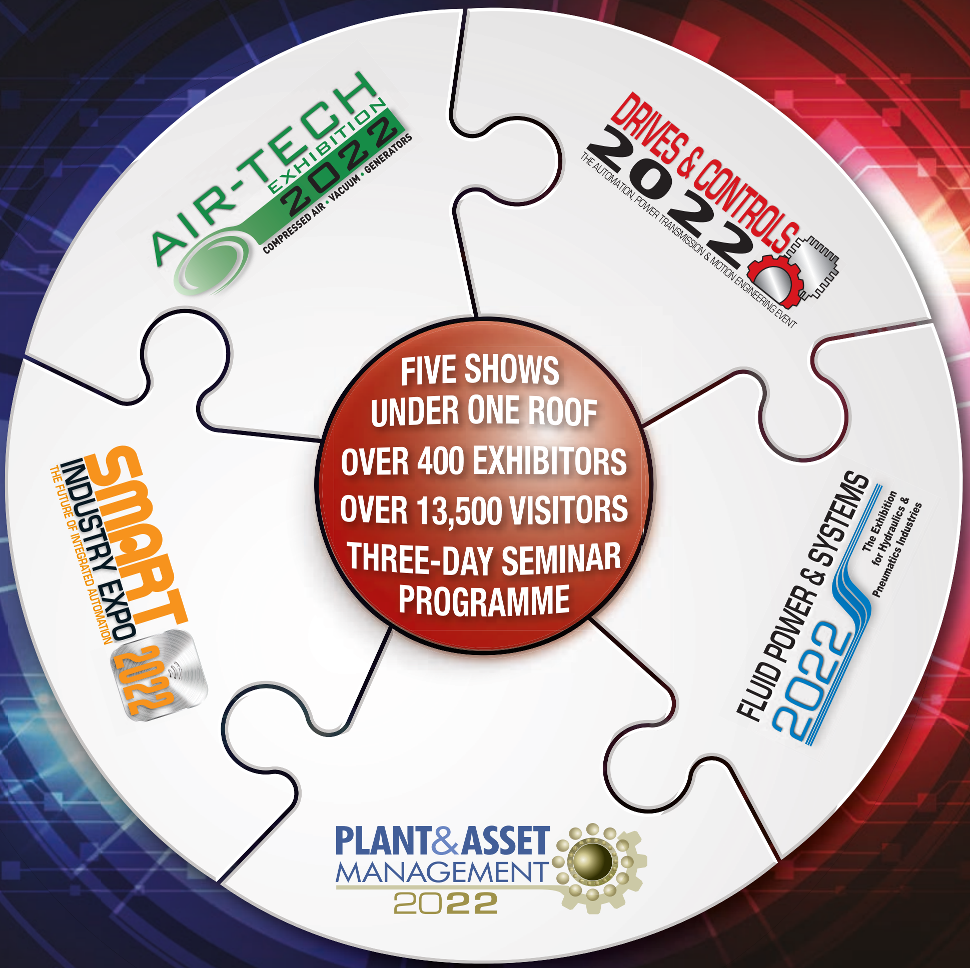


Figure 6: FC gate signal level 2, 3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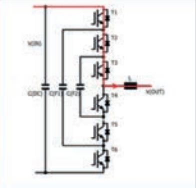
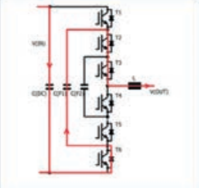
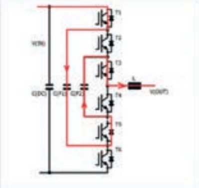
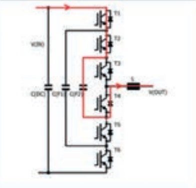
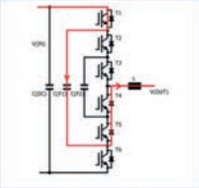
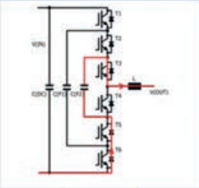
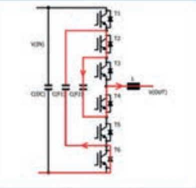
Level 1			Level 2.1			Level 2.2			Level 2.3		
Real Power Level 1 / 2											
											
Level1 (1200V)			Freewheeling Level 2 (800V) • Discharge C(F1)			Freewheeling Level 2 (800V) • Charge C(F1) • Discharge C(F2)			Freewheeling Level 2 (800V) • Charge C(F2)		
T1	T2	T3	T1	T2	T3	T1	T2	T3	T1	T2	T3
ON	ON	ON	OFF	ON	ON	ON	OFF	ON	ON	ON	OFF
			Level 3.1			Level 3.2			Level 3.3		
											
			T1	T2	T3	T1	T2	T3	T1	T2	T3
			ON	OFF	OFF	OFF	OFF	ON	OFF	ON	OFF

Table 3: **Operation of 4L FC inverter at real power**

	T1	T2	T3	V(OUT)	C(F1) (+) charging (-) dis-charging	C(F2) (+) charging (-) dis-charging
Real Power Level 1 / 2: At real power in Level 1: T1, T2, T3 are turned on, during freewheeling in Level 2 consecutively T1, T2, T3 are turned off						
Level 1	ON	ON	ON	1200V		
Level 2.1	OFF	ON	ON	800V	-	
Level 1	ON	ON	ON	1200V		
Level 2.2	ON	OFF	ON	800V	+	-
Level 1	ON	ON	ON	1200V		
Level 2.3	ON	ON	OFF	800V		+
Real Power Level 2 / 3: At real power in Level 2: 2 switches (out of T1, T2, T3) are turned on, during freewheeling in Level 3 remains only one (out of T1, T2, T3) turned on.						
Level 2.3	ON	ON	OFF	800V		+
Level 3.1	ON	OFF	OFF	400V	+	
Level 2.2	ON	OFF	ON	800V	+	-
Level 3.2	OFF	OFF	ON	400V		-
Level 2.1	OFF	ON	ON	800V	-	
Level 3.3	OFF	ON	OFF	400V	-	+

Table 4: **4L FC inverter switching sequence**

The switching frequency in the switches is only one third of the frequency at the inductor. This leads to identical load and losses in all switches. The optimum for all switches regarding static losses and switching losses is the same. This is also valid in reactive power and reverse power direction. Operation at real power (positive half-wave) is shown in Tables 3/4.

In a sequence of three times excitation and freewheeling there are one (Level 1-2 / 4-3) or two (Level 2-3) cycles of charging / discharging the FC capacitors. Charging and discharging of the FC is compensating each other, so that the voltage of the FC will stay within the functional limits (e.g. +/- 10 % of the DC voltage). In the long run the tolerances will lead to some imbalance in the FC´s and have to be compensated.

Here is a simple logic for balancing - the target voltage of the FC is:

$V(F1) = 2/3x\ V(DC); X1 = V(F1)actual / V(F1)target$

$V(F2) = 1/3x\ V(DC); X2 = V(F2)actual / V(F2)target$

There are the following possible situations:

- X1>1, X2>1 => discharge FC1, FC2
- X1<1, X2>1 => charge FC1, discharge FC2
- X1>1, X2<1 => discharge FC1, charge FC2
- X1<1, X2<1 => charge FC1, FC2

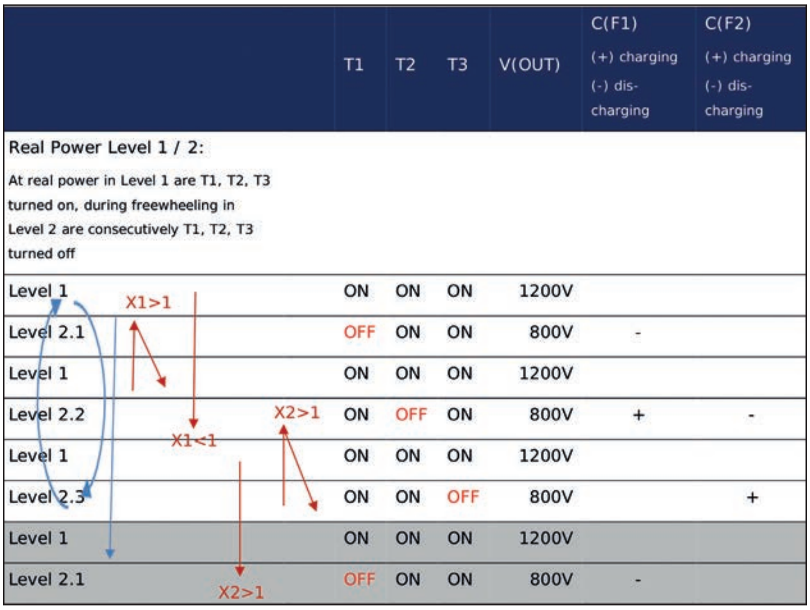
The circuit switches between Level 1 and the three different Level 2 options. During Level 1 it has to be decided which option will be taken - example:

- X1>1 => discharge FC1 (repeat level 1 / level 2.1)
- X1<1 => avoid discharge FC1 (skip level 2.1)
- X2>1 => avoid charge FC2 (skip level 2.3)
- X2<1 => charge FC2 (repeat level 1 / level 2.3)

The balancing at Level 2-3 is more complicated, because there are three different options for Level 2, and three different options for Level 3. Another frame condition is that only one switch is changing its state during one switching cycle. The goal is now to add a charge or discharge cycle for one capacitor without changing the voltage of the second capacitor. This is possible, if a short sequence is repeated where the targeted capacitor is getting the additional cycle (charge or discharge) but the other capacitor is getting the same cycles for both (charge/discharge).

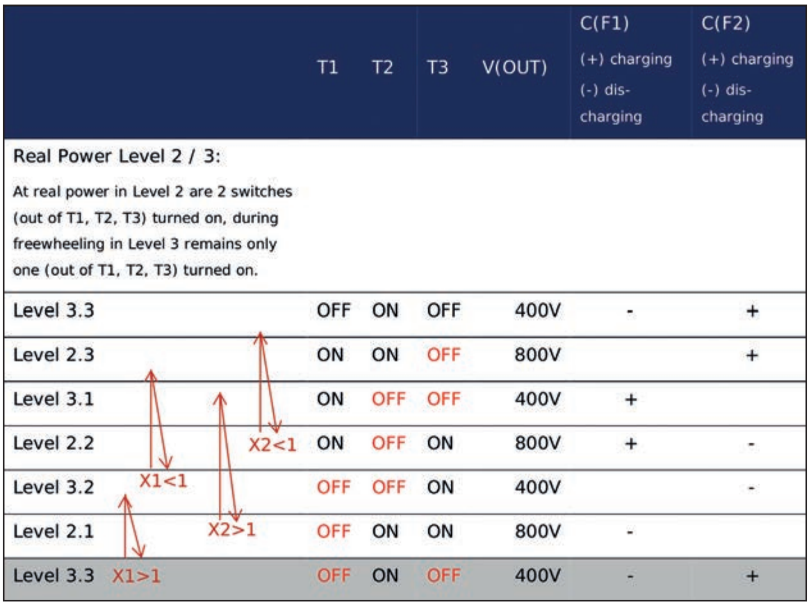
Example:

- X1>1 => discharge FC1 (level 3.3=>2.1=>3.2=>2.1=>3.3…)
- X1<1 => charge FC1 (level 2.2=>3.1=>2.3=>3.1=>2.2…)
- X2>1 => discharge FC2 (level 3.2=>2.2=>3.1=>2.2=>3.2…)
- X2<1 => charge FC2 (level 3.1=>2.3=>3.3=>2.3=>3.1…)



	T1	T2	T3	V(OUT)	C(F1) (+) charging (-) dis-charging	C(F2) (+) charging (-) dis-charging
Real Power Level 1 / 2: At real power in Level 1 are T1, T2, T3 turned on, during freewheeling in Level 2 are consecutively T1, T2, T3 turned off						
Level 1	ON	ON	ON	1200V		
Level 2.1	OFF	ON	ON	800V	-	
Level 1	ON	ON	ON	1200V		
Level 2.2	ON	OFF	ON	800V	+	-
Level 1	ON	ON	ON	1200V		
Level 2.3	ON	ON	OFF	800V		+
Level 1	ON	ON	ON	1200V		
Level 2.1	OFF	ON	ON	800V	-	

Table 5: **Levels 1-2.3**



	T1	T2	T3	V(OUT)	C(F1) (+) charging (-) dis-charging	C(F2) (+) charging (-) dis-charging
Real Power Level 2 / 3: At real power in Level 2 are 2 switches (out of T1, T2, T3) turned on, during freewheeling in Level 3 remains only one (out of T1, T2, T3) turned on.						
Level 3.3	OFF	ON	OFF	400V	-	+
Level 2.3	ON	ON	OFF	800V		+
Level 3.1	ON	OFF	OFF	400V	+	
Level 2.2	ON	OFF	ON	800V	+	-
Level 3.2	OFF	OFF	ON	400V		-
Level 2.1	OFF	ON	ON	800V	-	
Level 3.3	OFF	ON	OFF	400V	-	+

Table 6: **Levels 2.1 – 3.3**

It is now possible to change the switching sequence in order to compensate the imbalance with this input. Every switching sequence has the actual condition of X1 and X2 and an expected result after execution of the next switching cycle. If the expected result is not achieved, the cycle will be repeated one time. The signal at the output filter is not affected, it is the same as without the additional balancing sequence (see Tables 5/6).

Voltage measurement in the 4L FC

Analog voltage measurement requires additional effort in isolated measurement. Fortunately, only the ratio between the DC voltages (VFC1= 2/3x VDC and VFC2=1/3x VDC) is required, or if the voltage is fixed, it would be enough to detect if the voltage in the FC is above or below a fixed target voltage.

Figure 7 shows a proposal for a detection of the target voltage ratio.

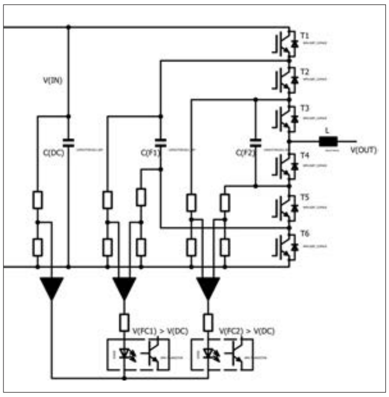


Figure 7: **4L FC inverter, capacitor voltage detection**

The FC has to be pre-charged to avoid over-voltage in the switches at the start up. With this circuit (see Figure 8) a simple pre-charging is achieved with a resistor divider circuit. The resistor values have to be calculated as follows:

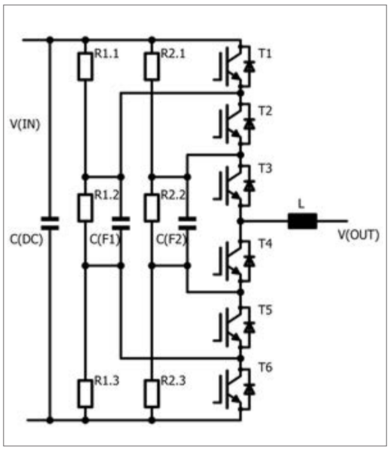


Figure 8: **Pre-Charge circuit for FC inverter**

1. R1.2 = 4x R1.1; R1.1 = R1.3
2. R2.1 = R2.2 = R2.3

The result is: V(F1) = 2/3 * V(DC) and V(F2) = 1/3 * V(DC)

Conclusions

The special features of FC inverters are:
* No requirement to provide additional external voltage levels, the switching level
- No presence of low frequency ripple (150 Hz)
- Inductor frequency is 2x (3L) 3x (4L) switching frequency of the individual switches
- All switches are loaded identical during one output sine wave
- The balancing of the FC voltage is possible with low effort in the circuit design and cost (voltage detection and switching sequence)

The utilization of the listed features open opportunities for high efficient FC inverter ideas.

Literature

Thierry Meynard, Henri Foch, "Electronic device for electrical energy conversion between a voltage source and a current source by means of controllable switching cells" US Patent: US5737201A, Apr. 7, 1998

A. Ruderman, B. Reznikov, "Simple Analysis of a Flying Capacitor Converter Voltage Balance Dynamics for DC Modulation" EPE/PEMC 2008, Aachen, Germany

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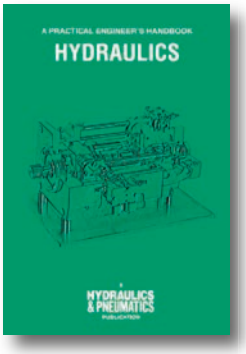

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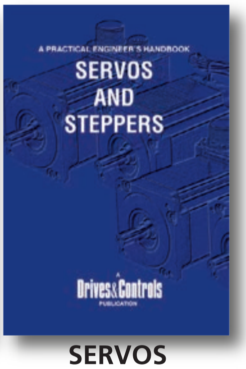

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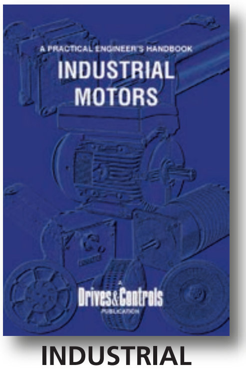

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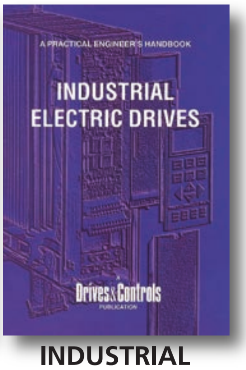

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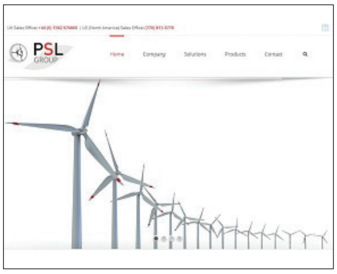

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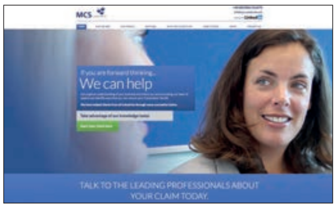

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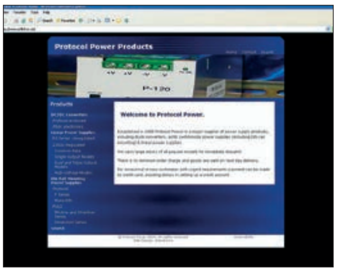

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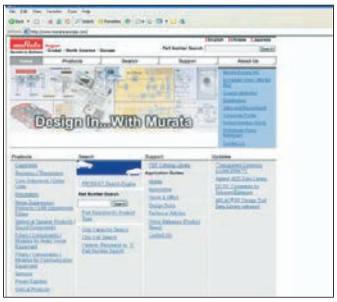

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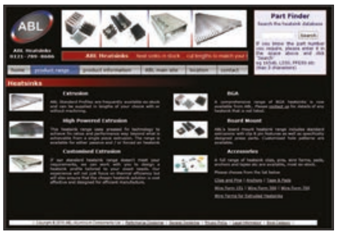

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