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HIGH-POWER SEMICONDUCTORS

Third Generation Press-Pack IGBTs and Diodes for Megawatt Applications

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COVER STORY

Third Generation Press-Pack IGBTs and Diodes for Megawatt Applications

Press-pack IGBT technology has come of age with the introduction of the latest generation of soft punch through die. First introduced twelve years ago, as a high reliability solution for hostile environments, the press-pack IGBT has evolved towards the product of choice in many high power applications. The first European made devices were targeted at induction heating power supplies, a 1.8kV medium frequency device, offered as a solution to overcome the punishing thermal stress of such applications. These new introductions were both expensive to produce and very application specific. However, the robust nature of the design attracted wider appeal and new products were introduced with higher voltage and less application specific characteristics. Background to the evolution of the new generation and its enhanced characteristics are introduced for the largest member of the product family. With high reliability and low losses, the new device is ideal for today's demanding environment of high efficiency and renewable energy sources. Full story on page 14

Cover supplied by Westcode/Ixys

The Power of Renewable Energy Applications

Europe, which has traditionally been the world's largest market for wind energy development, continued to see strong growth in 2009, also exceeding expectations. According to the Global Wind Energy Council, more wind power was installed than any other power technology, accounting for 39% of the total new generation capacity. Taken together, renewable energy technologies accounted for 61% of new power generating capacity in 2009.10.5GW were installed in Europe last year, including 582MW offshore, taking the total wind power capacity up to 76.2GW. While the traditional wind markets in Germany and Spain continue to drive investment, other 'second wave' countries are now firmly established, with new capacity additions of over 1,000MW in 2009 in Italy, France and the UK. Eleven out of the EU's 25 member states now have more than 1GW of wind power capacity. Investment in new European wind farms in 2009 reached €13 billion, including €1.5 billion offshore. The wind capacity installed by the end of 2009 will in a normal year produce 163TWh of electricity, meeting 4.8% of total EU power demand.

Germany continues to lead Europe, adding 1.9GW in 2009 for a total capacity of nearly 26MW. 38TWh of wind-generated electricity was generated in Germany in 2009, in a wind year that was below average, accounting for about 7% of the country's total power consumption. The German wind power sector now employs around 100,000 people. Spain led the European league tables for new installed capacity, with additions of 2.5GW of wind power, bringing its total up to 19GW. Wind energy now represents Spain's third largest power generation source with a production of 36TWh in 2009, covering 14.5% of the country's electricity demand, compared to 11.5% in 2008. Italy, France and the UK all continued to show strong growth and added 1.1GW each to their wind power capacity.

Until 2013, Europe will continue to host the largest wind capacity. However, GWEC expects that by the end of 2014, Europe's installed capacity will stand at 136GW, compared to Asia's 150GW. By 2014, the annual market will reach 15GW, and a total of 60GW will be installed in Europe over this period.

At the end of 2009, the China Meteorological Administration published a new wind assessment, which shows that China has a potential to develop 2,380GW of class 3 wind power and 1,130GW for class 4, while the offshore potential reaches 200GW for class 3. The planning and development for this 'Wind Base' programme, which aims to build 128GW of wind capacity in six Chinese provinces, is well underway, and construction has started on some projects. The programme will be key to reaching the Chinese government's National Mid and Long-Term Development Plan of 3% non-hydro renewable electricity production by 2020. The breathtaking growth of the Chinese wind energy industry has been driven primarily by national renewable energy policies. An amendment to China's Renewable Energy Law was introduced in 2009, reiterating priority grid access for wind farms, a stipulation which had previously not been enforced. In addition, the new amendment requires grid operators to purchase a certain fixed amount of renewable energy, and penalties for non-compliance are foreseen. The Chinese government has been very successful in fostering a domestic turbine manufacturing industry through a variety of measures, including a local content requirement, by sharing the burden of the extra costs related to wind power across all the provinces, and by setting a mandatory renewable energy market share for the big utilities. All these factors have driven the wind market to develop rapidly and to stimulate the wind manufacturing business. By the end of 2009, there were almost 80 wind turbine manufacturers, 30 of which had actually already sold wind turbines. Goldwind is one of the first enterprises in China focusing on research and manufacturing solutions for wind turbines. Since 2000, Goldwind has had an average annual growth of 100% for the last ten consecutive years. Goldwind was one of the top five global suppliers of wind power generators with a market share of 7.2% of the newly installed wind power capacity in 2009.

The Chinese wind power market is vital for European power semiconductor vendors, i. e. Goldwind recently signed a sales contract directly with Semikron China thereby ensuring the continued supply of SKiiP intelligent power modules and complete Semistack power electronic assemblies. Also Infineon will focus more on power electronics for renewable energies once the acquisition of their wireless solution business by Intel will be completed early next year. In particular the company plans to invest in the further development of power semiconductors based on Silicon Carbide and also Gallium Nitride. Additionally Infineon will produce discrete power semiconductors such as MOSFETs and IGBTs on 300mm wafers. This step shall push productivity and secure the leading position in power semiconductors. The long-term goal is to grow to a €5 billion company. This growth will be fueled by the exploding markets in renewable energies, associated power transmission based on smart grids and the electrification of automobiles, all relying heavily on semiconductors and power semiconductors in particular.

Thus the future of power electronics seems to be bright along with the growth (not only) in renewable energy applications!

Achim Scharf
PEE Editor

Record Revenues and Profits with Semiconductors

Chip suppliers are reporting rising inventory, but the swelling stockpiles do not represent a cause for concern in the industry at present with demand expected to increase during the coming months, according to semiconductor industry analyser iSuppli. And the power semiconductor industry will finish 2010 on a high note.

Midway through the second-quarter reporting period, total chip inventory among the approximately 35 semiconductor component manufacturers tracked, climbed to $9.6 billion, up a strong 9% from $8.9 billion in the first quarter - faster than the seasonal average of 3.2%. Likewise, average Days of Inventory (DOI) grew, increasing by about four days during the period to 73 days, up 6% from 69 days - a rate slower than the historical DOI seasonal increase of 9.6%, or 6 days.

All told, the numbers underline a common theme for the semiconductor industry in the second quarter of record revenues, profits and gross margins. Such indicators, along with positive revenue guidance for the third quarter, are providing managers with the confidence needed to increase inventories for the second half of the year. "Across the semiconductor market, management comments in earnings announcements have been extremely positive, citing strong results in various end applications and geographies", commented semiconductor manufacturing researcher Sharon Stiefel. "The solid second-quarter results, based on higher-than-usual seasonal revenues, favourable Average Selling Prices and innovative new products, are allowing companies to finally relax their vice grip on inventories". Given the quick rise in demand, however, semiconductor suppliers are finding it difficult to restock to pre-recessionary levels. Products being shipped are intended to meet current orders and not meant for placement into inventory.

As a result, the current backlog is driving many semiconductor suppliers to increase capacity, although conservative capital spending appears to be the norm. Instead of committing to long-term capital investments for new facilities, suppliers often are investing cautiously in equipment to relieve constriction points in production. The exceptions to the rule are the large corporations, entities such as Intel Corp. and Samsung Electronics Co. Ltd., with enough cash to invest, the economic downturn notwithstanding.

Power management semiconductors to enjoy unparalleled growth this year

Fueled by gains in both the commercial and industrial sectors, the power management semiconductor industry will finish 2010 on a high note that will be unmatched over the next few years. Comprising ICs and discretes, power management semiconductors will generate $31.4 billion in 2010, up a sizable 40% from $22.4 billion in 2009. This year's expansion not only will reverse the losses of 2009, when revenue declined by 16%, it also will be unequaled during the next four years, none of which will enjoy growth higher than 13%. "Growth was solid for the first half of the year, marked by an exceptionally robust first quarter, due mainly to demand in the industrial and communication markets, as well as to deliveries that had been pushed to the start of this year after the component shortages of late 2009", said, principal analyst Marijana Vukicevic. "Revenue will continue to expand into the third quarter,after which the market will slow as the year ends, in keeping with normal seasonal patterns. For the second half of the year, growth will be propelled by demand in the consumer electronics, wireless and data processing sectors, reflecting the overall improvement of the Consumer Confidence Index. Prices, however, are likely to increase as backlogs ease at the backend, and some time will be needed before supply catches up with demand".

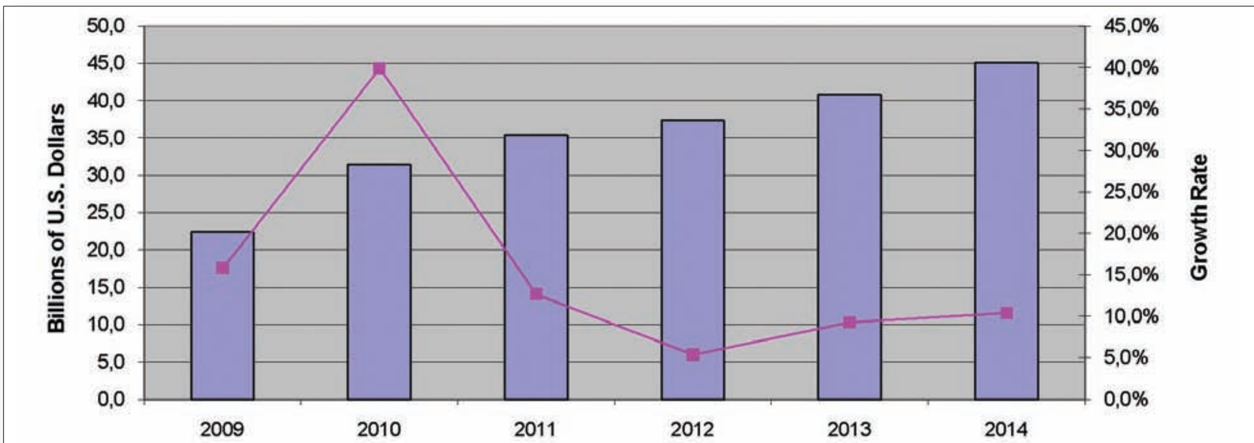
Over the next five years, a good part of growth in power management semiconductors will derive from the vibrant alternative energy market, which will bring inverters to the attention of many suppliers. The need for inverters will stem from applications in the automotive, solar and wind turbine markets. Revenue is expected to more than double by 2014, reaching more than $7 billion, compared to $2.9 billion in 2009.

Among the various types of power management semiconductors, the fastest growth will take place among power MOSFETs. Power MOSFET revenue will increase at a Compound Annual Growth Rate of 21%, higher than any type of power management semiconductor in either the discrete or IC category. The best performer will be low-voltage discretes, exploding at a runaway CAGR of 26% with forecasted revenue by 2014 of $4.9 billion. Several markets will contribute to the growth of low-voltage power MOSFETs, including wired communications, consumer, automotive and industrial. Overall, ICs will slightly outpace discretes in growth during the period, total revenue will climb from $12.4 billion in 2009 to $25.3 billion by 2014, a CAGR of 15.3%. In comparison, total revenue for discretes will rise from $10 billion to $19.7 billion, a CAGR of 14.5%.

Power semiconductors as a whole are expected to grow about 15%, driven mainly by the notebook market, server infrastructure replacement and alternative energy requirements issuing from hybrid and electric vehicles, wind and solar energy and grid upgrades.

Furthermore, observable improvements in the efficiency of electronics products and processes that make use of the semiconductors - everything from power tools to forklifts, from trains to cars - can be considered an emerging trend for power management, iSuppli believes.

www.isuppli.com



Revenue projections for the power management semiconductor market from 2009 to 2014 Source: iSuppli August 2010

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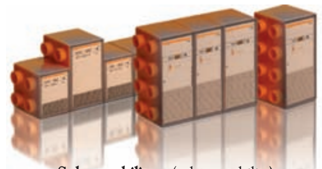

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Solar Inverter Shipments hit 5GW

Solar inverter shipments reached 4.9 GW in Q2 2010, growing by 284%, according to IMS Research.

More than half of these shipments were for installations in Germany, which grew by 388% in Q2, driving total shipments up to more than 8GW for the first six months of 2010 - a three-fold increase over the same period last year. EMEA accounted for around 90% of inverter shipments in Q2, growing by more than 300% over the previous year; further, the Americas market doubled in size. Indeed, all regions recorded impressive growth, generating around €1.5 billion in revenues for inverter suppliers. The inverter shipments of more than 8 GW in the first half 2010 were similar to shipments for the whole of 2009. "Records continue to be broken in the PV market and Q2 was no different. 4.9GW of inverters shipped made it the largest quarter on record and 30% higher than the previous record of 3.7GW shipped in Q4'09", commented PV Research Director Ash Sharma. "Shipments of 8 GW in the first six months of the year appear to support our prediction of close to 15GW of new PV installations in 2010; with Q3 and Q4 both expected to be strong quarters for suppliers".

Whilst MW shipments grew 284% in Q2, revenues 'only' grew by 165% due to a 30% fall in inverter prices. Despite extraordinarily high demand amidst tight supply, inverter prices fell for the fifth consecutive quarter in Q2 2010. Much of this, however, can be attributed to a continuing shift towards larger inverters, which have an inherently lower price per watt.

With the market being affected both by extremely high demand and also production issues, major changes in the market share of suppliers are expected this year. IMS Research estimates that market leader, SMA Solar Technology's market share fell by 5% in Q2, whilst Power-One was the industry's biggest share gainer, up by more than 6%.

On the other hand, solar microinverters and DC/DC power optimizers are forecast to generate more than $1.5 billion in revenues over the next five years. Shipments of the devices are forecast to grow over 100% per year and will total more than 16 million in the same period. Both microinverters and power optimizers are possible solutions for PV installations that suffer from shading or orientation problems, which is where IMS predicts they will see greatest uptake. However other possible advantages include the enhanced monitoring and communications, simpler installation, higher energy yields, and increased reliability by removing the single failure point of a central inverter. "Although last year there was only one supplier shipping any significant volume - Enphase Energy - that is all about to change; soon more than a dozen suppliers will be serving the growing market and even market leader SMA now has a microinverter platform following its acquisition of OKE", Sharma added.

www.pvmarketresearch.com

Power Semiconductors on 300mm Wafers by Infineon

Infineon Technologies and Intel Corporation have entered into a definitive agreement to transfer Infineon's wireless business to Intel in a cash transaction valued at approximately $1.4 billion. Thus Infineon's annual revenue will decrease from approximately €3 billion to €2 billion, but with the additional cash in hand the company intend to increase its position in power semiconductors.

"The sale of WLS is a strategic decision to enhance Infineon's value. We can now fully concentrate our resources towards strong growth in our core segments Automotive, Industrial & Multimarket (IMM) and Chip Card & Security (CCS). This creates a great perspective for our customers, employees and shareholders", commented CEO Peter Bauer this deal. "In particular we plan to invest in the further development of power semiconductors based on Silicon Carbide and also Gallium Nitride. Additionally we will produce discrete power semiconductors such as MOSFETs and IGBTs based on our thin wafer technology on 300mm wafers. This step will push productivity and secure our leading position in power semiconductors. Our long-term goal is to grow with our three core businesses to a €5 billion company", Bauer stated. This growth will be fueled by the exploding markets in renewable energies, associated power transmission based on smart grids and the electrification of automobiles, all relying heavily on semiconductors and power semiconductors in particular.

With this strategy Infineon follows Texas Instruments, purchasing 300mm wafer processing equipment for favourable pricing from former Infineon DRAM subsidary Qimonda who went bankrupt in April 2009. TI will ship first low-power (up to 40V) semiconductors manufactured on 300mm wafers by end of this year.

www.infineon.com

Infineon's CEO Peter Bauer plans to increase the company's power semiconductor business by moving to 300mm wafers

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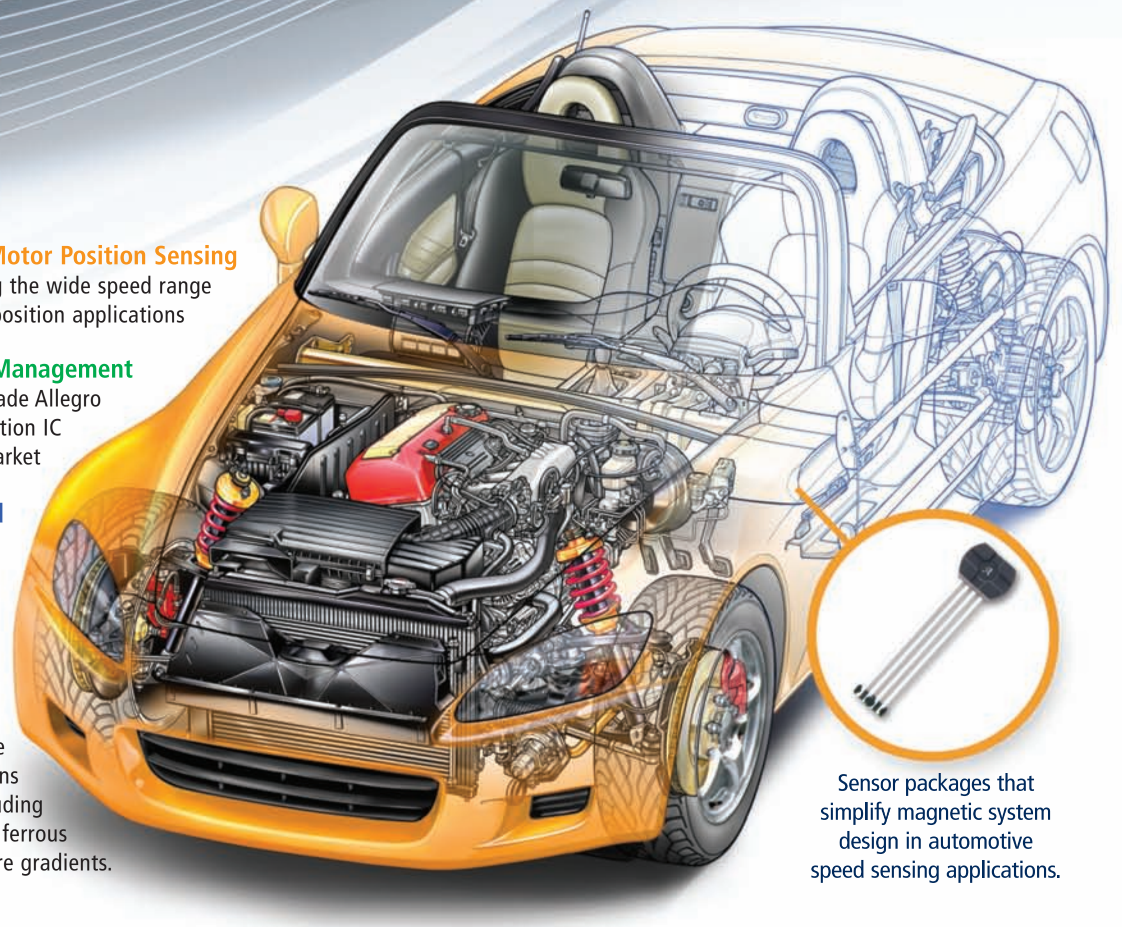

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Electrical Metering Market Changes Face

Smart meters are dramatically changing the way energy is produced, bought, sold and consumed. In the global fight against carbon emissions, smart meters are set to play a key role in encouraging increased consumer awareness of energy consumption, more dynamic pricing and a consequent drop in demand, expects Mark England, CEO of UK-based Sentec.

Smart metering rollouts are taking place in many countries as governments address stringent carbon-reduction targets. But the progress of these rollouts is markedly different across different countries. In the UK, preparations for the nationwide smart meter rollout are well underway, with British Gas recently announcing that it is doubling the scope of its smart metering programme to install meters in two million homes by 2012. Individual countries within Europe are at very different stages along the path to smart metering. Spain is currently undergoing large-scale trials, and Sweden has nearly completed its roll out of smart meters. While a number of other EU countries are also considering their own rollouts in the next decade, including France, Ireland, and Portugal, there are some clear lessons to be learned from international peers. For instance, some early adopters have run up against a technical stumbling block as they discover that their first-generation smart meters, developed to support time-of-use pricing and fraud detection, now need upgrading for more sophisticated functions.

With specifying and manufacturing meters becoming steadily easier, the sector is seeing mounting interest from non-traditional players who are following the lead of large utilities like Enel and introducing their own proprietary meter designs. Even Google wants a piece of the action, launching its own free energy monitoring tool, Google PowerMeter, which uses energy information provided by utility smart meters and energy monitoring devices to allow users to view their home's energy consumption from anywhere online. Microsoft has also launched a rival online power management tool called Hohm, which provides users with personalised energy-saving recommendations such as placing new caulking on windows, eliminating air leaks, and installing a programmable thermostat.

The pace - and success - of smart metering rollouts is likely to vary widely by region and by country. In the US, the smart meter market is driven primarily by the communications infrastructure and is characterised by a profusion of relatively new players. The incumbent manufacturers have already adopted their own proprietary communication solutions to compete. However, the US market is likely to be a tougher nut to crack for these newcomers, largely because they lack the scale of their manufacturing counterparts in Europe. In Europe, several large utilities now dominate the energy sector, and consequently the smart metering landscape. Huge utilities like Germany's RWE and Italy's Enel have a network of subsidiaries that give them enormous cross-border scope across Europe. And as these utilities start to operate across multiple territories, the road towards adopting a single, cohesive standard of metering throughout Europe suddenly becomes much smoother. "Smart metering is already a reality and will represent a long-term change in the way customers and suppliers alike view their relationship with energy. As smart metering technology becomes ever more sophisticated, it is likely to act as a springboard for broader smart grid technology applications as they develop. This is a market with huge potential for both new and existing industry players to make their mark through meter designs, communications solutions and software development", Mark England expects.

Sentec's CEO Mark England predicts a huge market potential for smart meters along with the deployment of smart grids

According to market researcher Greenbang, the smart electricity market in the European Union is expected to expand rapidly in coming years up to $26 billion by the year 2020. Government initiatives, growing demand for energy, and rising oil prices are all expected to result in between 133 to 145 million new smart meters being installed by the end of the decade. Recently the EU set the target of installing smart meters in 80% of households by 2020. It is estimated that only about 53 million smart meters are currently installed across Europe.

www.sentec.co.uk, www.greenbang.com

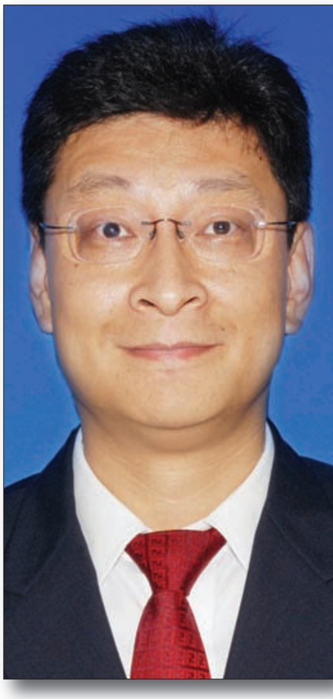
Isabellenhütte and Austriamicrosystems Cooperate

Isabellenhütte is one of the pioneers in current and voltage measurement of 12V vehicle batteries. In 2002, the company introduced the ISA-ASIC, the world's first all-in-one measuring system for current, voltage and temperature for electronic battery management. Together with Austriamicrosystems, an international leader in the design and production of high-performance analogue ICs, the company has produced numerous ICs for 12V vehicle systems in recent years.

This longstanding relationship has now led to a cooperation agreement being signed by both companies to focus their expertise. This will provide them with advantages for future development work and drive market penetration. The partners have already introduced sustainable solutions for measuring the current of 12V and 24V batteries and also high-voltage systems for hybrid and electric vehicles and will now jointly continue developing their products. "We feel that by joining forces we are increasing our opportunities for developing and producing flexible and adaptable sensor systems", said Isabellenhütte's Managing Director Peter Müller. "We anticipate that demand for ICs will continue to rise, as battery management is a key technology for hybrid and electric vehicles", added Bernhard Czar, Marketing Director at Austriamicrosystems AG.

www.isabellenhuette.de

Chinese Goldwind Prefers Semikron for Wind Turbines



Semikron's Chinese Managing Director entered in a long-term supply agreement with leading wind power manufacturer Goldwind

Xinjiang-based Goldwind Science & Technology recently signed a sales contract directly with Semikron China thereby ensuring the continued supply of SKiiP intelligent power modules and complete Semistack power electronic assemblies for the Goldwind wind power generators.

"Semikron technology powers nearly half of the globally installed wind power capacity and Goldwind is one of the top five wind turbine manufacturers in the world. Our goal is to establish a long-term business relationship providing the most efficient technology and best service beneficial to both companies", commented Lixin Ren, Managing Director of Semikron Greater China. In 2009, Semikron expanded its global network of Solution Centers to Zhuhai, China. The new solution center specializes in the design and manufacture of SEMISTACK power assemblies based on SKiiP for wind generators and solar power inverters. Customers can benefit from 'made in China with German quality' power assemblies with flexible and customized designs, local technical support, fast deliveries and competitive pricing.

China has the world's second largest wind power capacity after the US and just ahead of Germany. In 2009, 13.7GW wind power was installed thereby more than doubling the cumulative installed capacity in a single year, which has now reached 25.8GW (Source: BTM Consult APS, March 2010). Goldwind is one of the first enterprises in China focusing on research and manufacturing for wind turbines. Since 2000, Goldwind has had an average annual growth of 100% for the last ten consecutive years and has a market share of 7.2% of the newly installed wind power capacity in 2009. According to a survey carried out by BTM Consult, the total wind power capacity installed until 2009 was 122GW, around 57GW comprises semiconductors from Semikron. "Semikron's experience in stack design and production gave us confidence that we can work together and achieve long-term success", added Kai Wu, Goldwind's Supply Chain Management Manager.

www.semikron.com, ww.goldwind.cn

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PCIM 2011 Call for Papers

The Call for Papers PCIM Europe 2011 is now open. Deadline for abstract submissions is 15 October 2010. The event is Europe's number one meeting place for all fields of Power Electronics, Intelligent Motion and Power Quality/Energy Management.

The topics of lectures cover, amongst others, recent developments in power semiconductors, passive components, products for thermal management, new materials and their application as well as power quality, smart grids and energy management.

Proposals will be considered for conference papers or posters. The successful papers will be selected by the Advisory Board which comprises international experts from industry and academia supported by the overall Conference Director Prof. Leo Lorenz. All accepted papers will be included in the official PCIM proceedings CD and the IET Inspec database.

The winner of the Best Paper Award will receive 1,000 Euro and the participation at PCIM China Conference in Shanghai including flights and accommodation. For outstanding contributions from young authors not older than 35, three "Young Engineer Awards" of €1,000 each will be granted. The prizes will be awarded at the PCIM Europe 2011 Conference.

www.pcim.de

Third Generation Press-Pack IGBTs and Diodes for Megawatt Applications

Press-pack IGBT technology has come of age with the introduction of the latest generation of soft punch through die. Background to the evolution of the new generation and its enhanced characteristics are introduced for the largest member of the product family. With high reliability and low losses, the new device is ideal for today's demanding environment of high efficiency and renewable energy sources. **A. Golland and F. Wakeman, Westcode Semiconductors Ltd, Chippenham, UK**

First introduced twelve years ago, as a high reliability solution for hostile environments, the press-pack IGBT has evolved towards the product of choice in many high power applications. The first European made devices were targeted at induction heating power supplies, a 1.8kV medium frequency device, offered as a solution to overcome the punishing thermal stress of such applications. These new introductions were both expensive to produce and very application specific. However, the robust nature of the design attracted wider appeal and new products were introduced with higher voltage and less application specific characteristics.

A first generation high voltage device, with current rating up to 900A, saw favour in traction applications [1]. Limitations of die technology meant these early high voltage devices, required snubbers and were more suited to GTO thyristor circuit topologies. A second generation of 4.5kV die followed, based on soft punch through technology, which offered more classical IGBT characteristics giving a wide appeal for a broader range of applications including drives, traction and utility applications. Now a third generation die set is launched with improved forward voltage and SOA performance. This new die set, in conjunction with larger package options, is an ideal solution for the needs of the latest generation of medium voltage drives.

Press-pack encapsulation of small die

The concept behind the press-pack housing is to keep it simple; all pressure contact, no solder or bonded joints [2]. However, to achieve this takes a great deal of control of materials and the manufacturing process. The key element of the press-pack IGBT evolution was the introduction of the single die cell with the first generation of high voltage devices [3]. Each individual IGBT die is mounted in its own cell, which can be pre-tested before assembly into the package, under clean room conditions. Among the latest generation of products the largest device boasts a 125mm contact electrode and 42 individual dies in hard parallel configuration (Figure 1). The multichip bondless technology offers unrivalled ruggedness, with thermal cycling

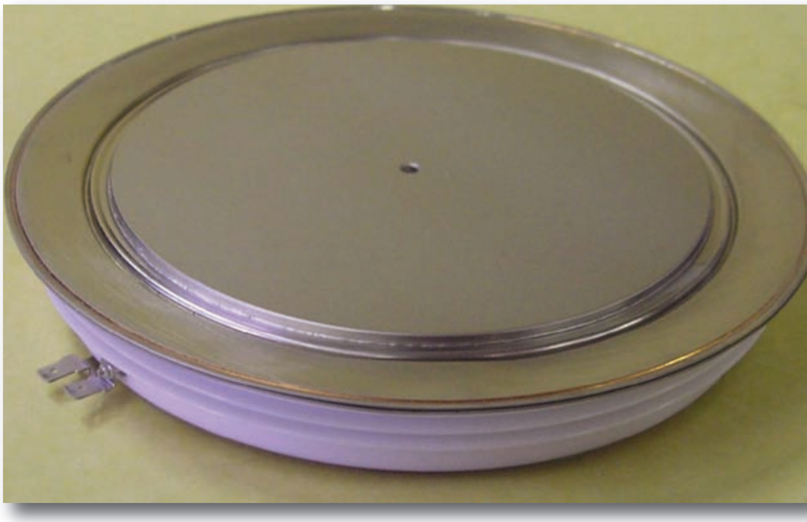


Figure 1: **Latest generation of IGBT press-packs boasting a 125mm contact electrode and 42 individual dies in hard parallel configuration**

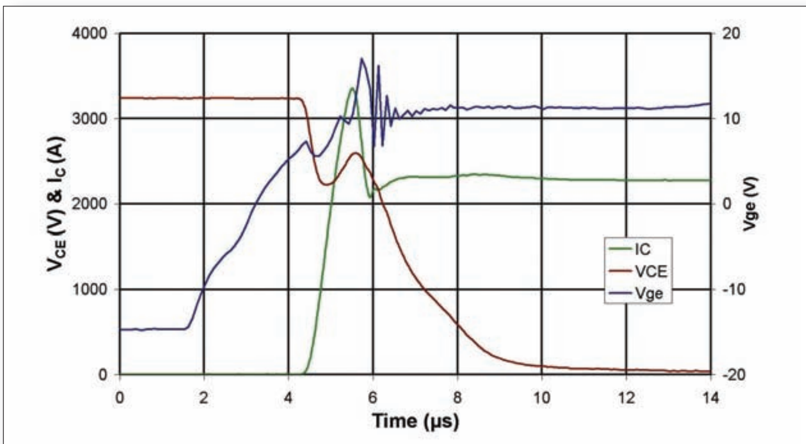


Figure 2: **Turn-on transient of the IGBT under nominal switching conditions**

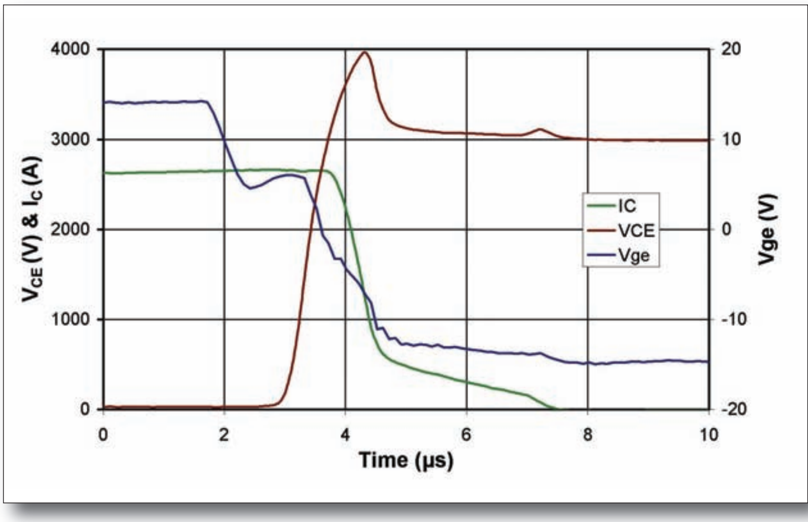


Figure 3: Turn-off transient of the IGBT under nominal switching conditions

capabilities beyond that of larger bondless monolithic devices or alternative multichip packaging concepts [4]. The fully hermetic double side cooled package makes the device suitable for all cooling systems; air, liquid and even full immersion. Also failure to short circuit and a predictable rupture rating give more options in system protection.

Improved die technology

The new chipset technology is the latest evolution of our soft punch through planar cell design, which has been proven in press-pack applications over the last seven years. The new enhanced cell design features the addition of an N-enhancement layer, along with further optimisation and tight control of the emitter structure. This gives a significantly improved carrier concentration under the emitter. The more favourable carrier distribution leads to 25% reduction in $V_{ce(sat)}$ (typically 3.6V at nominal current and $T_{j\,max}$) without any appreciable increase in the turn-off losses, when compared to the previous generation.

Careful optimisation of the deep low concentration buffer and anode gives a positive temperature coefficient throughout the entire current range, which is important for very large area devices and also ensures excellent short circuit performance, well in excess of typical requirements. We are now able to offer technology with on-state losses broadly comparable to that available with typical trench designs, while retaining the superiour Reverse Bias Safe Operating Area (RBSOA), Short Circuit Safe Operating Area (SCSOA), soft switching behaviour and easy driving characteristics associated with our planar technology. Similarly, a new diode chip complements the new IGBTs in our reverse conducting parts, along with our third generation HP Sonic-FRD monolithic diodes to support the asymmetric parts and clamping applications.

2400A / 4500V asymmetric device performance

To fully evaluate and qualify the T2400GB45E IGBT, an extensive range of measurements has been carried out. The device has a nominal current rating of 2400A, which equates to a current density of 57A/cm^2, and nominal DC-link voltage of 2.8kV, with RBSOA testing carried out up to 4800A and 3200V. All switching waveforms are shown with an E2400TC45C freewheeling diode and unclamped (stray) inductance of approximately 180nH. Junction temperatures are 125°C for the IGBT and 150°C for the diode unless stated otherwise.

Figure 2 shows the turn-on transient of the IGBT under nominal switching conditions with a gate resistor of 1.6Ω and additional gate-emitter capacitance of 267nF. The very low input capacitance of the enhanced planar cell provides a fast voltage fall time. In this case we are able to further optimise the switching conditions for both the IGBT and diode by combination of gate resistance and additional external capacitance. Under these conditions typical turn-on losses are 7.2J.

Figure 3 shows the turn-off transient of the IGBT under nominal switching conditions with a gate resistor of 1.5Ω and additional gate-emitter capacitance of 267nF. The highly rugged cell allows high switching speed, while the carefully optimised buffer ensures a soft turn-off transient with no voltage disturbances or oscillations, even at high DC-link and stray inductance levels. Under these conditions typical turn-off losses are 7.85J.

Figures 4 and 5 show the turn-on and turn-off transients respectively under RBSOA conditions. The device can clearly be seen in figure 7 to be sustaining a large amount of energy in the dynamic avalanche mode, evident by the self-limiting of dv/dt and clamping of the peak induced turn-off voltage for a period of approximately 1.8µs; no external voltage clamps or snubbers are applied. RBSOA

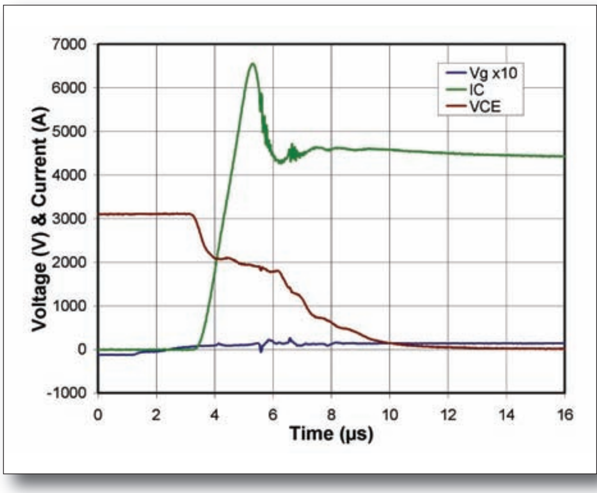


Figure 4: Turn-on transient of the IGBT under RBSOA conditions

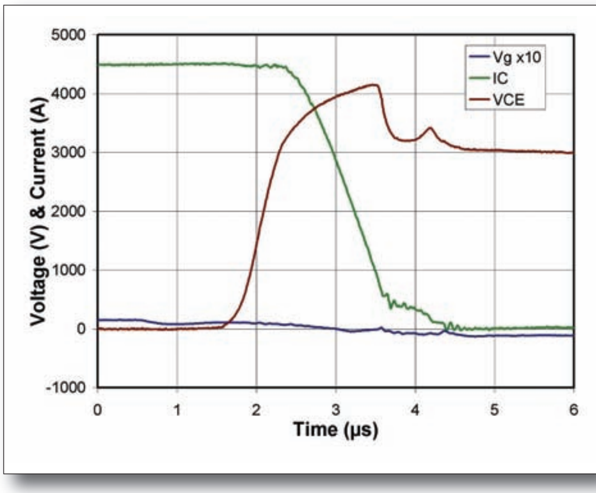
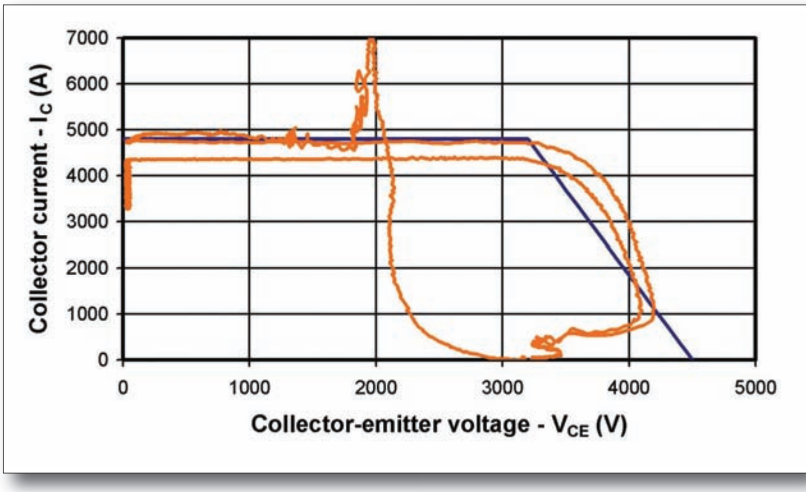


Figure 5: Turn-off transient of the IGBT under RBSOA conditions

Figure 6: Switching loci of a double pulse RBSOA test overlaid on the device data sheet limit characteristic



does not increase linearly with device voltage and for high voltage devices this parameter becomes technically challenging.

Furthermore as the device current increases, the insertion and therefore total commutation loop inductance tends to increase due to larger package size and larger busbar requirements; this in turn dramatically increases the energy stored in the unclamped inductance that each individual die must sustain (in an ideal situation the inductance would reduce linearly as the number of die increases to maintain the same effective inductance per die or per ampere). The advanced low loss technology combined with the superiour thermal performance of the press-pack construction change the fundamental limits for typical inverter designs. No longer are designs limited by average current, rather commutation or peak currents (RSOA) become the limiting factor.

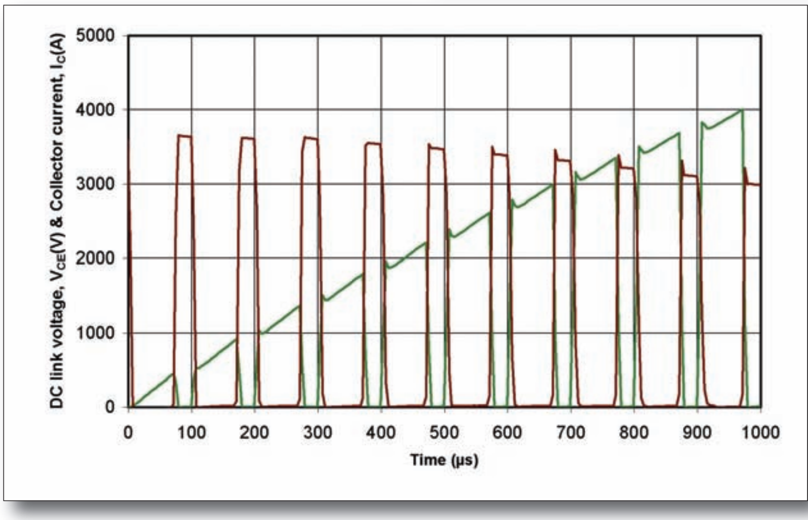


Figure 7: Additional RBSOA test conducted as a burst of 10 pulses at a frequency of 10kHz from an initial voltage of 3.6kV

Figure 6 shows switching loci of a double pulse RBSOA test overlaid on the device data sheet limit characteristic. Figure 7 shows an additional RBSOA test conducted as a burst of 10 pulses at a frequency of 10kHz from an initial voltage of 3.6kV with current increasing to 4kA, further demonstrating the outstanding robust nature of these devices.

Figure 8 shows a typical type I short

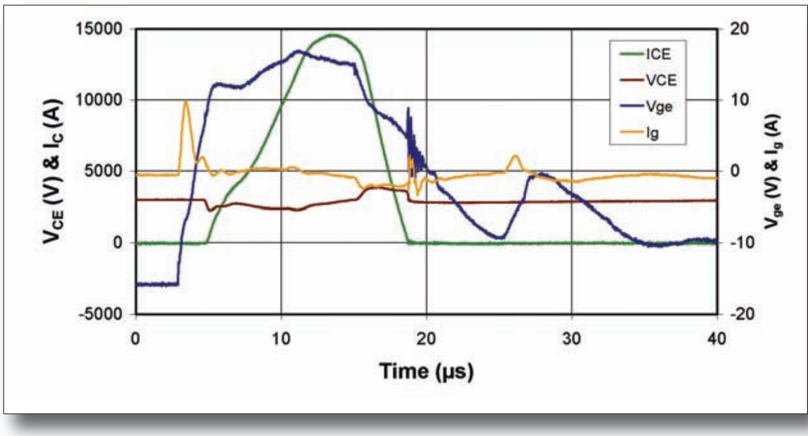


Figure 8: Typical type I short circuit test waveform at DC-link voltage of 3kV and nominal pulse width of 13µs

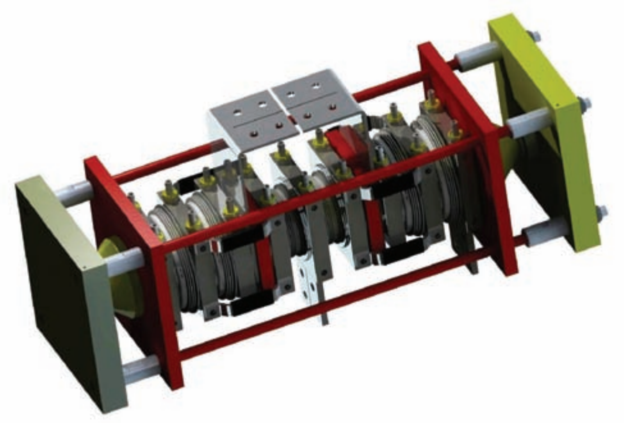


Figure 9: Typical phase leg arrangement for a 1600A, 3.3kV neutral point clamped inverter phase leg

circuit test waveform at DC-link voltage of 3kV and nominal pulse width of 13μs using a soft turn-off gate resistor of 10Ω. The device is able to withstand both type I and II short circuit events with gate voltages up to 18V across the full operating temperature range.

Multi-megawatt applications

The high current rating and high DC-link rating make this device a natural fit for medium applications in the multi-megawatt power range. In particular the press-pack construction lends its self well for multilevel water-cooled converters where extremely high power density is achievable. Figure 9 shows a typical phase leg arrangement for a 1600A, 3.3kV neutral point clamped inverter phase leg and Figure 10 shows the possible configuration of an 18MW, 6.6kV variable speed drive. These ratings fit well to a wide range of applications including high performance motor drives, high-speed locomotive traction, railway interties, utility scale VAr and power quality compensators and renewable grid converters, to name a few.

Of specific emerging interest is the current trend toward medium voltage machines for the next generation of wind turbines. Particularly in offshore applications, where ratings of 6-8MW are in development employing full-scale power conversion at 3.3kV, for both machine and grid side connection. The very high power density converter solutions possible with the press-pack IGBT, combined with high reliability and fully hermetic construction make this an extremely attractive solution to the unique challenges of these next generation turbines.

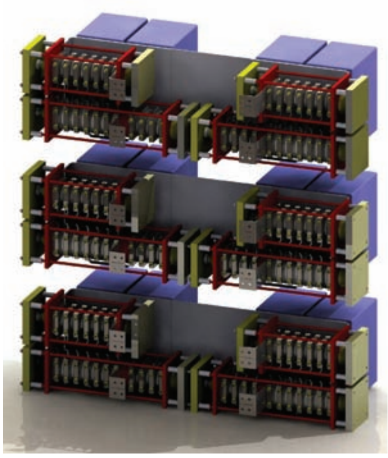


Figure 10: Possible configuration of an 18MW, 6.6kV variable speed drive

Literature

[1] F. Wakeman & A. Golland, "Press-pack IGBTs for traction applications", Power Electronics Europe, issue 1, 2004.

[2] F. Wakeman, K. Billett, R. Irons & M. Evans, "Electromechanical characteristics of a bondless pressure contact IGBT" APEC 1999, pp312-317.

[3]. F. Wakeman, G. Li & A. Golland, "New family of 4.5kV Press-pack IGBTs" PCIM Europe 2005.

[4] F. Wakeman, D. Hemmings, W. Findlay & G. Lockwood, "Pressure contact IGBT, testing for reliability", PCIM Europe 2000.

IGBT Gate Driver Solutions for Low and Medium Power Applications

Power electronics systems are commonly used in motor drive, power supply and power conversion applications. They cover a wide output power spectrum: from several hundred watts in small drives up to megawatts in wind power installations or large drive systems. Inside the system the gate driver circuit with its extensive control and monitoring functions forms the interface between the microcontroller and the power switches (IGBT). In this second part of the article fully integrated gate driver solutions for the low power range, their technologies, circuit aspects and specific designs are shown and discussed. **R. Herzer, J. Lehmann, M. Rossberg, B. Vogler, SEMIKRON Elektronik, Nuremberg, Germany**

IGBT driver solutions for low and medium power applications (600V, 1200V, <50A) are aimed at high volume markets, where system costs and geometric size per function are the most relevant parameters. IC-based designs are thus replacing conventional hybrid IGBT drivers [4, 14, 15, 16]. As already discussed in the chapter 'Gate driver topologies and insulation principles' [30] for an asymmetric grounded DC link and low power applications, the microcontroller, th e primary side, the emitter and secondary side gate driver of the low side switch (BOT) can be placed on the same ground potential. In this case a potential separation is only necessary for the secondary side of high side switch (TOP).

System and high voltage IC design

Figure 10 shows a typical block circuit diagram of a 3-phase power conversion system with an additional 7th channel at the low side to support power factor correction schemes or to be used as a brake chopper. The topological blocks to be integrated into a gate driver HVIC are marked (orange). Depending on the different applications only high side- [17], half-bridge [14] and six-pack driver ICs [4] are also possible, as well as the integration of additional blocks such as bootstrap-diodes or charge pumps for power supply and VCE detection diodes and circuits.

The corresponding block diagram of a monolithic integrated 7-channel IGBT driver (Sevenpack) is given in Figure 11. Input interfaces (IIF) serve to process logic thresholds for direct connection to 5V or 3.3V microcontrollers. An interlock and dead time between TOP and BOT switch of a half-bridge is usually implemented in the external drive controller pattern but in many cases an additional hardware interlock and dead time is implemented in the gate driver as well as a short pulse suppression.

Three 600V (or 1200V) level-shifters transfer the signals to the fully insulated high sides, where the differential transmission signals are filtered and reconstructed. The signals are driven at the chip output by a CMOS stage. The output currents (sink/source) vary from several hundred mA up to 4.5A [19]. The driver operates normally at 15V ($V_{op,max}$ to 20V).

The branch delay times of the six main channels TOP/BOT1-3 are delay-matched to ensure synchronized switching. Logic and error management generate the appropriate internal signals. These take into account not only under-voltage lockout (UVLO, primary and secondary side) as derived from a bandgap-stabilized reference but also external analog sensor signals such as shunt current monitoring.

Complete integration of an IGBT gate driver exit demands the following technological requirements:

- Insulation technology for the certain electrical separation of low- and high-side circuit blocks. Here PN-insulation [4, 14], dielectric insulation (SOI) [6] and mixed technologies of both [20] are used today.
- High-voltage devices of the 600V and 1200V class respectively, which can be used as level-shifter (no galvanic insulation). The lateral DMOS-transistor

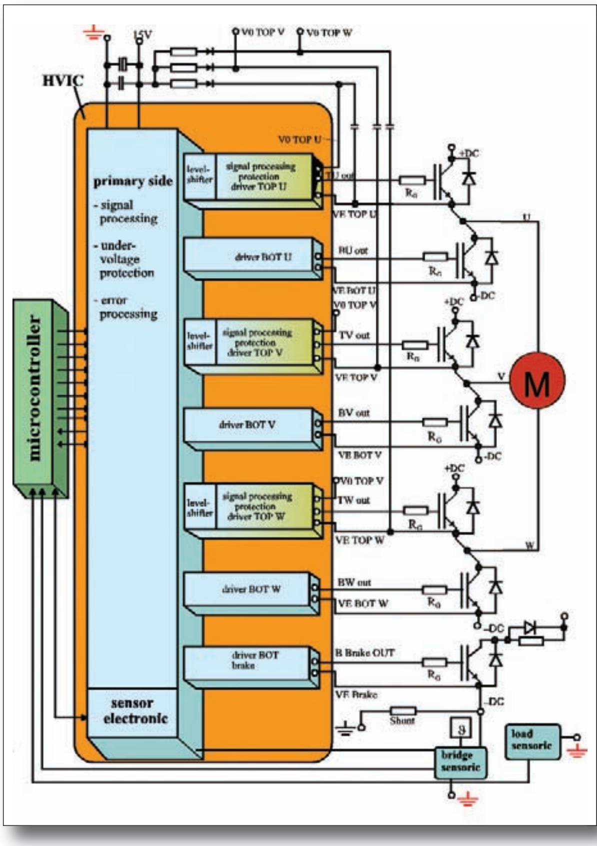


Figure 10: Power conversion system showing gate driver HVIC integration area

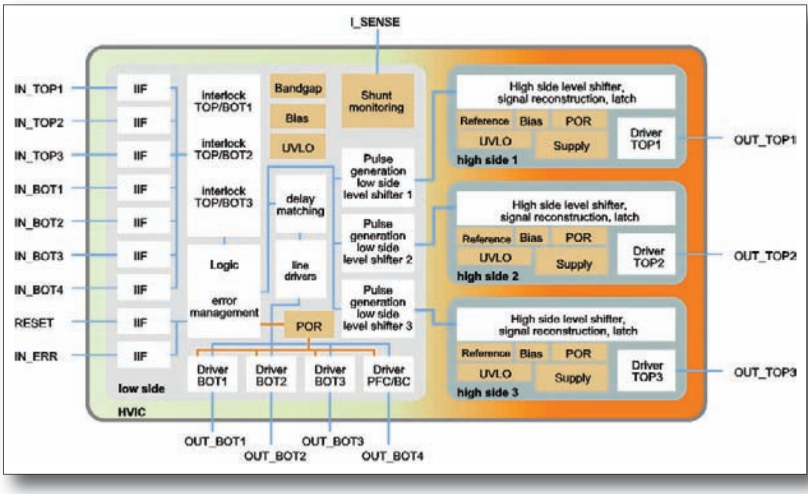


Figure 11: Typical block diagram of a monolithic integrated IGBT driver for seven switches (Sevenpack driver)

as classic RESURF (Figure 12) or as SOI-RESURF (Figure 14) device is the most common solution.

- Digital and analog circuits for operation voltages up to 20V for signal processing, control and driver functions on the low and particularly on the high side, where the ground potential is coupled on the emitter potential of the TOP switch and extreme voltage transients occur.

Gate driver in PN-insulation technology

The most important advantage of PN-insulation is that the device structures can be adjusted to the different voltage classes (600V, 1200V) by scaling of edge termination structure and doping concentration and depth of epitaxial layer, although of course the charges increase with the blocking voltage. This is shown in Figure 12 where the cross sections of the fundamental device structures are similar for the 600V and 1200V class, but the doping concentrations and distances are completely different. The full blocking voltage between high side and low side drops completely at the N- epitaxy / P-substrate junction and its lateral edge termination structure. Because of the large depth of N- region a parasitic coupling of the buried PN-junction on the active circuits on the surface can be avoided, especially at floating high side (Figure 12 middle). This makes the realization of sensitive analog circuits on the TOP-secondary side possible.

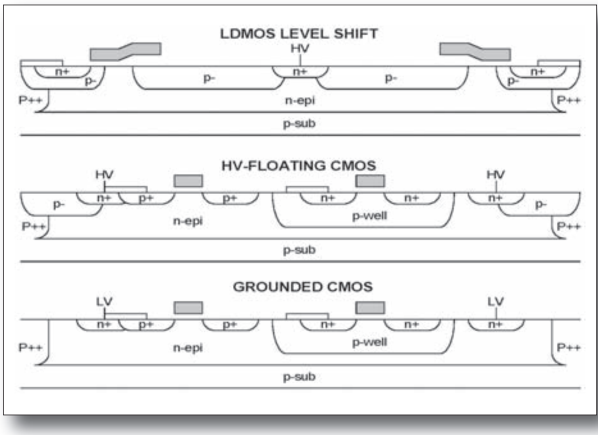


Figure 12: Fundamental device structures of a 600V/1200V PN-insulation technology [18]

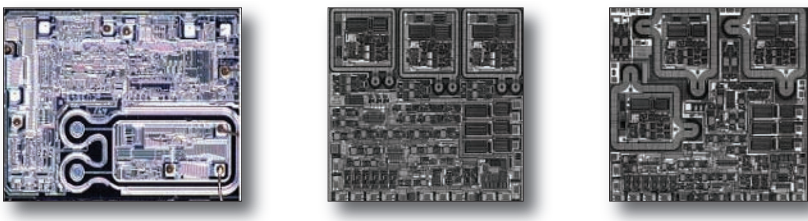


Figure 13: Chip photographs of different driver ICs in PN-insulation technology; left a 600V, 650/400 mA Halfbridge-driver [STM,14], in the middle a 600V, 500/250mA Sixpack-driver [IR,4,21], and right a 1200V, 500/250mA Sixpack-driver [IR,4,21]

Figure 13 shows chip photographs of different driver topologies, voltage and current classes of different manufactures. The insulated TOP secondary sides and their PN-edge termination structure around are clearly identifiable, as well as the driver output stages of every channel. In Figure 13 (left) and 13 (right) the differential level-shifters are embedded inside the termination structure while in Figure 13 (middle) the level-shifters are located separately.

Though the market has shown considerable interest in these compact and cheap high voltage driver ICs, the junction insulation has certain fundamental drawbacks. Negative transient voltages at the driver output can trigger internal parasitic thyristor structures, leading to latch-up. The problem can be somewhat alleviated by minority carrier suppression structures [22, 23] but it cannot be resolved completely. Also, PN leakage currents which increase with a factor of 4 per 10K temperature rise increase the losses and lead to an addition self-heating of the device which typically limits the operation temperature to 150°C.

Gate driver in SOI substrates

Appropriate high voltage silicon on insulator SOI-CMOS (600V) platform technology [24, 25] can provide complete latch-up immunity since all active devices are dielectrically insulated (see Figure 14). The regular CMOS circuits of the low side and the high side are based on quasi-bulk transistors in fully isolated silicon islands. This enables the operational temperature range to be considerably extended up to 200°C [6]. The active silicon is thick enough to prevent punch-through of the back side space charge region to the top side devices. The keys to the high breakdown voltages are the thick buried oxide layer and the selective layer thinning in the drift region of the high voltage devices.

Advanced level shifter concept

Even in low current applications and, yet more, in medium and high current applications, where high currents or high di/dt are switched, positive and negative voltage peaks may occur on parasitic elements in the power plane. These voltage peaks might cause a strong voltage drop between the primary and the secondary side of the gate driver (offset voltage). A negative offset voltage in particular is critical for junction-isolated HV-ICs [18, 14], commonly allowing only a few volts (typically -5V) below ground potential to prevent latch up [4]. Therefore the design goal for medium power applications is a significant extension of the

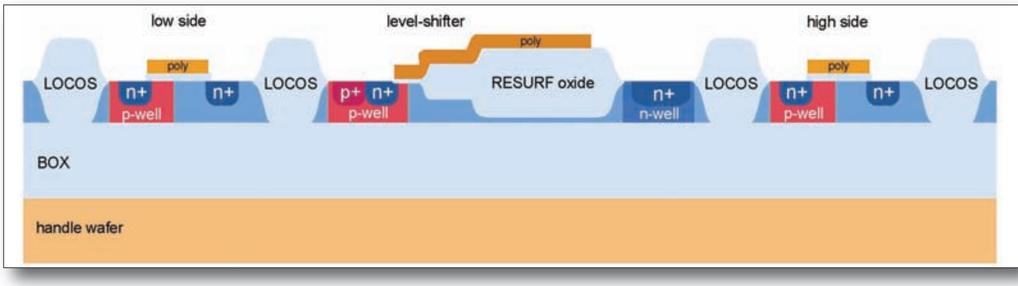


Figure 14: Schematic cross section of fundamental device structures of a 600V SOI-CMOS technology [24, NXP] [25]

range of the operational voltage shift between the primary side (control logic) and the secondary side (drivers). This requires an advanced level shifter concept for both the BOT and the TOP channel allowing "bipolar" operation.

The circuit principle of the BOT channel level shifter is shown in Figure 15. It consists of two independent transmission paths, an up-level shifter and a complementary down-level shifter. The configuration is that of a conventional static CMOS level shifter with additional diodes in each path. Both the up- and the down-level shifters use two cross coupled parallel branches with the function of a latch. Hence there are no cross currents under static voltage conditions. Because of the full dielectric insulation of each device, the circuit itself is latch-up free. For this reason and also that of the weak back gate effect

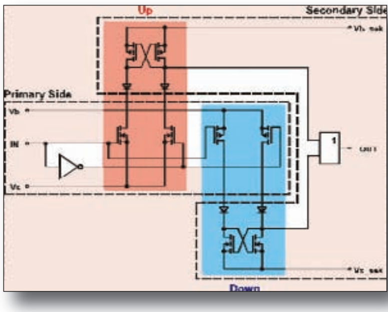


Figure 15: Circuit principle with up-/down- level shifter for the BOT channel

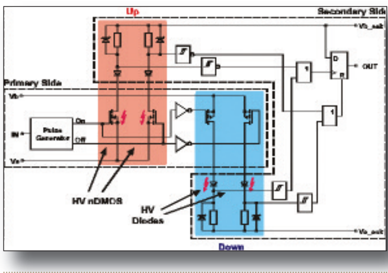


Figure 16: Circuit principle with up-/down- level shifter for the TOP channel

of the SOI technology used, every circuit part can carry any desired potential. The maximum allowable offset voltage is only limited by the breakdown voltage of the level shifter transistors.

Depending on the polarity of the offset voltage between the primary side and the secondary side ($V_{offset} = V_{s\_sek} - V_s$) the up-level shifter ($V_{offset} \geq 0V$) or the down-level shifter ($V_{offset} \leq 0V$) transmits the applied input signal from the primary to the secondary side. The inactive path is blocked by reverse-biased diodes. To reconstruct the signal on the secondary side, a simple logic disjunction can be used.

The circuit principle of the TOP channel level shifter is shown in Figure 16. As in the case of the BOT channel, the level shifter consists of two complementary parts - the high voltage up-level shifter and the low voltage down-level shifter. Because there are no p-MOS devices available with a breakdown voltage extending to 600V, a pulsed signal transmission simply requiring high-voltage n-DMOS transistors and high-voltage diodes, to block the high reverse voltage in the down-level shifter, is used. A pulsed transmission is applied to minimize the cross current and power consumption but requires more complex signal generation and reconstruction in comparison to the BOT channel. The differential transmission with two branches per level shifter, a robust signal processing and reconstruction on the secondary side provide maximum immunity against parasitic coupling from the power plane.

Seven channel 600V gate driver design

Figure 17 shows the chip photograph of a 7-channel gate driver IC. It contains all the functionality needed for a 3-phase power system and a fourth independent BOT channel is implemented for PFC or brake chopper applications according to the power conversion system of Figure 10 and the block diagram of Figure 11. It is realized in a 600V CMOS-SOI technology [24] whose cross section is shown in Figure 14.

The three insulated TOP secondary sides with their HV-DMOS-transistors and HV-diodes of up-/down- level shifter circuit (regarding Figure 16) are clearly to recognisable, as are the output stages of the 3 TOP and 4 BOT channels with 1.4A/1.4A (source/sink) peak current at

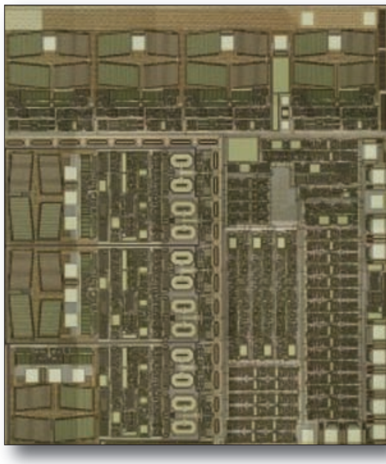


Figure 17: Chip photograph of a 600V/1.4A 7-channel gate driver IC in SOI-CMOS technology (chip size 4.6mm x 4.1mm)

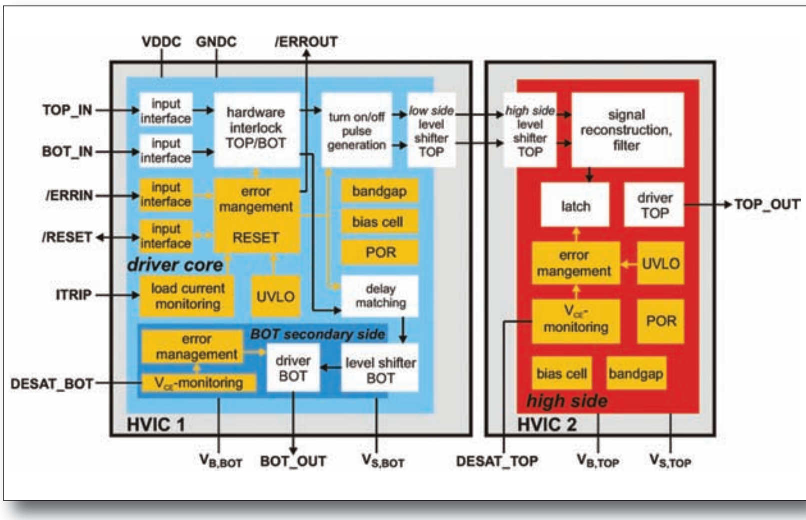


Figure 18: Block diagram of a two-chip 1200V SOI half-bridge gate driver

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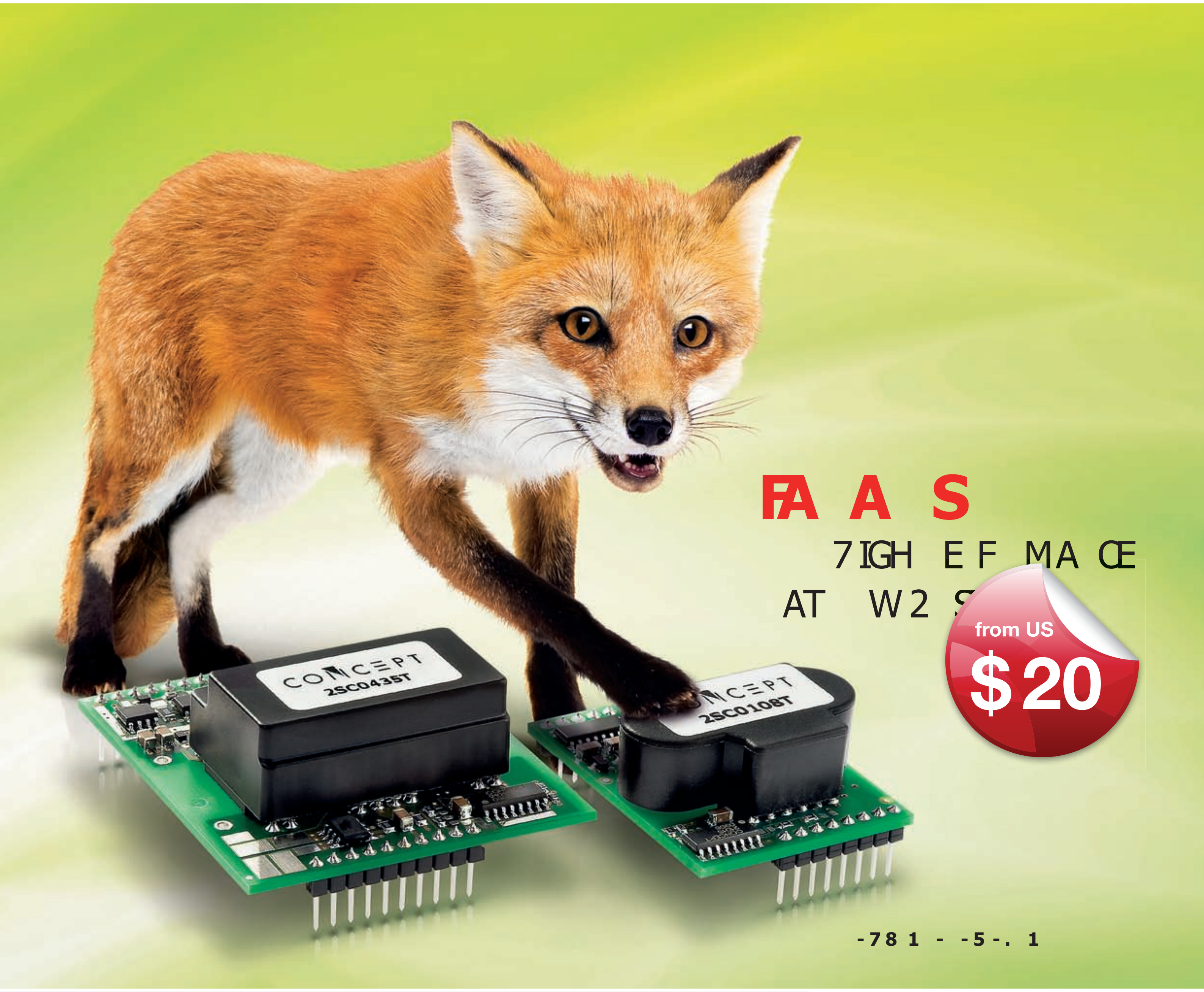

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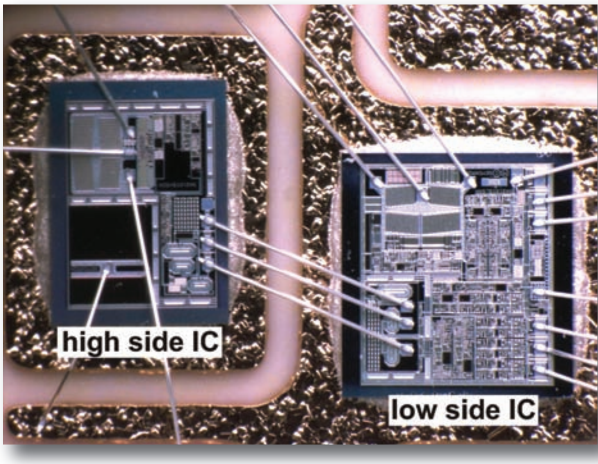

Figure 19: **Assembled two-chip 1200V, 1.4A/1.4A SOI half-bridge gate driver in a 1200V, 50A Sixpack-IPM**

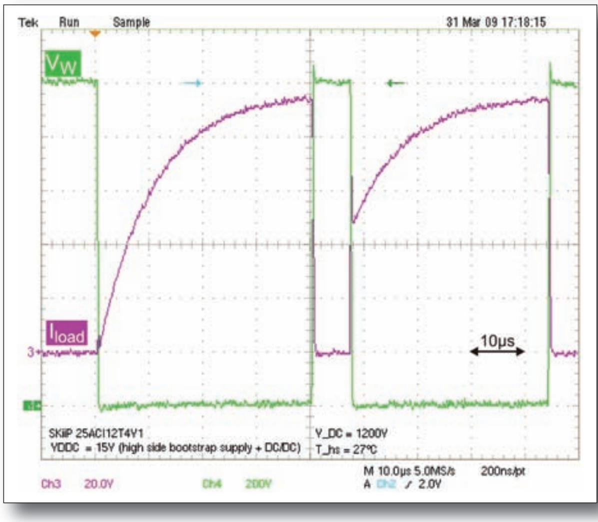

Figure 20: **Double pulse measurement (TOP-IGBT switched with load, V_{DC}=1200V, I_{load}=50A)**

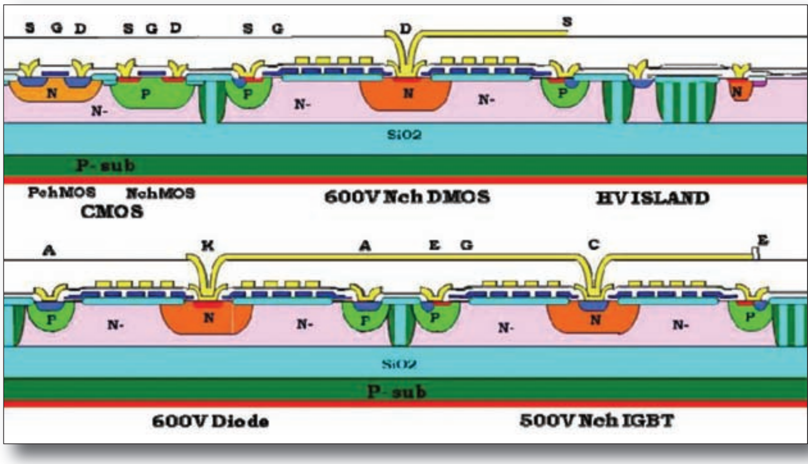

Figure 21: **Schematic cross section of fundamental device structures of a 500V SOI-CMOS technology [28]**

15V supply voltage and room temperature. In comparison to the PN-insulation driver designs in Figure 13, the insulation distances between low side and high side are very small due to the dielectric insulation. The design is extremely compact and the fully dielectric insulation of each device leads to low leakage currents and high latch-up ruggedness even at temperatures up to 200°C [6]. The capabilities of the level shifters are demonstrated experimentally in [13, 26]. The circuit remains operational for negative

reference voltages down to -45V (bottom channel) and -20V (top channel) respectively. The powerful output stages of every channel can drive the gates of 600V/50A IGBTs directly in IPM configurations [13]. Each TOP channel has a separate bandgap reference and an UVLO circuit in order to monitor the high side operational voltage. This may be important if the TOP channels are powered by a bootstrap circuit.

Advanced level shifter concept for 1200V CMOS-SOI gate drivers

600V gate drive ICs based on 600V SOI-CMOS can overcome most of the disadvantages of gate drive ICs which rely on conventional junction isolation. Nevertheless, SOI technologies for the 1200V class do not currently exist. For this reason a new concept for 1200V signal transmission and high side insulation has been developed and was implemented in the half-bridge gate driver IC here presented. The transmission of the control signals to the high side is based on a new 1200V level shifter topology with cascaded 600V transistors and without further signal processing on the originating intermediate potential. A balanced voltage division across the HV transistors during switching is achieved by a balanced capacitive divider. The implemented active clamping circuitry prevents the exceeding of the maximum voltages. The limited breakdown voltage of the vertical dielectric insulation of the SOI substrate (BOX, Figure 14) requires the subdivision of the offset voltages on two physically separated dies and that, in turn, requires that all high side functions are integrated in a separate high-side IC.

Figure 18 shows the block circuit diagram and Figure 19 the chip photography of a two-chip 1200V half-bridge gate driver. Exemplarly for the performance reached, Figure 20 shows a double pulse measurement of a 1200V/50A IGBT at 1200V DC link

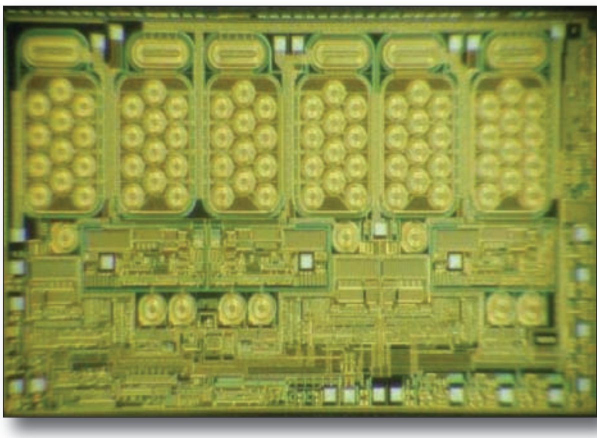

Figure 22: **Chip photograph of gate driver and 500V, 1A IGBT/FWD inverter in SOI-technology [28]**

voltage and rated current (50A) with inductive load.

Driver and inverter integration on a single chip

The fully dielectric insulation of every device in SOI-substrates enables also the integration of high-voltage bipolar devices like IGBTs and diodes together with driver and monitoring functions on the same chip. Figure 21 presents the cross section of the fundamental devices of this technology and Fig.22 the chip photograph of a 500V/1A inverter [27, 28 Mitsubishi]. For chip area and cooling reasons, such solutions are limited today on low power applications (several hundred watts).

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The Hazards of Hipot Testing

Hipot testing is an abbreviation for "high potential" testing - a category of electrical tests used to verify the effectiveness of electrical insulation in transformers, motors, printed circuit boards, electrical sub-assemblies (such as power supplies) and finished equipment. It's also known as "dielectric withstand" testing. This article considers the requirements for testing and provides broad guidelines on what is required of an equipment manufacturer in the type test procedure. It primarily refers to Class I equipment, the differences for Class II equipment are detailed separately. **Kent Smith, Applications Engineer, XP Power, Pangbourne, UK**

Electrical equipment that is connected to the AC mains supply must pass a 'type' test requirement by the relevant safety agency. The commonly applicable specifications are IEC60950-1 for ITE & industrial equipment and IEC60601-1 for medical equipment. Before sending equipment for type testing, the manufacturer, or the power supply manufacturer, will usually want to ensure that it meets the requirements by carrying out their own tests. However, test specifications can be misinterpreted, leading to damage to power supplies and delays in gaining the relevant approvals for a product to be brought to market. The safety regulations refer to the following types of insulation:

* Between primary (AC input) and secondary (DC output) reinforced insulation is required
* Between primary and earth basic insulation is required
* Between secondary and earth operational insulation is required

Class I equipment utilizes an insulation system where a protective earth is employed to ensure safe operation. Class II equipment utilizes double or reinforced insulation to ensure safe operation with no provision for protective earth. Figure 1 represents a typical Class I power supply insulation system.

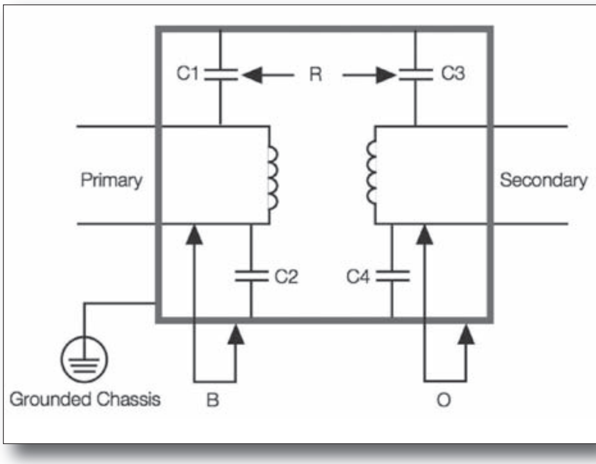


Figure 1: Typical power supply insulation (R - location of typical reinforced insulation; B - location of typical basic insulation; O - location of typical operational insulation)

Safety agency testing

Hipot testing requirements are categorized as either type testing (design verification) or production testing.

Hipot type testing is performed by the safety agency, and tests are intended to prove that the construction of the power supply meets the requirements dictated by the relevant safety standard. For IEC60950-1 (ITE) and IEC60601-1 (Medical) the requirements are shown in Table 1.

Hipot production testing is performed during the manufacturing process and is intended to ensure integrity of safety critical insulation. Production line testing is conducted on basic insulation and on reinforced insulation during the manufacturing process of the subassembly and barrier components.

Reinforced insulation cannot be tested without over-stressing basic insulation on the end product. (Note: see UL60950-1, C5.2.2 or UL60601-1 2nd Edition Section 20.4 or IEC60601-1 3rd Edition Section 8.8.3 for more information).

Because of this, manufacturers are permitted to test reinforced insulation separately, meaning that they are permitted to test transformers and other primary to secondary isolation barriers separately before other components are incorporated into the product. Only basic insulation or primary to earth insulation is tested on the final assembly prior to shipping the product.

Because only basic insulation exists between primary and chassis ground and only operational insulation exists between secondary and chassis ground, applying 3000VAC directly from primary to secondary on the finished product will over-stress the primary to chassis ground and secondary to chassis insulation resulting in a potential failure.

60950-1	Primary to Secondary	3000 VAC, or the equivalent DC voltage
	Primary to Grounded chassis	1500 VAC, or the equivalent DC voltage
	Secondary to Grounded chassis	No requirement provided the secondary voltage is less than 42.4 VAC or 60 VDC
60601-1	Primary to Secondary	4000 VAC, or the equivalent DC voltage
	Primary to Grounded chassis	1500 VAC, or the equivalent DC voltage
	Secondary to Grounded chassis	No requirement provided the secondary voltage is less than 42.4 VAC or 60 VDC

Table 1: Insulation type testing levels

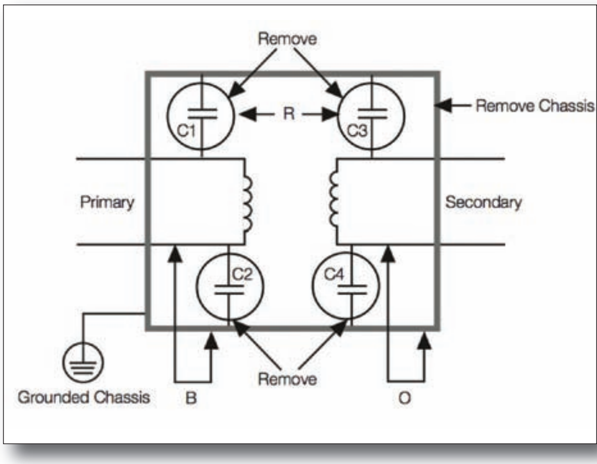


Figure 2: Power supply disassembly may be required for type testing

To properly test reinforced insulation the power supply needs to be removed from the chassis. In addition, all paths to chassis ground, as far as practical, need to be removed so as not to over-stress basic and operational insulation during the test.

This usually entails removal of all Y-capacitors. Figure 2 shows the components that need to be removed.

On many products not all potential paths can be removed. Printed circuit boards may utilize earth traces between primary and secondary while complying with creepage and clearance requirements. In some instances, when applying the primary to secondary hipot voltage, a breakdown or arcing may be observed which can lead to component failure, rendering the power supply inoperable. This is a breakdown of operational insulation (secondary to chassis ground) only. It does not indicate a failure of primary to secondary insulation that is the focus of the test. Provided this 'fails' in a safe manner, the test is considered successful for safety purposes.

Class II power supplies

The previous sections of this document deal with Class I power supplies, which employ a safety earth. In the case of Class II power supplies there is no safety ground and so there is no need, nor ability, to test from primary to earth. Because of the lack of any grounding we also do not have to worry about over stressing any components from the primary to ground, or from the output to ground. The user is able to simply test from the input to the output on the power supply at 3000VAC (or 4121VDC) for ITE devices or 4000VAC (5656VDC) for medical devices to verify the insulation in the supply.

Trends in Medical Power Supplies

Medical electronic equipment is getting smaller. Of course, this could be said of all electronic equipment but it is in the medical area that pressure for size and weight reduction is greatest. Not only is the hospital bedside environment very space-constrained but there is a trend for more equipment to be used in the home, in doctors' offices, and even in cars and on planes. This is creating particular pressure on power supply manufacturers to reduce the size of their products.

In the last 10 years a typical convection-cooled, 100W AC/DC power supply has shrunk from a 4 x 7 inch (10.16cm x 17.78cm) footprint in 1998 to just 2 x 4 inches (5.08cm x 10,16cm) today, a reduction of over 70%. This size reduction has had to be managed carefully. Smaller packages mean less area for heat dissipation, which in turn requires higher efficiency. For example, taking an industry standard footprint of 3 x 5 inches (7.62cm x 12.7cm), convection cooling can effectively remove about 18W of waste heat. Extrapolating from the 20W power loss curve in Figure 1, a 120W power supply needs to be at least 86% efficient for convection cooling to be sufficient.

Figure 1 also shows the dramatic effect that a relatively small improvement in efficiency can have on the available power from a power supply for a given heat dissipation. Taking the 20W power loss curve, an efficiency gain from 88% to 93% would enable an power supply to deliver over 250W rather than around 150W, within a given footprint.

For the power supply designer, size and efficiency are usually the most important trade-offs. Increasing the switching frequency means that smaller components can be used - notably capacitors and inductors. However, switching losses rise and a power supply that may be 92% efficient at 30kHz will be only 83% efficient at 200kHz. Reliability is always of paramount importance in medical applications, so keeping the power system running well within its maximum ratings is always desirable.

The main converter topology is critical to efficiency. For power supplies in the 100W to 200W range, a resonant topology is often chosen. This can virtually eliminate switching losses, enabling smaller heatsinks to be used - so contributing to the dual goals of smaller size and higher efficiency.

In many power supplies, it has become economical to use Silicon Carbide (SiC) diodes in power factor correction circuits. These need no snubber circuits, reducing component count and saving space while giving a typical 1% boost to efficiency.

The falling price of power MOSFETS means that they are now becoming common as the main rectifier of switching power supplies. Efficiency improvements of more than 40% in this part of the circuit are possible. For example, a 20A diode with 0.5V forward voltage dissipates 10W, whereas a MOSFET with an 'ON' resistance of, say, 14mΩ at 100°C dissipates just 5.6W.

Lastly, control circuits have been greatly simplified in recent years, largely through higher integration of semiconductor functions. Application specific chips are now available that can provide the main converter voltage and a host of automatic protection features. Comprehensive monitoring and control signals are also more easily implemented thanks to more highly integrated power management devices.

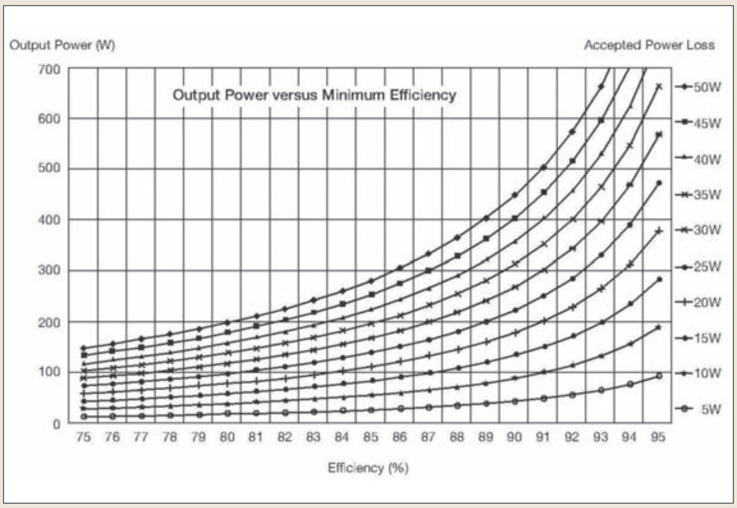


Figure 1: Minimum efficiency required for a given power supply output to ensure compliance with safety standards

Design of a High-Density Power Supply for FPGAs

Although the versatile and configurable nature of Field Programmable Gate Arrays (FPGAs) is attractive to system designers, the complex nature of design rules that govern the inner working of these devices and their outer interface protocols require extensive training, reference design evaluation, design simulation and verification. As a result, FPGA suppliers provide detailed hardware and firmware support to assist system architects with new challenges in the digital domain. However; obscure intricacies in the analog domain, specifically in the realm of delivering power and regulation voltages with DC/DC regulators for core, I/O, memory, clocks, and other rails, demand new solutions. **Alan Chern and Afshin Odabaee, Linear Technology Corp., USA**

To power each rail efficiently and in a smallest possible space requires a DC/DC regulator circuit that contains, on average, 10 components (inductor, MOSFETs, capacitors, DC/DC regulator, etc.). A 6-rail FPGA may require as many as 60 components to power it. Aside from the long list of components needed to power the FPGA, there are hidden costs of component insertion, reliability, circuit board complexity and more.

Managing multiple voltage rails

Prior generations of FPGAs required two or three power rails. Now, some of the high-end multiple-core devices require as many as seven rails; a mixture of 3.3V legacy power rails and recent lower voltages, ranging from 2.8V to 1.0V and below. Moreover, a mix of other voltage rails that are needed for devices other than FPGAs such as memory, network processors, graphics processors, digital-to-analog or analog-to-digital converters as well as op amps and RF ICs.

To ensure a "clean" start-up of a system with multiple voltage rails such that none of the rails conflict with each other requires a DC/DC regulator equipped with sequencing and tracking functions. Simply stated, each regulator must be able to track the output voltage of other regulators. The good news is that FPGAs no longer require any sequencing on their rails. However, sequential ramp-up or ramp-down of several voltages across different sections within a system are still required to prevent possible latch-offs that may occur when a voltage rail comes up too fast or too slow. In the past, tracking and sequencing of power rails was handled by a separate power management IC. Today, designers require that both the sequencing and tracking functions are embedded into the regulators, particularly when they must be located at different corners of the system.

Fast I/O nodes often demand the most power in FPGA-based applications. It's very usual to see 1.8V and 2.5V I/O voltages that create loads in tens of Amperes. The very high-end systems have requirements for 40A up to 80A I/O designs.

Due to the logistics of a board design, the DC/DC regulator must be placed at a distance from its load and requires a long PCB trace from its output to the point of regulation. At large load current levels, PCB traces introduce a voltage error equal to the value of the load current (I) multiplied by the impedance (R) of the trace. This IxR voltage error has become more problematic since the load voltages have been decreasing and load currents increasing. For example, a 200mV IxR drop for a 3.3V rail produces 6% error, whereas for a 1.2V rail it introduces a 17% error. Therefore, although the DC/DC regulator can be set to regulate a 1.2V output, the load will only see 1.0V due to IxR voltage drop.

With today's 90- and 65nanometer processes where Vt and performance of the FPGA are dependent on the precision of supply rails, an error of 17% can easily degrade performance. For example, a 100mV difference in Vt can scale the leakage current by factor of 10 or more.

Standard DC/DC regulators provide precise regulation but only if the load is very close to its output. It cannot compensate for the IxR voltage drop. The error correction must be handled with the help of a remote sense amplifier. The tightest regulation is possible with differential remote sensing of the load, which requires a precision op amp and precision resistors. An ideal regulator should provide better than ±1.5% regulation accuracy right-at-the-load even over -40ºC to 85ºC temperature range. This accuracy may be insignificant for a 3.3V rail where the digital ICs can tolerate ±0.5V variation, but a 90nm or 65nm device with 1.8V, 1.0V or 0.9V rails will require higher accuracy.

Once the output voltage of the regulator is set by the user, the differential remote sensing automatically adjusts the regulated voltage at the point of the load by compensating for any IxR voltage drop across the PCB trace for a wide range of load currents. As a result, the regulation is

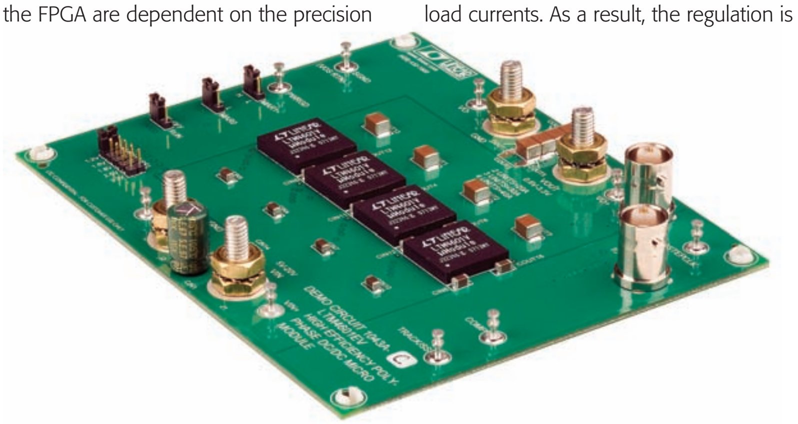
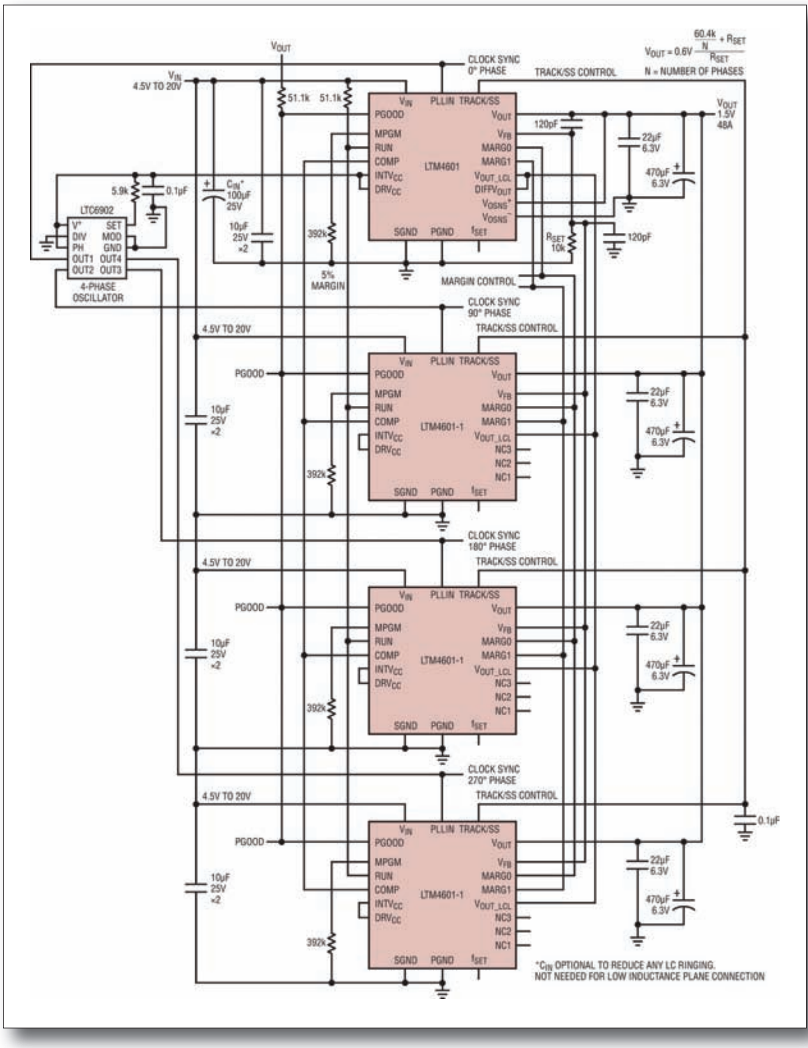


Figure 1: **Four DC/DC µModule regulator systems current share to regulate 1.5V at 48A with only 2.8mm profile and 15mm x 15mm of board area**

Figure 2: Paralleling of multiple DC/DC µModule regulators systems to achieve higher output current



very precise when the system is in standby mode, or at full speed when load current and IxR voltage drop are their peak.

Lowering voltage ripple noise and capacitor requirements

In non-portable applications, as the requirements for voltages drop and currents rise, heat dissipation and operating efficiency become more important factors in the selection of a DC/DC regulator. In portable applications, although load current per rail is less, the operating and standby efficiencies still play an important role in preserving a battery's energy and simplifying thermal management of the portable product.

A switchmode DC/DC regulator offers a higher performance solution than a linear regulator in either portable or non-portable applications, especially for high power requirements. For example, a switchmode regulator providing 1.2V at 5A from a 3.3V input supply at 90% efficiency compares to a linear regulator's 36% efficiency; furthermore, whereas the switchmode regulator dissipates 0.7W, the linear regulator dissipates 10.5W.

On the other hand, a switchmode regulator introduces switching noise and higher output ripple noise (output voltage peak-to-peak ripple) because of its inherent switching operation. Unfortunately, the lower voltage rails of new FPGAs and tighter eye-diagrams of faster I/O signals are less tolerant of power supply "noise".

To alleviate the ripple noise, more input and output capacitors can be added to the circuit to dampen peak-to-peak ripple voltage. However, dampening the switching noise is more challenging. One possible approach is to synchronize the DC/DC regulator's operating frequency to an external clock which forces the regulator to operate within a set frequency chosen to have minimum interference with other noise-sensitive parts of the system. This method is especially effective when several switchmode regulators are all synchronized to a clock frequency that is safe for the rest of the system.

These methods help with design of a less noisy switchmode point-of-load regulator; however the problem of noise can be greatly reduced if the DC/DC regulator is designed from the ground up with the proper architecture, functions and layout. Such a regulator minimizes its dependency on capacitors, filtering, and EMI (electromagnetic interference) shielding.

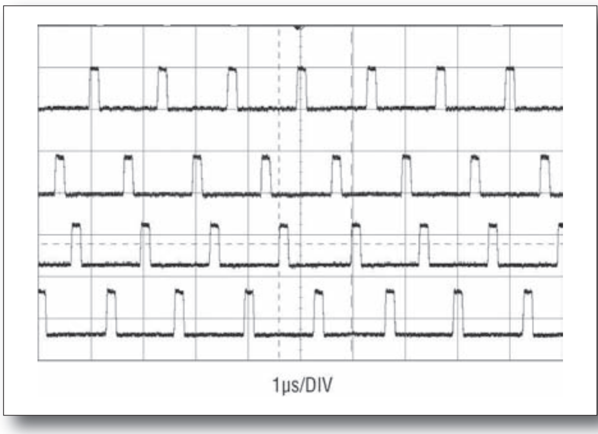


Figure 3: By operating each DC/DC µModule regulator 90° out-of-phase, the input and output ripples are reduced, which also reduces the requirement for input and output capacitors (shown are individual µModule switching waveforms for Figure 2)

Fine tuning voltages during system qualification and assembly

The performance of an FPGA or its supporting ICs can differ when they are assembled into a complete system versus when they are individually tested on a lab bench. Elements such as the type of solder, temperature, PCB layout, trace impedances and assembly process influence the performance of a component. For example, if the core of the FPGA is regulated at a voltage other than expected and this leads into a slower speed, the system's computational capability will be degraded. In some instances, the quality control personnel must reject a system that deviates from its expected performance.

For this reason, as engineers evaluate the performance during qualification or assembly, they need the ability to raise or lower the output voltage in small increments. This function is called margining. In the previous example, the core voltage could be increased so that the operating frequency of the FPGA reaches its desired level. The margining function can also help the system manufacturer increase the overall yield during production.

In a recent application discussion with a system designer, the requirement for his power supply was to regulate 1.5V and deliver up to 40A of current to a load that consisted of four FPGAs. This means that up to 60W of power must be delivered in a small area with lowest profile (height) possible to allow smooth flow of air for cooling. The power supply had to be surface-mountable and operate at high enough efficiency to minimize heat

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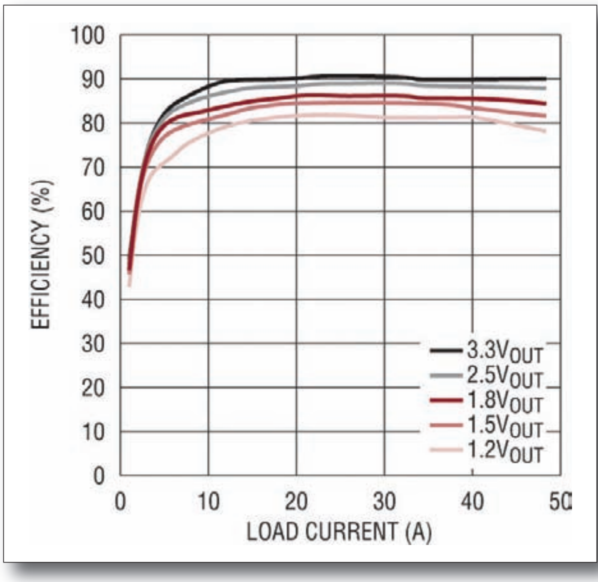


Figure 4: Efficiency of the four DC/DC µModule regulators in parallel remains high over a wide range of output voltages

dissipation. He also demanded the simplest possible solution so his time could be dedicated to the more complex tasks. Aside from precise electrical performance, this solution had to remove the heat generated during DC to DC conversion quickly so that the circuit and the ICs in its vicinity did not over heat. Such solution requires an innovative design to meet these criteria such as very low profile to allow efficient air flow and to prevent thermal shadow on surrounding ICs; high efficiency to minimize heat dissipation; current sharing capability to spread the heat evenly to eliminate hot spots and minimize or eliminate the need for heat sinks; and a complete DC/DC circuit in a surface mount package that includes the DC/DC controller, MOSFETs, inductor, capacitors and compensation circuitry for a quick and easy solution.

Innovation in DC/DC design

The innovation is a modular but surface mount approach that uses efficient DC/DC conversion, precise current sharing and low thermal impedance packaging to deliver the output power while requiring minimal cooling. Because of the low profile and power sharing among four devices, a system using this solution depends on fewer fans or slower fan speed as well as minimal or no heat sinks. These contribute to a lower cost system that consumes less power to remove heat.

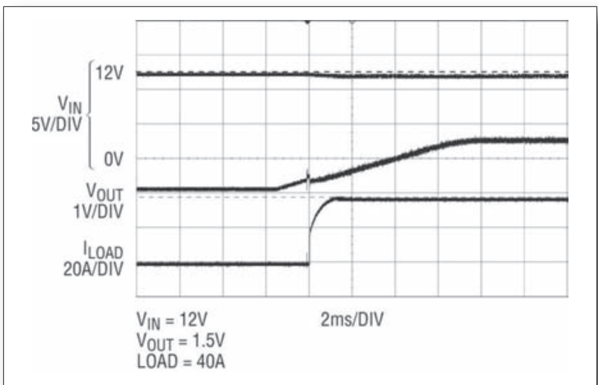
Figure 1 shows a test board for such circuit. The design regulates 1.5V output while delivering 40A (up to 48A) of load current. Each "black square" is a complete DC/DC circuit and is housed in a 15mm x 15mm x 2.8mm surface mount package. With a few input and output capacitors and resistors, the design using these DC/DC µModules is as simple as shown.

The LTM4601 µModule DC/DC regulator is a high performance power module shrunk down to an IC form factor. It is a completely integrated solution, including the PWM controller, inductor, input and output capacitors, low RDS(ON) FETs, Schottky diodes and compensation circuitry. Only external bulk input and output capacitors and one resistor are needed to set the output from 0.6V to 5V. The supply can produce 12A (more if paralleled) from a wide input range of 4.5V to 20V. The pin-compatible LTM4601HV extends the input range to 28V.

A significant advantage of the LTM4601 over power-module or IC-based systems is its ability to easily scale up as loads increase. If load requirements are greater than one µModule regulator can produce, simply add more modules in parallel. The design of a parallel system involves little more than copying and pasting the layout of each 15mm _ 15mm µModule regulator. Electrical layout issues are taken care of within the µModule package, there are no external inductors, switches or other components to worry about.

Output features include output voltage tracking and margining. The switching frequency, typically 850kHz at full load, constant on time, zero latency controller delivers fast transient response to line and load changes while maintaining stability. Should frequency harmonics be a concern, an external clock can control synchronization via an on-chip phase lock loop.

Figure 5: Controlled soft start is important in proper start-up of the FPGA or the system as a whole (soft-start current and voltage ramp for four DC/DC µModules in parallel)



Four parallel regulators provide 48A

Figure 2 shows a regulator comprising four parallel LTM4601s, which can produce a 48A (4 _12A) output. The regulators are synchronized but operate 90° out of phase with respect to each other, thereby reducing the amplitude of input and output ripple currents through cancellation (Figure 3). The attenuated ripple in turn decreases the external capacitor RMS current rating and size requirements, further reducing solution cost and board space.

Synchronization and phase shifting is implemented via the LTC6902 oscillator, which provides four clock outputs, each 90° phase shifted (for 2- or 3phase relationships, the LTC6902 can be adjusted via a resistor). By operating the regulators out-of-phase, peak input and output current is reduced by approximately 20% depending on the duty cycle (see the LTM4601 data sheet). This reduction in turn, reduces the requirement for input and output capacitors. The clock signals serve as input to the PLLIN (phase-lock loop in) pins of the four LTM4601s. The phase-lock loop of the LTM4601 comprises a phase detector and a voltage controlled oscillator, which combine to lock onto the rising edge of an external clock with a frequency range of 850kHz. The phase lock loop is turned on when a pulse of at least 400ns and 2V amplitude at the PLLIN pin is detected, though it is disabled during start-up. Figure 3 shows the switching waveforms of four LTM4601 regulators in parallel.

Only one resistor is required to set the output voltage. In a parallel setup, the value of the resistor depends on the number of LTM4601s used. This is because the effective value of the top (internal) feedback resistor changes as you parallel LTM4601s. The LTM4601's reference voltage is 0.6V and its internal top feedback resistor value is 60.4kΩ, so the relationship between V_{OUT}, the output voltage setting resistor (R_{FB}) and the number of modules (n) placed in parallel is according to equation 1:

$$V_{OUT} = 0.6V \frac{\frac{60.4k}{n} + R_{FB}}{R_{FB}} \quad (1)$$

η is the number of paralleled modules.

Figure 4 illustrates the system's high efficiency over the vast output current range up to 48A. The system performs impressively with no dip in the efficiency curve for a broad range of output voltages.

Soft-Start and Current Sharing

The soft-start feature of the LTM4601 prevents large inrush currents at start-up by slowly ramping the output voltage to its nominal value. The relation of start-up time to VOUT and the soft-start capacitor (C_{SS}) according to equation 2 is:

$$V_{OUT(MARGIN)} = \frac{\%V_{OUT}}{100} \bullet V_{OUT}$$

$$t_{SOFTSTART} = 0.8 \bullet \left(0.6V - V_{OUT(MARGIN)}\right) \bullet \frac{C_{SS}}{1.5\mu A} \quad (2)$$

For example, a 0.1µF soft-start capacitor yields a nominal 8ms ramp (see Figure 5)

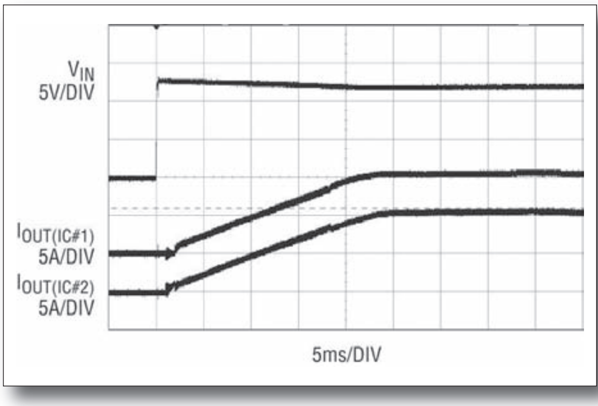


Figure 6: Each DC/DC µModule regulator starts and ends by sharing the load current evenly and balanced, a crucial feature to prevent one regulator from overheating (two parallel LTM4601s, as each rises to a nominal 10A each, 20A total)

with no margining.

Current sharing among parallel regulators is well balanced through start-up to full load. Figure 6 shows an evenly distributed output current curve for a 2-parallel LTM4601 system, as each rises to a nominal 10A each, 20A total.

In summary, the DC/DC µModule regulators are self-contained and complete systems in an IC form factor. The low profile, high efficiency and current sharing capability allow practical high power solutions for the new generation of digital systems. Thermal performance is impressive at 48A of output current with balanced current sharing and smooth uniform start-up. The ease and simplicity of this design minimizes development time while saving board space.

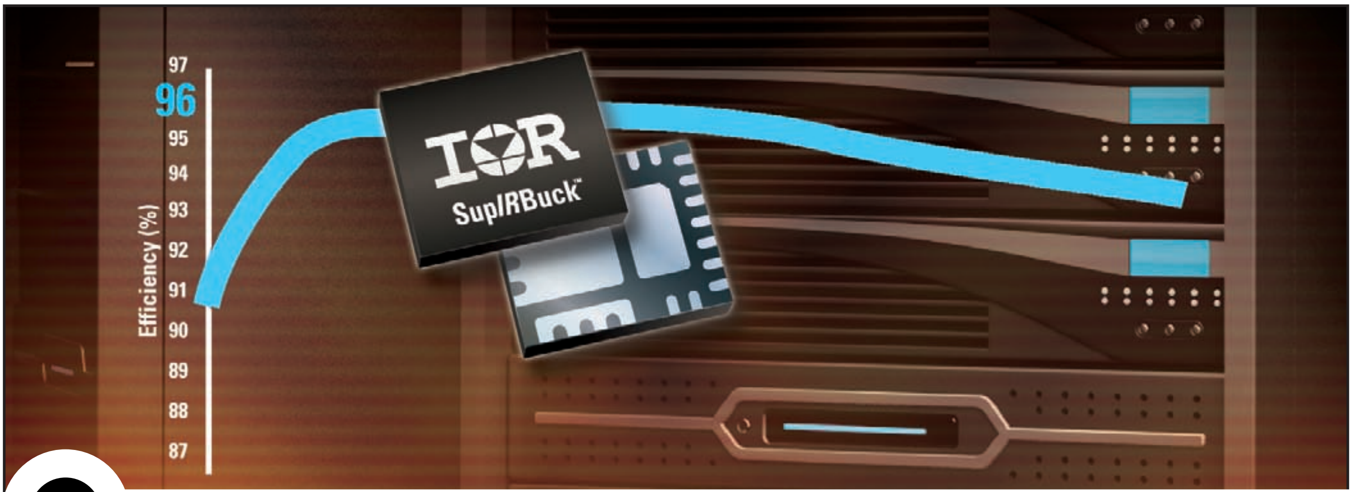
Thermal performance and layout

In the first portion of this article, we discussed the circuit and electrical performance of a compact and low profile 48A, 1.5V DC/DC regulator solution for a 4-FPGA design. The new approach uses four DC/DC regulators in parallel (Figure 1) to increase output current while sharing the current equally among each device. This solution relies on the accurate current sharing of these regulators to prevent hot-spots by dissipating the heat evenly over a compact surface area.

The move to shrink the size of FPGA-based systems while increasing functionality, memory storage and computational power, have prompted designers to refine the techniques used to cool the components. One simple method is to provide an efficient air flow over the components. Tall components obscure the flow over the thinner packages such FPGAs or a memory ICs. In the case of pre-fabricated DC/DC point-of-load regulators, the blockage is severe as these devices reach a height that is between 6 to 10 times the height of the FPGA and other ICs.

The thin ball grid array (BGA) packaging of the FPGAs is extremely helpful in efficient dissipation of internally generated heat from the top of the package. This benefit is diminished when a taller device such as a pre-fabricated DC/DC regulator inhibits air flow and casts a "shadow" on the device next to it.

Figure 7 is a thermal image of the board shown in Figure 1 with readings of the temperatures at specific locations. Cursors 1 to 4 show an estimation of the surface temperature on each module. Cursors 5 to 7 indicate the surface temperature of the PCB. Note the difference in temperature between the inner two regulators, cursors 1 and 2, and the outside ones, cursors 3 and 4. The LTM4601 µModule regulators placed on the outside have large planes to the left and right promoting heat sinking to cool the part down a few degrees. The inner two only have small top and bottom planes to draw heat away, thus becoming slightly warmer than the outside two.



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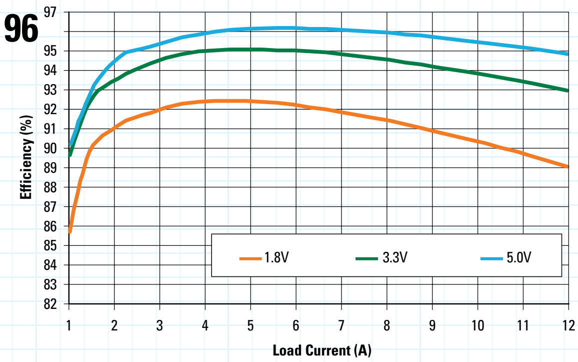

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Part Number	Package	Input Voltage	Maximum Current	Maximum Frequency	Additional Features
IR3843WM	5x6 PQFN	1.5V to 16V	2A	1.5MHz	OV detection, Sequencing
IR3842WM	5x6 PQFN	1.5V to 16V	4A	1.5MHz	OV detection, Sequencing
IR3841WM	5x6 PQFN	1.5V to 16V	8A	1.5MHz	OV detection, Sequencing
IR3840WM	5x6 PQFN	1.5V to 16V	12A	1.5MHz	OV detection, Sequencing
IR3832WM	5x6 PQFN	1.5V to 16V	4A	1.5MHz	OV detection, DDR tracking
IR3831WM	5x6 PQFN	1.5V to 16V	8A	1.5MHz	OV detection, DDR tracking

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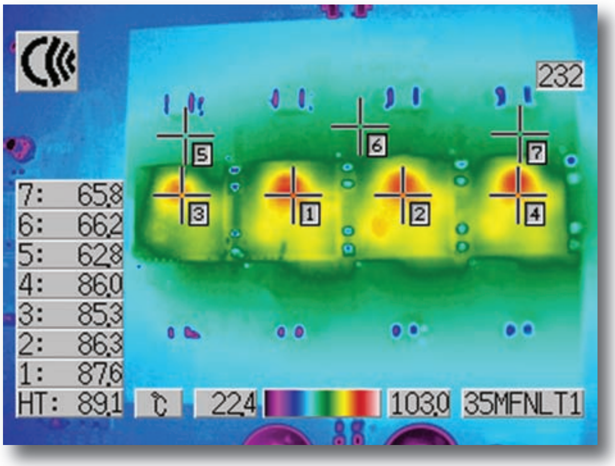


Figure 7: Thermograph of 48A, 1.5V circuit of Figure 1 shows balanced power sharing among each DC/DC µModule regulator and low temperature rise even without airflow (V_{IN}=20V to 1.5V_{OUT} at 40A)

Airflow also has a substantial effect on the thermal balance of the system. Note the difference in temperature between Figures 2 and 3. In Figure 7, a 200LFM airflow travels evenly from the bottom to the top of the demo board, causing a 20°C drop across the board compared to the no air flow case in Figure 7.

The direction of airflow is also important. In Figure 4 the airflow travels from right to left, pushing the heat from one regulator to the next, creating a stacking effect. The device on the right, the closest to the airflow source, is the coolest. The leftmost regulator has a slightly higher temperature because of spillover heat from the other regulators. Heat transfer to the PCB also changes with airflow.

Simple copy and paste layout

Further heat dissipation is possible by adding vias underneath the part. Vias provide a path to the power planes and into the PCB, which helps draw heat away. Vias should not be placed directly under the pads. Figure 6 shows the layout of the vias on the DC1043A demonstration circuit. The cross marks indicate the vias in between the LGA pads.

Layout of the parallel regulators is relatively simple, in that there are few electrical design considerations. Nevertheless, if the intent of a design is to minimize the required PCB area, thermal considerations become paramount, so the important parameters are spacing, vias, airflow and planes.

The LTM4601 regulator has a unique LGA package footprint, which allows solid attachment to the PCB while enhancing thermal heat sinking. The footprint itself simplifies layout of the power and ground planes, as shown in Figure 7. Laying out four parallel regulators is just as easy. If laid out properly, the LGA packaging and the power planes alone can provide enough heat sinking to keep the LTM4601 cool.

Conclusions

Delivering 60W of power in a compact space without efficient means to remove the heat from the power supply exacerbates the already challenging task of system heat management and cooling. The DC/DC µModule family is designed with careful attention to the layout of its internal components, package type, and electrical operation, which ease thermal management of a very dense power supply circuit. The LGA package and simple layout allow 100% surface mountable and low profile design for maximum efficiency in air flow. This new approach in power supply design takes advantage of paralleling multiple DC/DC µModule regulators and following a copy & paste approach in layout design, to provide a 60W power supply with minimum components while operating efficiently in a compact, low profile space.

Integrated FETs for Power over Ethernet

Power over Ethernet (PoE) Power Sourcing Equipment (PSE) controllers use high-voltage, high-current FETs for connecting the power source to the load. Integrating the FET reduces the space required to implement the PSE subsystem and also reduces component count. This article explains the precautions that must be taken with integrated FETs using the recently introduced Silicon Labs Si3452 PoE controller as an example.

John Gammel, PoE Applications Manager, Silicon Labs, Austin, USA

This controller supports four independent PoE (IEEE 802.3af) and PoE+ (IEEE 802.3at) PSE ports, offers real-time power measurement capabilities, energy-efficient powered device (PD) detection and disconnect algorithms, and low on-resistance power FETs and sense resistors. These features enable smaller, highly energy-efficient and lower-cost PoE/PoE+ Ethernet switches and midspans designed to power multi-radio wireless access points, industrial automation systems, VoIP phones, and building security and surveillance systems.

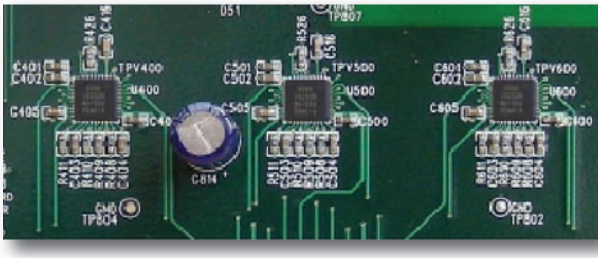


Figure 1: 12 PoE Ports with Si3452 (no backside components)

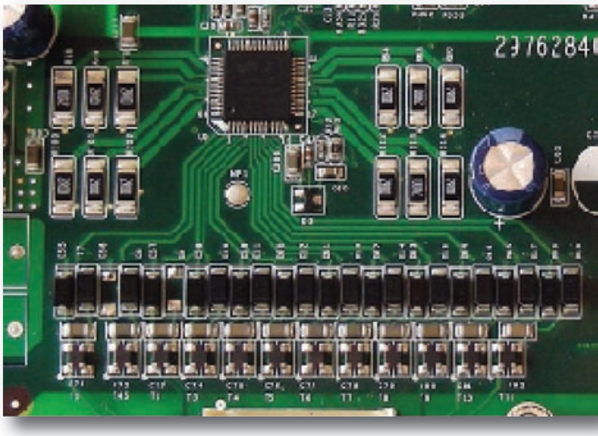


Figure 2: Representative layout of 12 ports without integrated FETs (FETs are on the backside, photo is to same scale as Figure 1)

FET current carrying requirements

With a standard TO-223 FET package and two 0805 resistors for current sensing, the external FETs use about 50mm^2 of package area per port. When the controller size is added, the package area per port is approximately 70mm^2 compared to less than 20mm^2 for a typical PoE controller with integrated FETs. Figures 1 and 2 show representative layouts for 12 port comparing the Si3452 with integrated FETs to a 12 port solution without the integrated FETs.

Some other advantages of FET integration are higher reliability due to lower component count and interconnections and guaranteed coordination with the PoE controller fault protection and current limit. When the FET is integrated, the current sense resistor is also typically integrated, which reduces noise and offset effects and typically allows the use of smaller sense resistors for less current sensing power loss. While the advantages of using the integrated FET are compelling, the reduced size means more care must be taken to avoid heating in both normal and transient conditions.

Until recently, the required power level for PoE PSE was 15.4 W. The recently adopted 802.3at amendment to the IEEE standard increases the power level to 30W for "Type 2 circuits" (cat 5E or better cable). The requirements for DC and transient current limit performance as well as typical current limits are shown in Table 1.

As can be seen, the FET must be capable of handing high DC current and high transient power conditions. These are addressed below.

DC current levels

When using integrated FETs, some care is required because, typically, four or more ports can be supported on one IC; so, I^2R losses from all ports combine.

For example, the Si3452 4 port PoE controller has a maximum combined FET and current sense resistance of 0.6Ω. In a worst-case situation, with all four ports carrying 600mA, the power dissipated is 1.2W (including V_{dd} and V_{ee} consumption). The Si3452 is packaged in a 6x6 mm QFN

Port	Power level	Voltage	Maximum DC current	Minimum current limit	Minimum current limit time	Typical current limit	Typical current limit time
Type 2	30W	50-57V	600mA	686mA	10ms	800mA	15ms
Type 1	15.4W	44-57V	350mA	400mA	50ms	425mA	60ms

Table 1: FET current carrying requirements

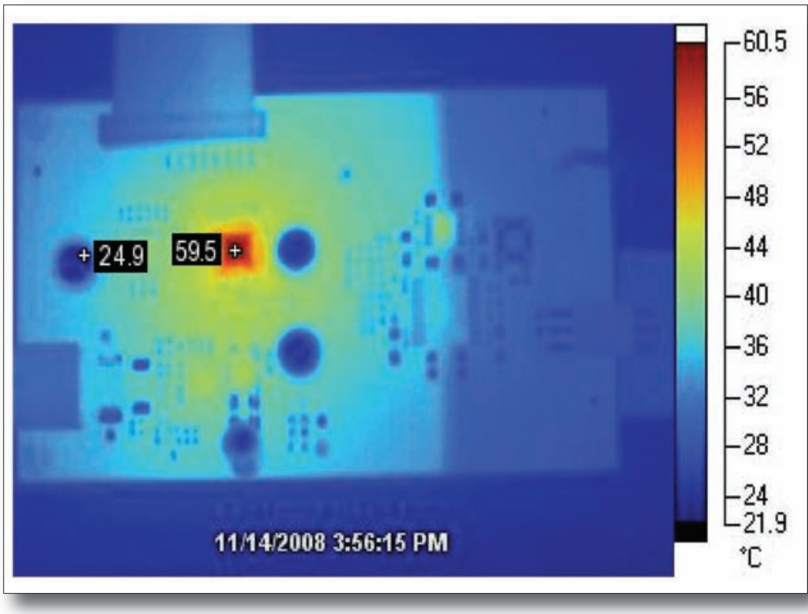


Figure 3: Measured thermal rise of Si3452 with four ports carrying 600mA

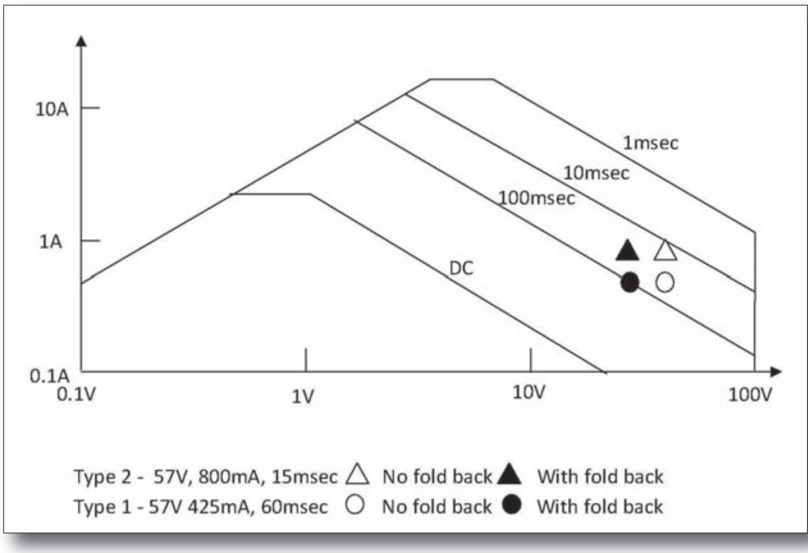


Figure 4: Typical FET SOA curves

with exposed pad. To dissipate this amount of heat, it is recommended that the exposed pad be connected by 25 vias to a heat spreading layer on the back of the PCB with at least 1inch^2 of copper per IC. With the recommended layout, the thermal impedance is 32°C/W with no airflow, and the worst case rise is less than 40°C. The Si3452 is rated for a junction temperature of 125°C; so, operation of 85°C is possible even without forced air cooling. Figure 3 shows the measured 34.6°C thermal rise of a Si3452 with four ports carrying the worst-case 600mA.

Transient conditions

The FET must be protected against faults and start-up transient conditions. Normally, the FET source is connected by a current sense resistor to a V_{ee} supply of as much as -57V, and the drain is clamped to ground; so, the worst case fault causes 57V of drain voltage on the FET while it is in the on state.

When using an external FET, is it not practical for the controller IC to measure the FET temperature for protection; so, the FET current limit and overload timing (TICUT) must be adjusted to fall within the safe operating area (SOA) of the FET (see Figure 4).

As can be seen, the required current limit and time is very close to the transistor SOA; so, a special technique, referred to as foldback current limiting, is employed. With the fold back current limit approach, the current limit is reduced as the FET drain voltage increases above a certain level (typically 25 V).

With the integrated FETs, it is possible to put thermal sensors close to the FET. The circuitry is arranged to turn off the FET if the thermal sensors activate, providing an additional level of safety against FET damage from fault conditions. Typically, these techniques are combined, resulting in the integrated FET being better protected against fault conditions despite the small size.

A concern with this approach is that a fault on one port might cause a thermal overload indication on another port. This is avoided by having the thermal sensors near each FET so that severe overloads are detected on a per-port basis. Overloads that are not as severe are protected by monitoring port current and shutting the port off after the required time. Combining these approaches prevents a fault on one port from affecting other ports.

Conclusion

Table 2 summarizes the issues with integrating FETs in PoE PSE controllers and the techniques for dealing with these issues in integrated FET controllers. By using the techniques described above, FETs can be safely integrated into PoE PSE controllers allowing significant savings in cost, component count and required PCB area.

Issue	Technique required
I^2R heating due to DC current on multiple ports	Use exposed pad package with multiple vias to a heat spreading plane
High current transients	Voltage foldback of current limit and thermal sensors for added safety
Faults on one port might affect another port	Place thermal sensors near FET. Monitor port current and shut port down if it is overloaded

Table 2: Summary of issues with integrating FETs in PoE PSE controllers

High-temperature Power MOSFETs

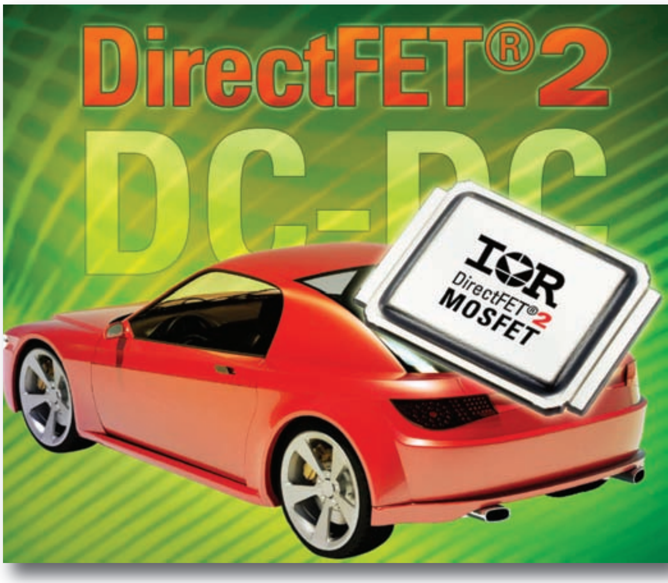
MSC expands its product portfolio with seven new N- and P-channel power MOSFETs in space-saving 8-pin HSON packages. These power MOSFETs from Renesas Electronics for breakdown voltages of 40, 60 or -30 V can switch currents up to 75A, are specified up to 175°C channel temperature and are qualified to AEC-Q101. Furthermore, the devices feature a low channel-to-case thermal resistance - e.g. 1.09°C/W with the NP75N04YUG power MOSFET - and a low on-resistance of maximum 4.8mΩ. Approximately only half the size of comparable performance power MOSFETs in conventional TO-252 package, the new members of the NP series are suitable for use in high-temperature environments such as for the control of direct injection in the engine compartment of a vehicle, control of electrical motor pumps, for controlling solenoid valves or as protection against reverse-battery connections.

www.msc-ge.com

Automotive Power MOSFETs for Switching Applications

International Rectifier has launched two automotive DirectFET2 power MOSFETs optimized with low gate charge for switching applications including Switch Mode Power Supplies (SMPS), Class D Audio systems or High Intensity Discharge (HID) lighting. The AUIRF7648M2 and AUIRF7669L2, IR's first automotive grade DirectFET devices tailored to DC/DC applications, offer low gate charge and on-state resistance to help minimize switching and conduction losses in a variety of switching applications. Moreover, the low parasitic inductance offered by the DirectFET power package results in excellent high frequency switching performance with reduced waveform ringing which in turn helps limit EMI and filter size. The AUIRF7648M2 features a PCB footprint 54% smaller than a DPak while the AUIRF7669L2 features a PCB footprint 60% smaller than a D2Pak. With package current ratings of 179A and 375A respectively for each device, the DirectFET package places no constraint on current capability of the silicon. Moreover, the maximum package current ratings far exceed the limits of traditional DPak and D2Pak packages. The devices are qualified according to AEC-Q101 standards, feature a lead-free and RoHS compliant bill of materials, and are part of IR's automotive quality initiative targeting zero defects.

www.irf.com



Isolated Gate Drivers for IGBTs

Avago now offers the 2.5 A peak-output drive ACPL-H342 and ACPL-K342 optically isolated IGBT gate drivers that feature a built-in Miller clamp, Rail-to-Rail output voltage, under-voltage lockout (UVLO) circuitry and protection against IGBT cross-conduction and current "shoot-through" for safe and efficient power inverter and motor control applications.

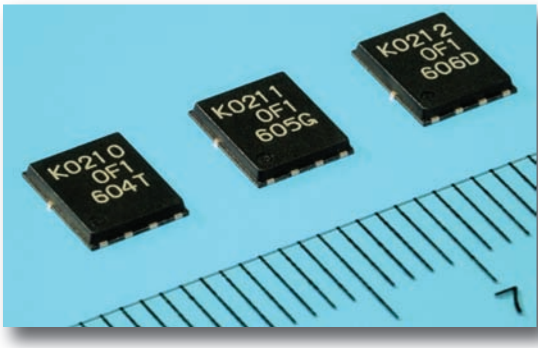
A Miller clamp allows the control of the Miller current during high dV/dt output transition. It can also eliminate the need for a negative power supply to ensure safe IGBT turn off by quickly discharging the IGBT's large gate capacitance to a low level without affecting the IGBT turn-off characteristics.

The UVLO function causes the output to be clamped whenever there is insufficient power supply voltage for safe operation. The circuitry ensures that there is sufficient gate drive voltage to switch the IGBTs completely on, therefore minimizing IGBT power dissipation. Once the supply voltage exceeds the positive-going UVLO threshold, the UVLO clamp is released, allowing the device output to turn on in response to an input signal. Efficiency has been a key design goal of the new ACPL-H342 and ACPL-K342 gate drives. Their rail-to-rail output voltage swing and the low output dead time, made possible by low propagation time, minimize driver dissipation and increase efficiency. Propagation delay is specified to prevent cross conduction of the IGBTs in the high- and low-side half-bridge IGBT configuration that is commonly used in power inverters. Propagation delay difference between two devices is -10ns minimum to -200ns maximum. Hence, shoot through is prevented, thus eliminating a major condition that can cause IGBT damage and shorten operating life.

www.avagotech.com

Power MOSFETs for High-Efficiency DC/DC Converters

Renesas announced the availability of its new 12th-generation power MOSFET products, the RJK0210DPA, RJK0211DPA, and RJK0212DPA, for DC/DC converters used in applications such as general point-of-load, base stations, computer servers and notebook PCs. The new power MOSFETs can be used as a step-down circuit for converting the 12V voltage supplied by a battery to 1.05V for use by the CPU. Further refinements to the manufacturing process allow to achieve approximately 40% lower FOM compared to the company's existing products, which contribute to reduction of power losses. The new products achieve maximum current of 40A for the RJK0210DPA MOSFET, 30A for the RJK0211DPA device, and 25A for the RJK0212DPA device.

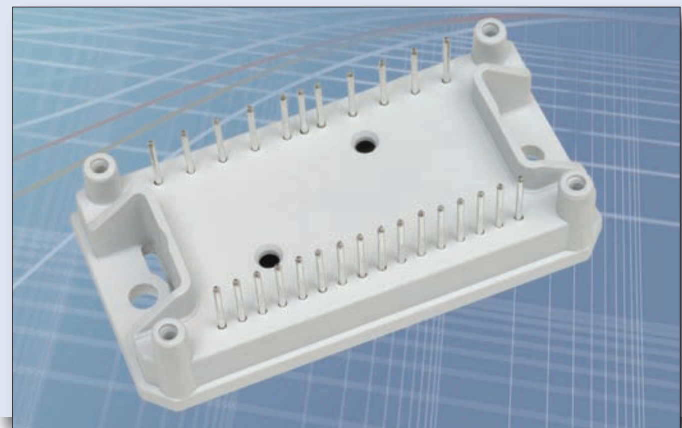


www.renesas.eu

IPM with Integrated Driver and Shunt

Vincotech's flowIPM integrates the inverter, rectifier, and entire driver circuit so there is no need for additional external components. Integrated shunts add highly precise current sensing to the inverter's capabilities. The flowIPM is used most frequently for applications such as motor driver circuits with up to 1kW output power. It is an optimum solution for mechanical environments where space is tight, for example, embedded motor drives for fans, pumps, washing machines, and small industrial motor drives. The family comprises four types, 4A and 10A versions are available for the inverter section. The module comes in a 17mm high flow 1B housing measuring 72mm by 36mm. Other options such as press-fit technology and phase-change material are also available on demand.

www.vincotech.com/en/products/power/flowIPM_1B



MOSFET with SiC Diode in Isolated Package

Ixys announced the integration of Silicon Carbide (SiC) technology and the latest super junction MOSFET technology into a single package enabling increased power density and higher efficiency in fast switching power supplies and solar inverter applications. The MKE range integrates these technologies into one part thereby reducing parasitic inductance and its associated losses, whereas the The ISOPLUS technology gives the designer a discrete package with ceramic, Direct Copper Bonded (DCB) isolation. This isolation has low thermal impedance and a higher reliability in power cycling than standard copper based solutions and non-isolated products. An example of this technology is the MKE11R600DCGFC which integrates a 600V, SJ MOSFET and a 12A/600V SiC diode in boost chopper circuit topology which is a common combination for Power Factor Correction (PFC) stages in high frequency switching applications. Because of the absence of minority carrier injection of SiC there is no reverse recovery of the boosting diode. This provides the highest efficiency with very low switching losses. The use of ISOPLUS packaging allows a mounting of MOSFET and boost diode very close together thereby minimizing stray inductance. Layout is designed to be user friendly as the gate and source connections are located side by side and are easily accessible.

www.ixys.com

1.8A Dual Point-of-Load Regulator

Semtech's SC283 is the smallest 1.8A dual-channel regulator for point-of-load (POL) applications, combining two step-down regulators in an ultra-small, low-profile 2mm x 3mm x 0.8mm, 18-pad MLPQ package. With integrated VID pins to enable independent configuration and control of the output voltages of each regulator, the SC283 eliminates the need for two pairs of external feedback resistors. The regulator operates at a fixed switching frequency of 2.5MHz enabling it to work with very small chip inductors, providing an 111mm^2 footprint. The SC283 supports output currents up to 1.8A per channel, along with very high power conversion efficiency (up to 94%), low shutdown current (1µA typ.) and excellent transient response for fast system wake-up from low-power standby mode to full-power operation. The SC283 offers full protection features, including internal soft start to minimize inrush current, input under-voltage lockout, output over-voltage and current-limit protection, and over-temperature protection. For applications requiring just one regulator, the SC183C offers the same performance, with a single output.

www.semtech.com

36V/200mA LDO

Texas Instruments announced a new low dropout regulator for -36V applications. The TPS7A30, paired with the positive voltage TPS7A49, provides designers with a total solution for powering precision analog applications. The devices feature ultra-high power supply rejection ratio performance and as low as 16µVrms of output noise. The TPS7A30 generates 200mA, while the TPS7A49 manages 150mA. The TPS7A30/TPS7A49 linear regulator family is stable with any output capacitance greater than 2.2µF. The LDOs come in an adjustable version with an output voltage ranging from 1.22V to 34V. The LDOs are designed for noise-sensitive applications, such as test equipment; industrial, networking and telecom equipment; base stations; microwave and radio links; noise filtering for receive, transmit and power amplifiers; and medical applications.

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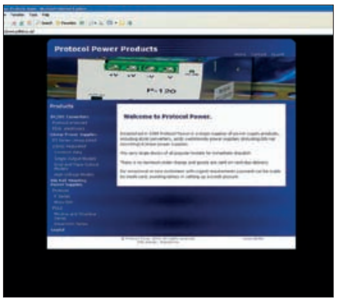

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Laird Technologies Ltd
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Mark 5 Ltd
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Voltage References

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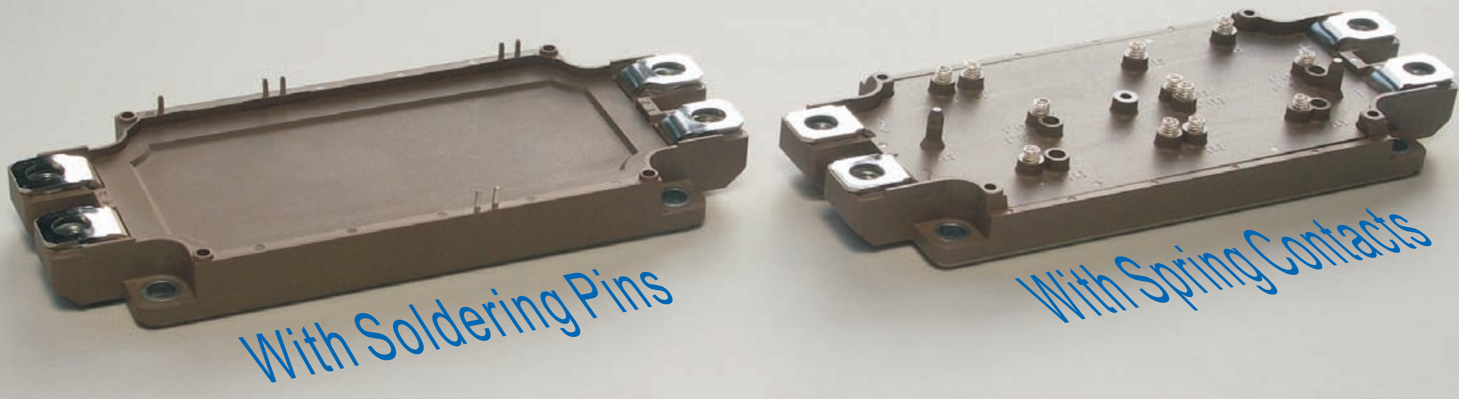
Dual-PACK IGBTs



We never sell a product alone
It always comes with Quality

Voltage & current range

I_C	1200V	1700V
225A	●	●
300A	●	●
450A	●	●
600A	●	

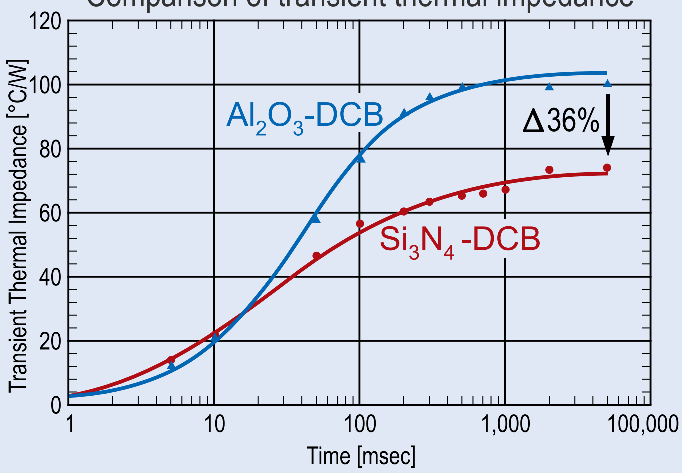
↓ SiN-DCB & thicker Cu pattern

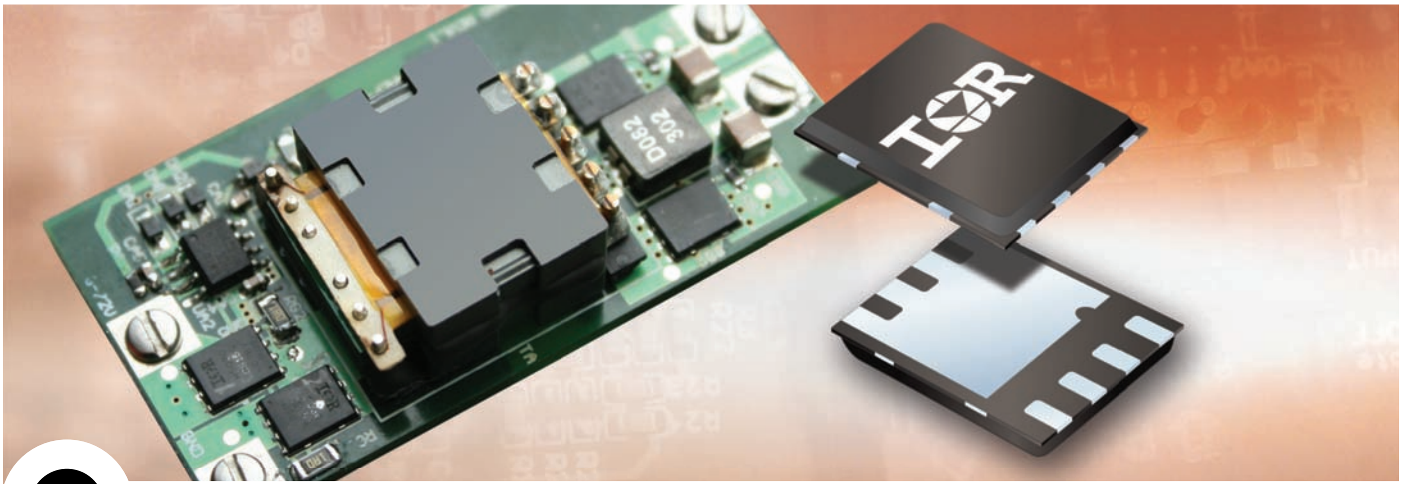
↓ Lower thermal impedance
Higher bending strength & fracture toughness

↓ Higher thermal cycling capability
Higher reliability

- $T_{j(op)}$ = 150°C continuous operation
- $T_{j(max)}$ = 175°C
- New solder material for higher reliability
- Low switching losses & low over voltage spike

Comparison of transient thermal impedance





Introducing 40 V – 250 V MOSFETs in High Current Package

Offering Optimized Performance and Cost for a Given Application

Standard Gate Drive

Part Number	Package	Voltage	Current	$R_{DS(on)}$ Max. @10V	Q_G Typ @10V
IRFH5004TRPBF	PQFN 5x6mm	40 V	100A	2.6 mΩ	73 nC
IRFH5006TRPBF	PQFN 5x6mm	60 V	100A	4.1 mΩ	67 nC
IRFH5106TRPBF	PQFN 5x6mm	60 V	100A	5.6 mΩ	50 nC
IRFH5206TRPBF	PQFN 5x6mm	60 V	98A	6.7 mΩ	40 nC
IRFH5406TRPBF	PQFN 5x6mm	60 V	40A	14.4 mΩ	23 nC
IRFH5007TRPBF	PQFN 5x6mm	75 V	100A	5.9 mΩ	65 nC
IRFH5207TRPBF	PQFN 5x6mm	75 V	71A	9.6 mΩ	39 nC
IRFH5010TRPBF	PQFN 5x6mm	100 V	100A	9.0 mΩ	65 nC
IRFH5110TRPBF	PQFN 5x6mm	100 V	63A	12.4 mΩ	48 nC
IRFH5210TRPBF	PQFN 5x6mm	100 V	55A	14.9 mΩ	39 nC
IRFH5015TRPBF	PQFN 5x6mm	150 V	56A	31 mΩ	33 nC
IRFH5020TRPBF	PQFN 5x6mm	200 V	41A	59 mΩ	36 nC
IRFH5025TRPBF	PQFN 5x6mm	250 V	32A	100 mΩ	37 nC

Logic Level Gate Drive

Part Number	Package	Voltage	Current	$R_{DS(on)}$ Max. @4.5V	Q_G Typ @4.5V
IRLH5034TRPBF	PQFN 5x6mm	40 V	100A	2.4 mΩ	43 nC
IRLH5036TRPBF	PQFN 5x6mm	60 V	100A	4.4 mΩ	44 nC
IRLH5030TRPBF	PQFN 5x6mm	100 V	100A	9.0 mΩ	44 nC

Features

- Low thermal resistance to PCB (down to <0.5°C/W)
- High Current Package – up to 100A continuous
- 100% RG tested
- Low profile (<0.9 mm)
- Industry-standard pinout
- Compatible with existing surface mount techniques
- RoHS compliant containing no lead, no bromide and no halogen
- MSL1, industrial qualification

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- Increased power density
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