POWER ELECTRONICS EUROPE

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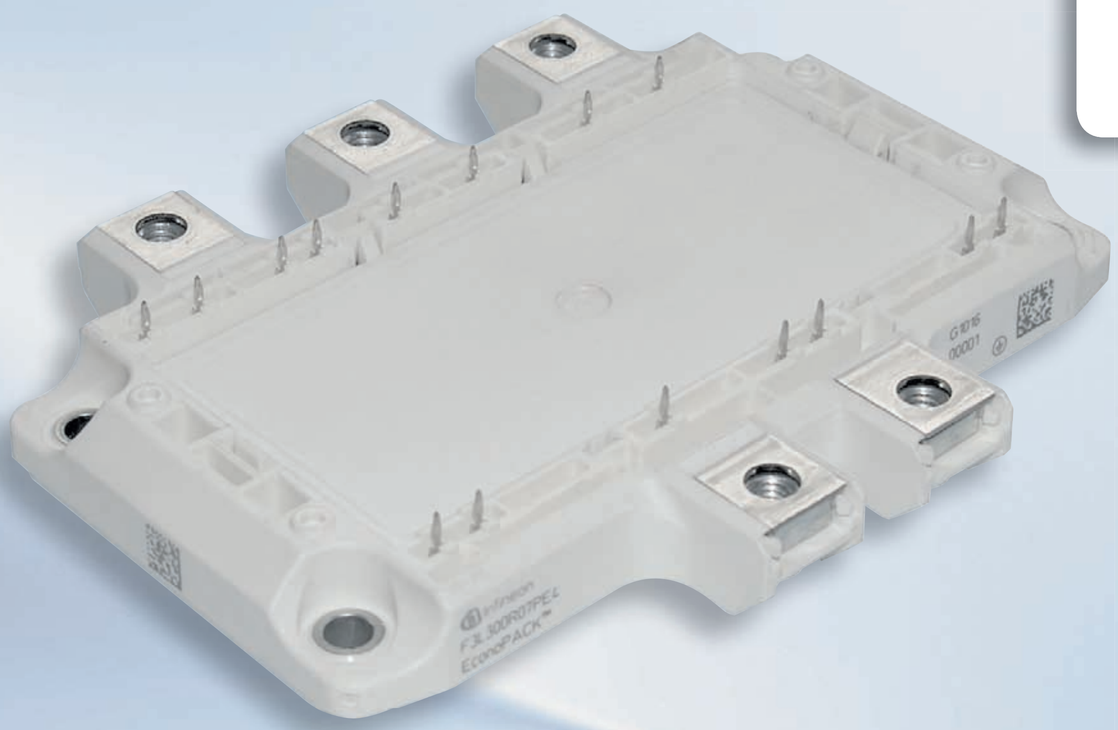
POWER MODULES

Power Electronics Packaging Revolution Without Bond Wires, Solder and Thermal Paste

THE EUROPEAN JOURNAL FOR POWER ELECTRONICS AND TECHNOLOGY

Also inside this issue



EconoPACK™ 4

The world standard for 3-level applications

The EconoPACK™4 is an optimized module for 3-level applications like:

- Uninterruptible Power Supply
- Solar Inverter
- High Speed Drives

where a rugged design, high efficiency and less harmonics are needed.

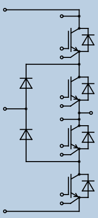
For these applications starting with 50kW up to 125kW, the EconoPACK™ 4 can be used to build up one phase. For higher power ratings modules can be switched in parallel.
All modules are equipped with the state of the art IGBT4.
Further information's are available on request.

The degree of efficiency for two 3-level topologies, NPC1 and NPC2, has to be investigated depending on the switching frequency.

- EconoPACK™ 4 in NPC2 topology for low and medium switching frequencies (approx. $f_{sw} \leq$ 12kHz)
- EconoPACK™ 4 in NPC1 topology for high switching frequencies (approx. $f_{sw} \geq$12kHz)

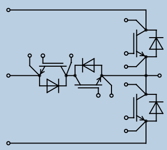
NPC1 topology

- 650V IGBT4
- Optimized for $f_{sw} \geq$12kHz
- Portfolio
  - F3L200R07PE4
  - F3L300R07PE4



NPC2 topology

- 650V/1200V IGBT4
- Optimized for f_{sw}<12kHz
- Portfolio:
  - F3L300R12PT4_B26
  - F3L400R12PT4_B26



[www.infineon.com/highpower]

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COVER STORY

Power Electronics Packaging Revolution Without Bond Wires, Solder and Thermal Paste

Power module packaging is driven by the ever increasing demand for higher power densities, reliability improvements and further cost reductions. The known reliability limitations of traditional solder joints and bond wires are holding back significant power density increases made possible thanks to higher junction temperatures and the future utilization of wide bandgap devices. Today, silver sintering has already started to replace the solder joint between chip and DBC substrate, leaving one major reliability bottleneck: the bond wire interface on the chip surface. Most of the new packaging approaches have been based on soldered or welded bumps, as well as on embedded interconnection technologies. The innovative packaging technology, named SKiN Technology, presented here, takes the silver (Ag) sinter joint and applies it to all remaining interconnections in a modern power module. In addition to the double-sided sintering of power chips, the entire DBC is sintered to the heat sink. The resulting device has a very high power density and demonstrates remarkable thermal, electrical, and reliability performance compared to traditional packaging technologies. Full story on page 23.

Cover supplied by SEMIKRON, Nuremberg, Germany

The Future (of Power Electronics) is in Renewable Energy

The share of electricity produced from renewable energies in Germany has increased from 6.3 percent in the year 2000 to about 17 percent in 2010. In 2010, investments totaling 26 billion Euros were made in Germany's renewable energies sector. According to official figures, some 370,000 people in Germany were employed in the renewable energy sector in 2010, especially in small and medium sized companies. This is an increase of around 8 percent compared to 2009, and well over twice the number of jobs in 2004 (160,500). About two-thirds of these jobs are attributed to the Renewable Energy Sources Act. Thus Germany is the world's first major renewable-energy economy. In 2010 nearly 17 percent (more than 100 TWH) of Germany's electricity supply (600 TWH) was produced from renewable energy sources, more than the 2010 contribution of gas fired power plants. Renewable electricity in 2010 was more than 100 TWh including wind power (36.5 TWh), biomass and biowaste (33.5 TWh), hydropower (20 Twh), and photovoltaig solar power 12.0 (Twh). Doubling its previous record, the German solar PV industry installed 7,400 MW from nearly one-quarter million individual systems in 2010, according to official figures issued by the German Bundesnetzagentur (federal network agency).

And in December alone, Germans installed more than 1,000 MW of solar PV, enough solar capacity to generate 1 TWh of electricity under German weather conditions. While they represent only half that installed in June 2010, the December installations were 50% greater than total solar PV installed in the USA in 2010 and as much as that rumored to have been installed in Japan last year. According to data posted publicly by Germany's electricity transmission exchange (EEX), that penetration of wind and solar reached more than 30 percent of supply on February 7. The combined real-time wind and solar generation varied from a high of 32 percent of supply at midnight to a low of 18 percent of supply at sunrise. Solar PV generation delivered more than 8,000 MW for the two-hour period from just before noon until 2:00 pm, reaching a peak of nearly 8,500 MW at noon. During the same time period, conventional sources contributed 50,000 MW and wind delivered another 10,000 MW to the network. Thus wind and solar power can not be ignored as minor and expensive contributors!

Germany uses an advanced system of feed-in tariffs to pay for renewable energy generation, and has an aggressive target of meeting 40 percent of its electricity supply with renewable energy by 2020. Its system of advanced renewable tariffs has enabled Germany to exceed its 2010 target. Following the March 2011 Japanese nuclear crisis, Germany's chancellor Angela Merkel closed two nuclear reactors permanently, and another five temporarily. She also called on her government to revisit its controversial decision to extend the life of its aging reactors. Now Germany's federal government is working on a new plan for increasing energy efficiency and renewable energy commercialization, with a particular focus on offshore wind farms.

Germany's renewable energy sector is among the most innovative and successful worldwide. Nordex, Repower, Fuhrländer and Enercon are wind power companies based in Germany. SolarWorld, Q-Cells and Conergy are solar power companies based in Germany. These companies dominate the world market. Every third solar panel and every second wind rotor is made in Germany. Germany's main competitors in solar electricity are Japan, the US and China. In the wind industry it is Denmark, Spain and the US.

Nearly 800,000 people work in the German environment technology sector; an estimated 214,000 people work with renewables. From this situation benefits heavily the power electronics industry, particularly the manufacturers of power semiconductors and power modules. According to IMS, the power module market grew by 65% in 2010, significantly faster than discrete power semiconductors. This was fueled by the recovering industrial motor drive market and a rapid expansion of inverter production for renewable energy applications. Sales of power modules in renewable energy inverters only grew by a staggering 98 percent!

Nuremberg-based Semikron is a typical example on that situation. More than 30% of the 2010 turnover is generated from the renewable energies market which has more than doubled over the last three years, following the drives market with a share of 35%. The company developed the first IGBT modules for use in wind turbines in the beginning of the 1990s. CEO Dirk Heidenreich expect around Euro 600 million turnover by end of the running fiscal year, mainly to investments in power modules for wind energy applications. And the recent political decisions to move out of nuclear power confirm the early investments in renewable energy applications.

It's time to go greener - worldwide!

Achim Scharf
PEE Editor

Wind Power Drives Global Renewable Energy Growth

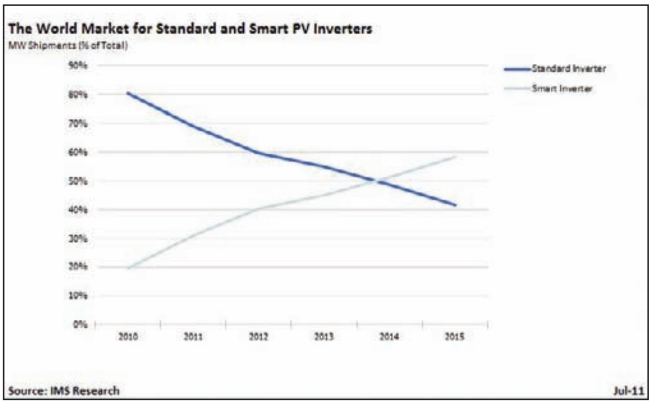
The REN21 Global Status Report released in July by the Global Wind Energy Council (GWEC) shows that renewable energy continues its strong performance despite continuing economic turmoil, cuts in incentives and subsidies and low natural gas prices. The growth of wind power in particular continues to drive renewable energy development, but other sectors such as solar PV are also seeing strong investment.

Trends for wind power include continued offshore development, the growing popularity of community-based projects and distributed, small-scale grid-connected turbines, and the development of wind projects in a wider variety of geographical locations. Average turbine sizes continued to increase in 2010, with some manufacturers launching 5MW and larger turbines, and direct-drive turbine designs captured 18% of the global market. "Wind power continues to lead the renewable electricity sector, with more new capacity installed in 2010 than for any other technology," said Steve Sawyer, GWEC Secretary. "Equally important to note is that in 2010 for the first time, more wind power was added in developing countries and emerging markets than in the industrialised world."

In 2010, renewable energy supplied an estimated 16% of global final energy consumption and delivered close to 20% of global electricity production. Renewable capacity now comprises about a quarter of total global power-generating capacity. Including all hydropower (estimated 30GW added in 2010), renewable energy accounted for approximately 50% of total added power generating capacity in 2010. Renewable energy policies continue to be the main driver behind renewable energy growth. By early 2011, at least 119 countries had some type of policy target or renewable support policy at the national level, more than doubling from 55 countries in early 2005. More than half of these countries are in the developing world. Last year, investment reached a record $211 billion in renewables, about one-third more than the $160 billion invested in 2009, and more than five times the amount invested in 2004.

Smart PV Inverter Shipments to grow to 27 GW by 2015

'Smart' PV inverter shipments are forecast to grow to 27 GW in 2015, accounting for almost 60% of the market compared to just 20% in 2010 according to IMS Research. This is being driven by utility concerns over grid imbalances, the growing proportion of PV connected to the grid, as well as the need for energy storage to take advantage of self-consumption tariffs and further incorporate PV into the 'smart grid'. Features such as reactive power, smart grid interaction and energy storage are transforming inverters from a simple power conversion unit into an essential component of grid infrastructure and will radically change the PV inverter market over the next five years. "Utilities, especially in Europe, are increasingly pushing for inverters to assist in grid stabilization and conform to stricter technical requirements", explains analyst Tom Haddon. Because of this, IMS Research forecasts that smart inverters will account for 80% of the EMEA market in 2015.



Germany is leading the integration of PV into the grid with the newly implemented Low and Medium Voltage Directives, and other European countries are likely to follow suit. Due to this, 'standard' inverters are forecast to fall to just 42% of global shipments by 2015 as the directives are fully enforced. "Reactive power is an essential feature for inverters to carry if PV is to be a substantial part of the energy mix to provide local grid control which is why the German authorities have acted first to implement such codes." Haddon added. Another new trend identified in the report is inverters incorporating energy storage and IMS forecasts that close to 5% of all PV inverters shipped in 2015 will be equipped with storage such as batteries to help power loads continuously throughout the day. However, in order for this to happen these products will have to quickly reduce in cost, and improve in efficiency and reliability before gaining widespread acceptance.

www.ren21.net, www.pvmarketresearch.com

Research for Volume Production of GaN On-Silicon Wafers

Capricorn Cleantech Fund, Robert Bosch Venture Capital (RBVC), and LRM jointly invested € 4 million in EpiGaN to launch volume production of GaN on-silicon wafers.

Incorporated in 2010, EpiGaN was founded as a spin-off of Belgium research institute Imec. For more than 10 years, the founders jointly developed state-of-the-art GaN-on-Si technology on 4" and 6" wafers at Imec, part of which has been licensed to EpiGaN. They are joined now by a consortium of investors who share their vision on GaN-on-Si as a key technology for enhancing power management efficiency, implementing renewable energy sources, or enabling cleaner transportation technologies with reduced environmental impact.

"EpiGaN has demonstrated the capability of its innovative material to support record device performance either in high voltage, high current or high frequency operation", said Dr Marianne Germain, CEO of EpiGaN. "The support of the investors will allow us to implement own production capacity and increase our market supply. 4" and 6" GaN-on-Si wafers for high voltage or RF applications are readily available while a 200mm wafer technology is under development at the Research Campus Hasselt in Limburg, geographically located squarely within Leuven, Eindhoven and Aachen".

www.epigan.com

Power Semiconductor Market Fueled by Energy Efficiency

Following the 2009 slump, the power semiconductor discrete and module market bounced back and grew by 43% in 2010 due to a year of spectacular recovery, according to IMS Research.

Against a background of burgeoning demand, delivery challenges and extending lead-times, Infineon retained the No. 1 spot as largest supplier of power discretes and modules. It was the largest market share gainer in the power MOSFET market and extended its leadership position in IGBTs. Other manufacturers with growing market shares included power module specialists Mitsubishi and Fuji Electric, with STMicroelectronics, International Rectifier and Vishay also gaining share in power discretes.

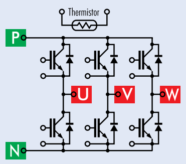
The overall discrete power semiconductor and power module market grew by 43% to just under $16 billion in 2010, almost $2 billion higher than its 2008 peak. The research firm found that the main drivers of growth were industrial motor drives, automotive and computer/office equipment. These applications have one thing in common: the adoption of the latest devices to improve power conversion efficiency. "2010 saw rapidly rising IGBT sales in the Chinese market for use in domestic appliances such as room air-conditioning and variable speed washing machines", commented IMS analyst Richard Eden. "Again, the driver for this market growth is the shift from inefficient equipment to inverterised replacements."

The Top Ten Suppliers of Power Semiconductors Worldwide in 2010 were Infineon, Mitsubishi, Toshiba, STMicroelectronics, Vishay, International Rectifier, Fairchild, Fuji Electric, Renesas, and Semikron.

The power module market grew by 65% in 2010, significantly faster than discrete power semiconductors. This was fuelled by the recovering industrial motor drive market and a rapid expansion of inverter production for renewable energy applications. IGBT module sales boomed on the back of a wave of industrial motor drive installations in new factories, the construction of which had been delayed by the recession. Sales of power modules in renewable energy inverters grew by a staggering 98% as countries rushed to install solar PV systems. Mitsubishi gained market share to retain the No 1 spot, ahead of Infineon, Semikron and the fast-rising Fuji Electric. All of the Japanese manufacturers benefited from the strengthening value of the Yen, which inflated their revenue share in terms of US dollars.

http://imsresearch.com

The 6-PACKs



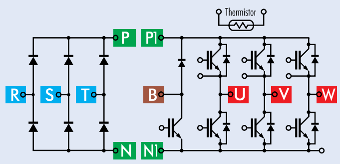
With soldering pins

	I_C	600V	1200V	1700V
45x107,5mm	50A		●	
	75A	●	●	
	100A	●	●	
62 x 122 mm	75A		●	
	100A		●	●
	150A	●	●	●
	180A		●	
	200A		●	

With PressFit contacts

	I_C	600V	1200V
45x107,5mm	50A		●
	75A	●	●
	100A	●	●
62 x 122 mm	100A		●
	150A	●	●
	180A		●
	200A		●

The PIMs



With soldering pins

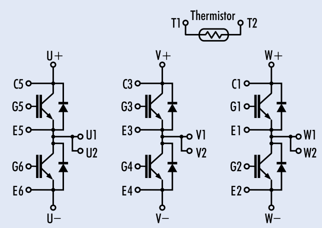
	I_C	600V	1200V
45x107,5mm	25A		●
	35A		●
	50A	●	●
62 x 122 mm	75A	●	●
	100A	●	●
	150A	●	●

With PressFit contacts

	I_C	600V	1200V
45x107,5mm	25A		●
	35A		●
	50A	●	●
62 x 122 mm	75A	●	●
	100A	●	●
	150A	●	●

The High Power 6-PACKs

	I_C	1200V	1700V
150 x 162 mm	225A	●	●
	300A	●	●
	450A	●	●
	550A	●	



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300 Millimeter Fab for Power Semiconductors

Infineon will further extend its technology leadership by driving 300mm thin wafer manufacturing of power semiconductors out of the newly-acquired facility in Dresden. The Company will also expand the 200mm manufacturing site in Kulim, Malaysia.

"With this leading innovation Infineon will expand its competitive advantage," said CEO Peter Bauer on July 28 by presenting its figures for the 3rd fiscal quarter 2011. The company will use the clean room that was purchased in May 2011 for about Euro 100 million from the insolvency administrator of Qimonda Dresden for the mass manufacturing of power devices on 300mm wafers. Until 2014 Infineon will invest around Euro 250 million and create approximately 250 jobs in Dresden. If the market revenue and underlying conditions develop in line with forecasts, further expansion

would be possible. "Even with higher costs for 30mm raw materials and tools, we expect a cost advantage of 20 to 30%", said Operations Manager Reinhard Ploss.

The company booked fiscal third quarter sales of Euro 1,043 million, an increase of 5% from the previous quarter. At a constant exchange rate for the Dollar against the Euro, quarter-over-quarter growth rate would have been approximately two percentage points higher. Growth was driven by strong demand in Industrial & Multimarket and Automotive. The Automotive division did not experience any significant negative impact neither on revenue nor on Segment Result from disruptions within the automotive supply chain after the Japan earthquake. Infineon expects sales for the fourth quarter of the 2011 fiscal year to be at least flat.

Manufacturing cost of 200mm vs 300mm power semiconductors

[related to physical wafers]	200mm	300mm
Wafer size	100%	225%
Equipment	100%	~160%
Raw wafer cost	100%	~300%
Personnel	100%	~80%
Other effects	100%	~150%
Relative Cost per mm²	**100%**	**70–80%**

www.infineon.com

Semikron Geared for Further Growth

Coinciding with the 60th anniversary the company further expands its headquarters in Nuremberg. The family business started from humble beginnings in 1951 but has established itself as a global player with 3,600 employees, 35 companies, and ten production sites worldwide.

CEO Dirk Heidenreich announced a turnover of Euro 545 million for fiscal year 2010, an increase of 68% compared to 2009, when Semikron faced a loss of 30% down to Euro 325 million due to the financial crisis. More than 30% of the turnover is generated from the renewable energies market which has more than doubled over the last three years, following the drives market with a share of 35%. The company developed the first IGBT modules for use in wind turbines in the beginning of the 1990s. These modules featured innovative pressure contact technology, integrated power, driver and sensor functions and met the challenges posed by this entirely new area of application in terms of long-term reliability and power density. "We are now even stronger and expect around Euro 600 million by end of the running fiscal year, mainly to our investments in power modules for wind energy applications", Heidenreich stated. "The recent political decisions to move out of nuclear power confirm our early investments in renewable energy applications!"

The experience in the electric hybrid vehicle market also dates back to the early 1990s with the Audi Duo, long before the German government announced that one million passenger cars should be electrically driven by 2020. In 2010 Semikron introduced Skai, the most compact power electronic systems for hybrid and electric vehicles for use in the agricultural industry, construction industry, materials handling and battery-powered vehicles of any kind. The dedication to this market is evident in partnering with Compact Dynamics and Drivetek, and the acquisition of Vepoint. Worldwide 560,000 electric fork lifts and 8,250 hybrid busses are powered

"We expect around €600 million turnover by end of the running fiscal year, mainly to our investments in power modules for wind energy applications", stated Semikron's CEO Dirk Heidenreich on occasion of the logistic center opening

Assembly station of power modules - adding the driver to the module's body

by Semikron technology.

Also SindoPower (**www.sindopower.com**), founded in 2009, is a holding company of the Semikron Group. The company's focus is a power electronic products platform including comprehensive information in the field of power electronics. Its product range includes IGBT modules, diode/thyristor modules, bridge rectifiers, CIB modules, discrete diodes and thyristors in soldered and screw design, or as disc or SMD components. SindoPower is now offering power electronic assemblies for up to 250A in the form of DIY kits containing heat sink, fan, single-phase and 3-phase diode semiconductor modules, sensors, complete with screws, tracks and assembly instructions. The new SEMISTACK kits can be configured online: to do so the customer selects the current, voltage, circuit topology, temperature sensor, and airing system. The online configurator then shows the right components as a finished single-source assembly.

In May this year a revolutionary packaging technology for power semiconductors which does away with bond wires, solders and thermal paste was launched (see our cover story). This reliable and space-saving technology is the optimum solution for vehicle and wind power applications, markets with a high growth rate.

A state-of-the-art logistics centre of 12,300m^2 was added in July to the total area of 42,000 m^2. During 2010 and 2011 a total of Euro 114 million has been invested in the expansion of production areas and equipment worldwide, including a new hall for the various tests such as power and temperature cycling. The investment of Euro 4.6 million in this hall covers 1,200m^2 space, 1.4MW electrical power supply, and 500kW of cooling power.

www.semikron.com

Chamber for various tests on high-power modules within the new test hall
Photos: AS

Cree Europe Names Vice President

Cree has appointed Stephan Greiner to Vice President of its EMEA region. Greiner leads the team from the German regional headquarter located in Munich/Garching. He brings more than 16 years of experience in the semiconductor sales market to his position at Cree. He worked as Vice President of Global Sales at the optoelectronics supplier Everlight Electronics in Taiwan. Before, he worked at the Osram Opto Semiconductors GmbH as Senior Director of Sales. In his new role, he is responsible for the sales of Cree's complete portfolio, ranging from LED chips and components to RF and Silicon Carbide Power devices.

www.cree.com

Vicor in Transisition

Andover-based Vicor Corp. is in a period of strategic and organizational transition to reach customers with new approaches in distribution and product platforms.

This transition should lead to significant growth rates starting in 2012, when the company anticipate revenue to be driven by new sources. “We are announcing new products, implementing a multi-tiered distribution model including Future Electronics, and aggressively pursuing new markets. Power density and conversion efficiency are becoming customer priorities, not just for the high end applications we have traditionally served such as IBM cloud servers, but for a broader range of applications and customers”, Vicor’s newly appointed VP Global Sales & Marketing, Philip D. Davies, pointed out at a recent trip to Munich. “As examples we will deliver customized bricks in 48 hours and will enter the electric vehicle market by offering high-voltage DC/DC converters in 2012”. Future Electronics will begin a phased rollout of Vicor’s products in August. Founded in 1968, the company has 5,000 employees in 169 offices in 42 countries around the world.

Obviously this transition makes sense, since Vicor’s business has been negatively impacted in recent quarters. Revenues of $65,402,000 for the second fiscal quarter ended June 30, 2011, decreased from $70,455,000 for the first quarter. “Bookings and revenues during the second quarter were negatively impacted by curtailed demand for bricks and custom products because of continued deferral of funding for defense electronics projects. Brick Business Unit revenues declined approximately 12% sequentially. Weakness in the defense market was partially offset by progress in other markets, led by our V.I Chip and Picor business units. V.I Chip experienced approximately 10% revenue growth sequentially, and continued to improve gross margins with higher volumes and efficiency initiatives”, commented CEO Patrizio Vinciarelli. Thus the focus is on the V.I chip business. PRM buck-boost regulators achieve 97% efficiency. Up to 130A VTM current multipliers free up prime PCB real estate at the POL. As Factorized Power components,

V.I Chips reduce distribution and interconnect losses and eliminate bulk capacitance with up to 4MHz switching frequency. Up to 400V input BCMs facilitate high-voltage power distribution.

www.vicorpower.com

Vicor’s newly appointed VP Philip D. Davies focuses on V.I chip business and distribution

100V Half-bridge Gate Driver for E-GaN Power FETs

National Semiconductor introduced the industry's first 100V half-bridge gate driver optimized for use with enhancement-mode Gallium-Nitride (GaN) power FETs in high-voltage power converters. According to National the LM5113 high-side and low-side GaN FET driver reduces component count by 75% and shrinks PCB area by up to 85% compared to discrete driver designs.

Designers of power bricks and communications infrastructure equipment require high power efficiency in the smallest form factor. Enhancement-mode GaN FETs enable new levels of efficiency and power density compared to standard MOSFETs due to their low on-resistance (R_{dson}) and gate charge (Q_g) as well as their ultra-small footprint, but driving them reliably presents significant new challenges [1, 2]. National's LM5113 driver integrated circuit (IC) eliminates these challenges, enabling power designers to realize the benefits of GaN FETs in a variety of popular power topologies. "National's LM5113 bridge driver helps designers unleash the performance of our eGaN FETs by simplifying the design. The driver reduces component count, and paired with our eGaN FETs, enables a tremendous PCB area savings and higher level of power density versus equivalent MOSFET-based designs", commeted Alex Lidow, co-founder and CEO for Efficient Power Conversion Corporation (**www.epc-co.com**).

Modes of operation

Using proprietary technology, the device regulates the high side floating bootstrap capacitor voltage at approximately 5.25V to optimally drive enhancement-mode GaN power FETs without exceeding the maximum gate-source voltage rating. The LM5113 also features independent sink and source outputs for flexibility of the turn-on strength with respect to the turn-off strength. A low impedance pull down path of 0.5Ω provides a fast, reliable turn-off mechanism for the low threshold voltage enhancement-mode GaN power FETs, helping maximize efficiency in high frequency power supply designs. The driver features an integrated high-side bootstrap diode, and also provides independent logic inputs for the high-side and low-side drivers, enabling flexibility for use in a variety of both isolated and non-isolated power supply topologies [3].

The inputs of the LM5113 are TTL logic compatible, and can withstand input voltages up to 14V regardless of the V_{DD} voltage. The split gate outputs provide flexibility to adjust the turn-on and turn-off strength independently and the strong sink capability maintains the gate in the low state, preventing unintended turn-on during switching. The LM5113 can operate up to several MHz.

The high side driver uses the floating bootstrap capacitor voltage to drive the high-side FET. As shown in the bock diagram, the bootstrap capacitor is recharged through an internal bootstrap diode each cycle when the HS pin is pulled below the V_{DD} voltage. For inductive load applications the HS node will fall to a negative potential, clamped by the low side FET. Due to the intrinsic feature of enhancement mode GaN FETs the source-to-drain voltage, when the gate is pulled low, is usually higher than a diode forward voltage drop. This can lead to an excessive bootstrap voltage that can damage the high-side GaN FET. The LM5113 solves this problem with an internal clamping circuit that prevents the bootstrap voltage from exceeding 5V.

The output pull-down and pull-up resistance of LM5113 is optimized for enhancement mode GaN FETs to achieve high frequency, efficient operation. The 0.5_ pull-down resistance provides a robust low impedance turn-off path necessary to eliminate undesired turn-on induced by high dv/dt or high di/dt. The 2Ω pull-up resistance helps reduce the ringing and over-shoot of the switch node voltage. The split outputs of the LM5113 offer flexibility to adjust the turn-on and turn-off speed by independently adding additional impedance in either the turn-on path and/or the turn-off path.

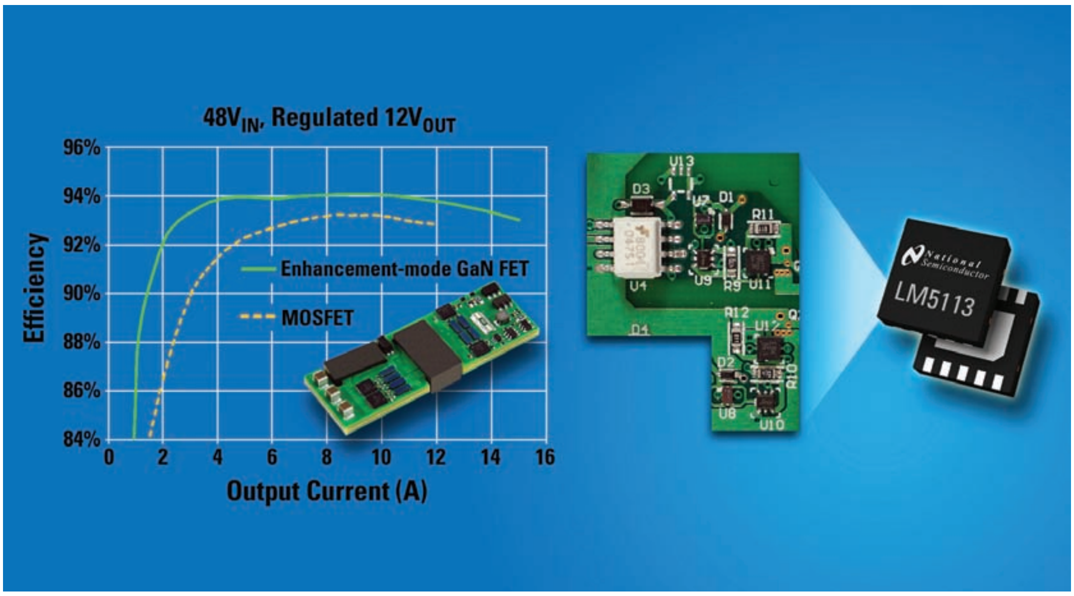
The LM5113 has an under-voltage lockout (UVLO) on both the V_{DD} and bootstrap supplies. When the V_{DD} voltage is below the threshold voltage of 4V, both the HI and LI inputs are ignored, to prevent the GaN FETs from being partially turned on. Also if there is sufficient VDD voltage, the UVLO will actively pull the LOL and HOL low. When the HB to HS bootstrap voltage is below the UVLO threshold of 3.3V, only HOL is pulled low. Both UVLO threshold voltages have 200mV of hysteresis to avoid chattering.

Bypass capacitor

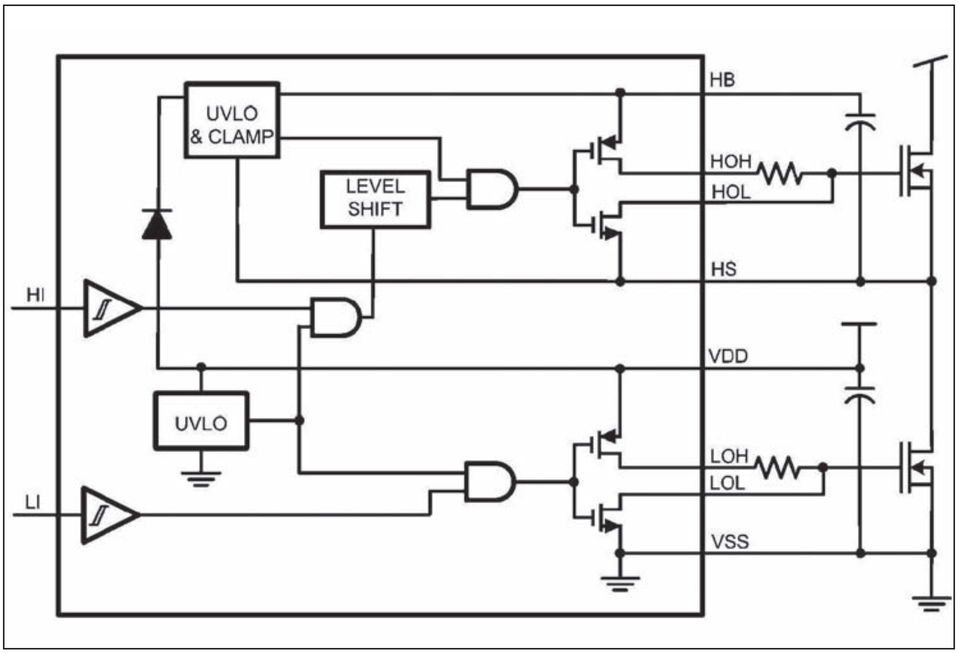
The V_{DD} bypass capacitor provides the gate charge for the low-side and high-side transistors and to absorb the reverse recovery charge of the bootstrap diode. The required bypass capacitance can be calculated as follows:

$$C_{VDD} > \frac{Q_{gH} + Q_{gL} + Q_{rr}}{\Delta V}$$

Q_{gH} and Q_{gL} are gate charge of the high-side



eGaN characteristics with conventional driver board and integrated driver LM5113



Simplified block diagram of LM5113

and low-side transistors respectively. Q_{rr} is the reverse recovery charge of the bootstrap diode, which is typically around 4nC. ΔV is the maximum allowable voltage drop across the bypass capacitor. A 0.1µF or larger value, good quality, ceramic capacitor is recommended. The bypass capacitor should be placed as close to the pins of the IC as possible to minimize the parasitic inductance.

Bootstrap capacitor

The bootstrap capacitor provides the gate charge for the high-side switch, DC bias power for HB under-voltage lockout circuit, and the reverse recovery charge of the bootstrap diode. The required bypass capacitance can be calculated as follows:

$$C_{BST} > \frac{Q_{GH} + I_{HB} \times t_{ON} + Q_{rr}}{\Delta V}$$

IHB is the quiescent current of the high-side driver, and t_{ON} is the maximum on-time period of the high-side transistor. A good quality, ceramic capacitor should be used for the bootstrap capacitor. It is recommended to place the bootstrap capacitor as close to the HB and HS pins as possible.

Power dissipation

The power consumption of the driver is an important measure that determines the maximum achievable operating frequency of the driver. It should be kept below the maximum power dissipation limit of the package at the operating temperature. The total power dissipation is the sum of the gate driver losses and the bootstrap diode power loss.

The gate driver losses are incurred by charge and discharge of the capacitive load. It can be approximated as

$$P = (C_{LoadH} + C_{LoadL}) \times V^2_{DD} \times I_{SW}$$

C_{LoadH} and C_{LoadL} are the high-side and the low-side capacitive loads respectively. It can also be calculated with the total input gate charge of the high-side and the low-side transistors as

$$P = (Q_{gH} + Q_{gL}) \times V_{DD} \times f_{SW}$$

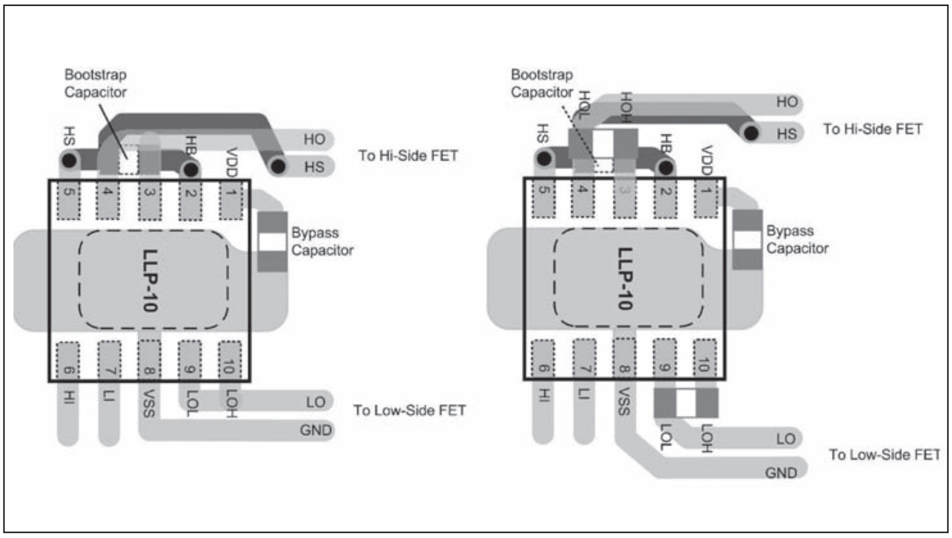
The bootstrap diode power loss is the sum of the forward bias power loss that occurs while charging the bootstrap capacitor and the reverse bias power loss that occurs during reverse recovery. Since each of these events happens once per cycle, the diode power loss is proportional to the operating frequency. Larger capacitive loads require more energy to recharge the bootstrap capacitor resulting in more losses. Higher input voltages (V_{IN}) to the half bridge also result in higher reverse recovery losses.

Layout considerations

Small gate capacitance and miller capacitance enable enhancement mode GaN FETs to operate with fast switching speed. The induced high dv/dt and di/dt, coupled with a low gate threshold voltage and limited headroom of enhancement mode GaN FETs gate voltage, make the circuit layout crucial to the optimum performance. Following are some hints.

The first priority in designing the layout of the driver is to confine the high peak currents that charge and discharge the GaN FETs gate into a minimal physical area. This will decrease the loop inductance and minimize noise issues on the gate terminal of the GaN FETs. The GaN FETs should be placed close to the driver.

The second high current path includes the



Recommended layout patterns wthout any gate resistors (left) and with an optional turn-on gate resistor (right)

bootstrap capacitor, the local ground referenced V_{DD} bypass capacitor and low-side GaN FET. The bootstrap capacitor is recharged on a cycle-by-cycle basis through the bootstrap diode from the ground referenced V_{DD} capacitor. The recharging occurs in a short time interval and involves high peak current. Minimizing this loop length and area on the circuit board is important to ensure reliable operation.

The parasitic inductance in series with the source of the high-side FET and the low-side FET can impose excessive negative voltage transients on the driver. It is recommended to connect HS pin and V_{SS} pin to the respective source of the high-side and low-side transistors with a short and low-inductance path.

The parasitic source inductance, along with the gate capacitor and the driver pull-down path, can form a LCR resonant tank, resulting in gate voltage oscillations. An optional resistor or ferrite bead can be used to damp the ringing.

Low ESR/ESL capacitors must be connected close to the IC, between V_{DD} and V_{SS} pins and between the HB and HS pins to support the high peak current being drawn from V_{DD} during turn-on of the FETs. It is most desirable to place the V_{DD} decoupling capacitor and the HB to HS bootstrap capacitor on the same side of the PC board as the driver. The inductance of vias can impose excessive ringing on the IC pins.

To prevent excessive ringing on the input power bus, good decoupling practices are required by placing low ESR ceramic capacitors adjacent to the GaN FETs.

The recommended layout patterns consider two cases without any gate resistors and with an optional turn-on HOH/LOH gate resistor. It should be noted that 0402 SMD package is assumed for the passive components in the drawing.

The LM5113 is available in a standard LLP-10 pin package, which contains an exposed pad to aid power dissipation. Production quantities will be available in September.

Literature

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Digital Control Brings More Efficiency to DC/DC Converters

As energy prices rise and "green" initiatives gain success, private companies and government regulators are ratcheting up the demands on power-supply manufacturers. The demands on server power supplies by the European Commission, which is the executive body of the European Union (EU), and the United States Environmental Protection Agency (EPA), have grown to cover efficiency across varying load levels, as well as standby power draw. Server-farm operators have implemented similar demands on their power-supply manufacturers. The Phase-Shifted Full-Bridge (PSFB) topology is one type of DC/DC converter that has the potential to meet the efficiency demands on future power supplies. A DSC's flexibility makes the temperamental PSFB topology easier to manage, and also enables advanced techniques that further improve the efficiency of the PSFB topology. **Charlie Ice, Product Marketing Manager, and Ramesh Kankanala, Principal Applications Engineer, Microchip Technology, Chandler, USA**

With these stringent regulations, and more on the horizon, power-supply manufacturers are turning to digital control. In a fully-digital solution, a fully-programmable Digital Signal Controller (DSC) directly generates the PWM signals that control the power stage. At the same time, the controller handles system-management tasks, such as data logging, communication and fault reporting. This enables the power-supply designer to program advanced control methods into the DSC, which would be difficult if not impossible in an analog design. This feature also gives the designer the flexibility to implement any data logging and communication standards needed by the end customer.

Necessity for the phase-shifted full-bridge topology

Let us discuss the simple full-bridge topology, necessary for high-frequency operations, and then move to efficiency-improvement strategies.

As shown in Figure 1, a Full-Bridge Converter is configured using four switches - Q1, Q2, Q3 and Q4. The diagonal switches Q1, Q4 and Q2, Q3 are switched ON simultaneously, which provides a full input voltage (VIN) across the primary winding of the transformer. During each half cycle of the converter, the diagonal switches Q1, Q4 and Q2, Q3 are turned ON, and the polarity of the transformer reverses in each half cycle. In the Full-Bridge Converter, at a given power compared to the Half-Bridge Converter, the switch current and primary current will be half. This reduction in current makes the Full-Bridge Converter suitable for high power levels. However, the diagonal switches are hard switched, resulting in high turn ON and OFF switching losses.

In the past, when sophisticated controllers were not available, power-supply engineers were forced to use less efficient hard-switched power-conversion methods. These losses increase with frequency and, thus, limit the frequency of operation, limiting the power supply's ability to efficiently deliver power.

Soft-switched full-bridge topology

Using today's DSCs, designers now consider higher operating frequencies to reduce the volume of magnetics and filter capacitors in power supplies. These higher frequencies, in turn, result in higher switching losses in hard-switched power converters, such as the traditional Full-Bridge Converter. A better alternative is to choose relatively complicated soft-switching methods to reduce switching losses and deliver higher power density.

A Soft-switched full-bridge (PSFB) converter is a soft-switched topology

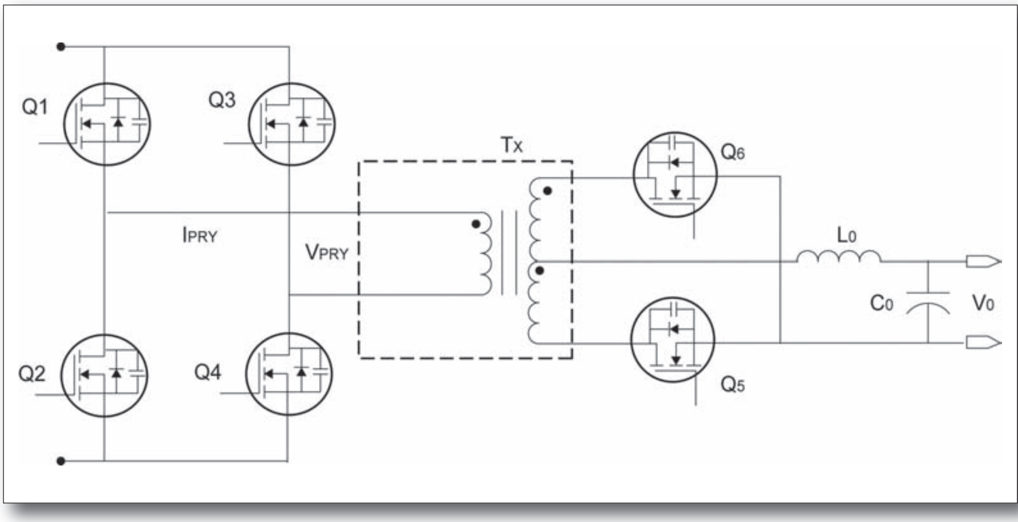

Figure 1: Full-Bridge Converter

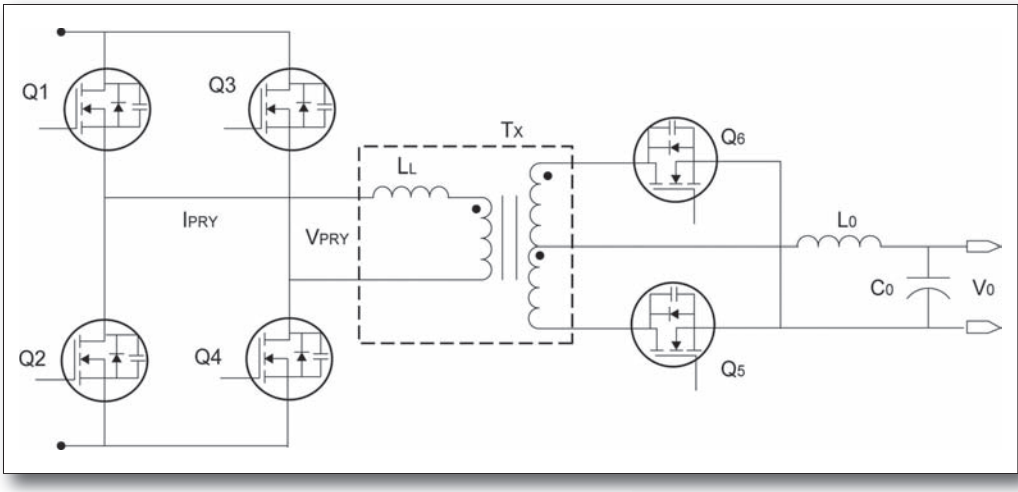

Figure 2: Phase-Shifted Full-Bridge Converter

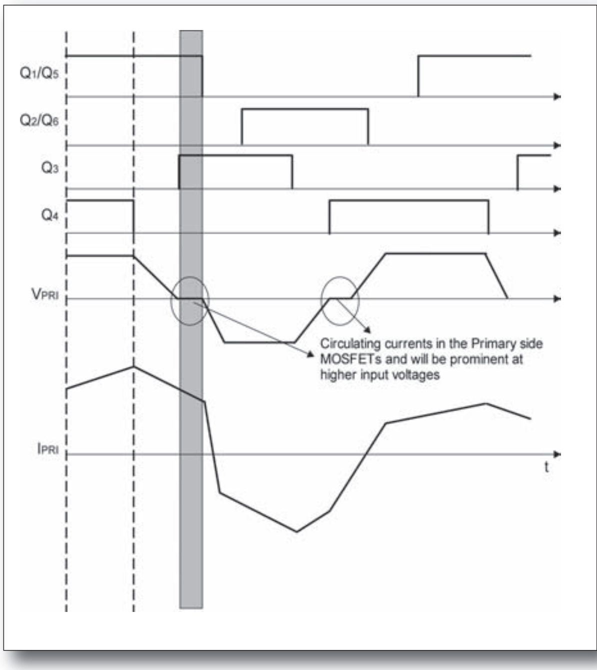

Figure 3: Traditional Configuration of Synchronous MOSFET Gate Drives

that uses parasitics such as output capacitance of switching devices (MOSFET, IGBT) and leakage inductance of transformers to obtain the resonant transition (Figure 2). This resonance will place zero voltage across the switching devices while they turn ON, and therefore eliminate their turn ON switching losses.

PSFB converters have been used in telecom and server applications where density and efficiency of the converter is paramount. The normal operation of PSFB converters is explained in many papers and we will start from that point to showcase how a DSC can further improve the performance.

Phase-shifted full-bridge converter with conventional synchronous MOSFET gate drives

Most DC/DC converters are designed with isolation transformers for user safety, and to comply with rules imposed by regulatory bodies. Higher-rated power supplies are designed with the PSFB topology in the primary and full-wave synchronous rectifier in the secondary to achieve high efficiency.

In PSFB converters, with a traditionally controlled synchronous MOSFET configuration, the MOSFETs Q1, Q3 or Q2, Q4 should be ON (Figure 3). At that time, there is no power transfer from the primary to the secondary and the MOSFET Q5 is still ON.

Due to the presence of an inductor (L_o) in the secondary side of the converter, the energy in the output inductor is circulating through the MOSFET Q5 and the transformer (T_x) secondary coil. The current continues to flow through the transformer secondary coils, either through the MOSFET's channel, or through the MOSFET's body diodes. Due to reflection of current from the secondary to the primary, circulating current exists during zero states (non-energy transfer states from the primary to the secondary) in the primary, which causes losses in the converter. These circulating current losses are predominant at higher voltages than the rated nominal input voltages. And also to avoid cross conduction, there is an intentional dead band between Q5 and Q6 MOSFET gate drives. During this period, neither of the synchronous MOSFETs conducts. Therefore, the current takes the path of the MOSFET body diode. These MOSFET body diodes have a high forward drop compared to the $R_{ds(ON)}$ of the MOSFET, which translates to (V_F * I) >> (I^2_{rms}* $R_{ds(on)}$).

The higher losses encountered in conventional synchronous gate drives can be prevented by using the overlapping gate-drive signals, as described in the next section.

Overlapping of synchronous MOSFET gate-drive signals

Losses that occur during the zero state of the transformer's primary side can be avoided by overlapping the synchronous MOSFETs' PWM gate drive. This increases the power supplies efficiency in three ways: First, in a center-tapped full-wave rectifier, overlapping the synchronous MOSFETs' results in cancellation of flux in the transformer secondary center tapped coils, effectively no flux linking from secondary to the primary. Second, instead of one synchronous MOSFET and one coil of the center-tapped transformer, two synchronous MOSFETs and two transformer center tapped coils conduct simultaneously. Therefore, the secondary current will have only half the effective resistance, and losses are reduced by half compared to when only one synchronous MOSFET is ON (Figure 4).

Finally, in the conventional switching methodology, intentional dead time may be around 10% of the switching and during this dead time, high secondary current flows through the high forward-drop body diode of the MOSFET. By configuring the overlap of the

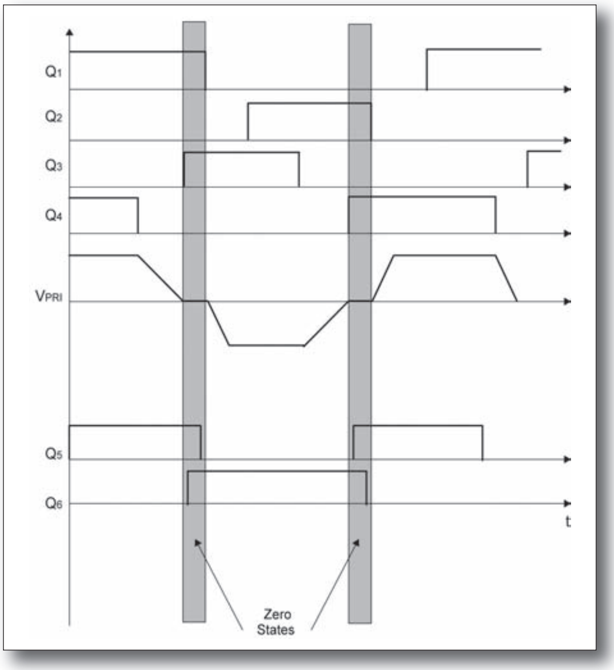

Figure 4: Overlapping Synchronous MOSFET Gate Drivers for Improved Efficiency

synchronous MOSFET's PWM gate drive, high secondary currents flow through MOSFET channel. In this instance, there will be only $R_{ds(ON)}$ losses, which are much less than the losses incurred by the MOSFET body diodes in the dead time. For a system with a telecom input (36 to 76 VDC), the DC/DC converter's efficiency improves anywhere from 3-4% by overlapping the synchronous MOSFET gate drive.

Implementing these techniques require a flexible power supply controller with completely independent PWM outputs. DSCs such as the dsPIC® DSC, offer the flexibility and PWM peripherals to easily implement this and other efficiency improving techniques.

Conclusion

The PSFB topology has the potential to achieve the efficiencies needed for modern power supplies. Digital control gives designers the ability to both control the PSFB topology very precisely and implement advanced control techniques, such as overlapping the synchronous MOSFETs. New topologies, new techniques, and new ideas are catapulting power supplies into the 21st century. Digital controllers such as the dsPIC DSC from Microchip are ready to take power supplies into the future.

Literature

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EconoPACK+ D-Series With Enhanced Characteristics

The EconoPACKTM+ is an innovative IGBT power module concept for very compact and high efficiency inverter designs with power ratings higher than 100kW. This power module concept was developed first by Infineon at the end of the 90 s [1]. Now after eleven years of EconoPACK+ experiences in the field it is the time to do the next step with a package upgrade and make the EconoPACK+ design fit for the future.

Wilhelm Rusche, Mark Essert, Christoph Urban, Infineon Technologies, Warstein, Germany

The first EconoPACK+ design was developed in a six-pack topology for a two level six pulse inverter [1]. Beside its initial purpose as a six-pack the module are very often used in parallel connection to increase the output power to several hundreds of kilowatts. In Figure 1 the EconoPACK+ and typical setups in high power frequency converters are presented.

Looking into the future, the triumphal procession of power electronics, and particularly the EconoPACK+, will go forward due to energy saving reasons e.g. in motion control and due to the still increasing demand of renewable energy systems in wind and solar applications. Moreover, power electronics will come more and more into consideration for further fields of applications. One of these new applications is the electric drive train in e.g. door to door delivery vehicles or in hybrid city busses. Such kinds of hybrid vehicles are covered by the group of commercial, agriculture and construction vehicles (CAV).

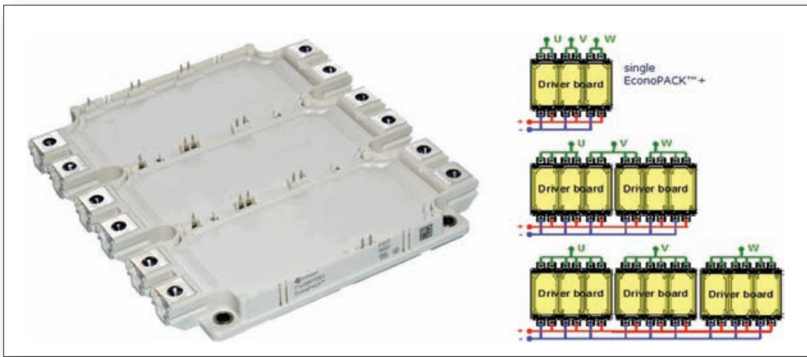


Figure 1: **EconoPACK™+ module and typical setups in high power frequency converters**

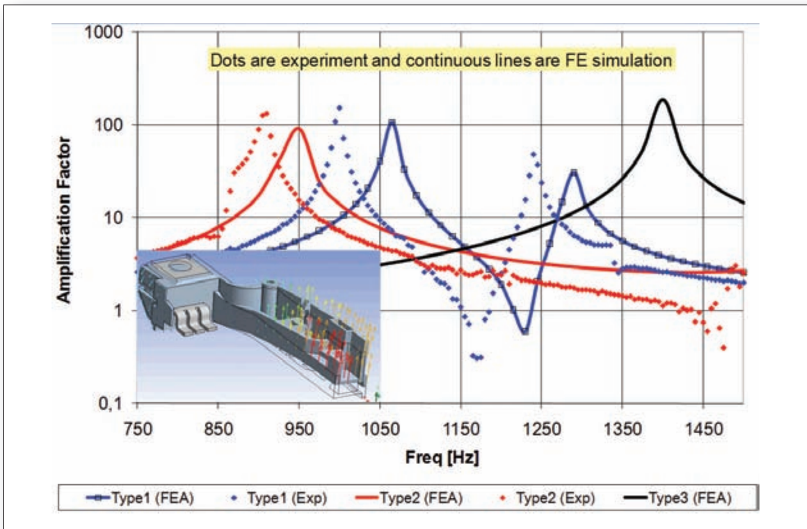


Figure 2: **Amplification factor of different designs, calculated and measured**

Based on the previous named applications and as a result of the energy saving and CO_2 reduction, the demand for robust and reliable power modules is growing more and more.

As power modules are not just excellent electronic devices but also units of significant mechanical size and weight, inverter designers have to take the mechanical robustness of the system into account. High power inverters with their huge capacitor bank and heavy output bus bars are having, depending on the application, more and more special requirements for mechanically rugged parts.

Mechanical ruggedness of the power module frame

Depending on the field of application, harsh vibration and shock conditions must be considered. Besides an adequate mechanical design of the inverter assembly to decouple the power electronics from destructive environmental conditions, the key devices such as capacitors and power modules should be self-protecting. Modules for CAV applications have higher requirements in vibration reliability. All the equipment, including the power module as a part of the power stage, installed into the vehicle has to withstand an increased vibration and shock load when the craft is in use. A rugged inverter- and power module frame design is needed to withstand environmental loads.

As a first indication of a rugged frame, the resonance frequency can be investigated. Finite element (FEA) analysis is carried out to compare different module package designs to ensure the highest possible ruggedness. Figure 2 shows a part of these results where the calculated and measured amplification factor of an external excitation of the package is compared. The most important point is the resonance frequency at which the maximum amplification occurs. The target of the design is to increase it above

1000Hz - significantly exceeding the conditions typically seen in the field.

In addition to the externally applied mechanical static- and dynamic stress, the frame also has to withstand stress caused by thermal changes. Furthermore the wear out of materials and joining zones is strongly depending on the level of the load applied, of the absolute temperature and the temperature change.

Thermal shock test

Thermally induced stress is addressed by the Thermal Shock Test (TST). This reliability test is a two chamber test which applies - as an accelerated test - an extremely hard temperature cycle to the devices under test (DUT). The DUT is moved periodically between two different chambers where it is stored for a period of time at -40°C and +125°C. This test with ΔT=165K has to be passed without failures at least 50 times.

The electrical contact technology as well as the power density has also to follow these requirements. For one decade of EconoPACK+ history, power contacts consisted of aluminium bond wires with their well known behavior. Driven by the ongoing increase of the power density of Silicon dies combined with rising junction operating temperatures T_{vjop} [2], power module designer strive for other joining technologies. On the way to higher power density, today's lifetime limitations of power contacts have to be overcome by new technologies.

Inherent advantages of ultrasonically welded joints

In high current applications, the limitations of aluminium bond wires become obvious. Paralleling multiple wires is needed to manage the temperature as depicted in Figure 3. To achieve a high current carrying capability, a robust and highly reliable power contact technology is needed. Ultrasonic metal welding (USW) contacts are able to handle all these requirements [3].

In Figure 3, a simulation of an US welded terminal compared to a power terminal solution with aluminium wires is given. Both simulations were made under identical boundary conditions. The results show a significant advantage of the ultrasonically welded terminal leading to an even reduced temperature down to approximately T=120°C.

This massive temperature reduction by ultrasonically welded terminals offers the opportunity to prepare the module for an increased rated current and thereby also for future chip generations. Figure 4 presents the temperature distribution of the EconoPACK+ power terminal at two different conditions derived from simulation.

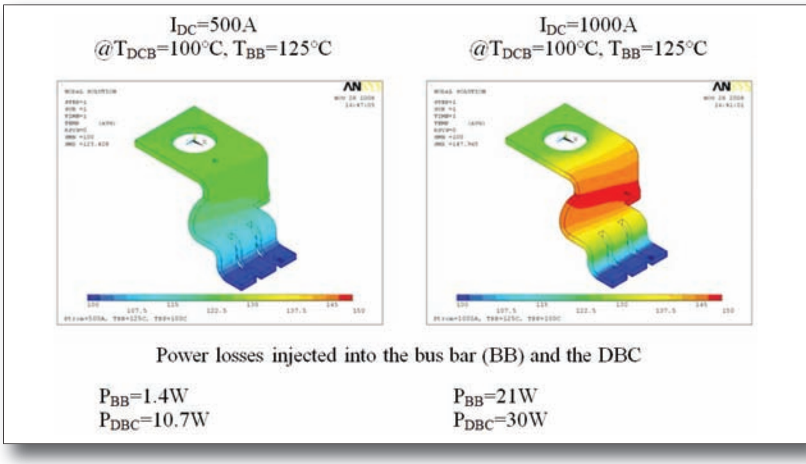


Figure 4: Power losses and resulting temperature distribution in a terminal at 500A and 1000A

The simulation of US welded terminals under two different conditions, presented in Figure 4, makes the advantages more obvious. For today's existing maximum DC current rating of the EconoPACK+, I_{Cnom}=450A, the new technology offers significantly reduced power losses in the terminal system itself and as a result of that a reduced operating temperature as well as lower mechanical stress in the device.

The previously given simulations are carried out to ensure the highest possible DC current under given conditions. In real applications the resulting temperatures especially at the power terminals are depending on the connected DC link design. A proper way for the investigation of a thermal behaviour is the measurement of the temperatures utilizing infrared thermographic camera systems (IR).

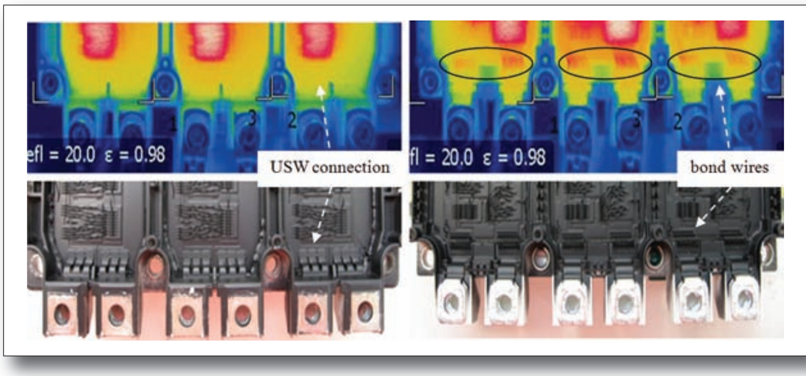


Figure 5: Thermographic picture of the wire bonded module (right) and the USW module (left)

To measure the temperatures most accurately, the IR system needs a black painted surface to take the temperatures by an infrared image. The measurement in Figure 5 compares USW terminals with wire bonded terminals, investigated by an IR system under identical load and cooling conditions. The hot bonds are clearly visible in comparison to the colder USW connections which adopt the same temperature as the substrates (DBC).

Ultrasonic welding is a kind of large-scale bonding. A welding tool induces ultrasonic energy and pressure on the movable joining partner. No consumables like solder or bond wire are needed. Even

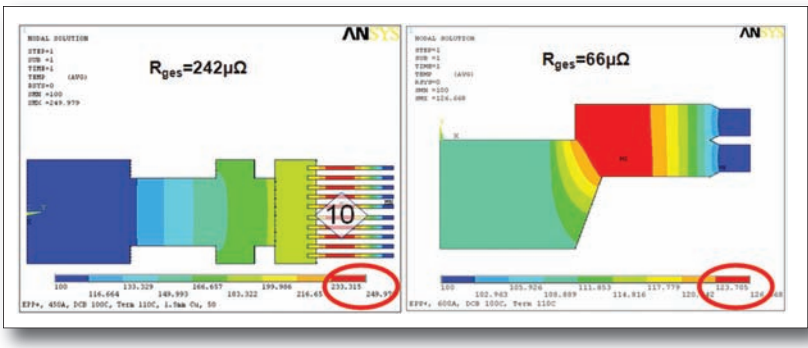


Figure 3: Simulated temperature distribution with aluminium bond wires vs. an US welded terminal

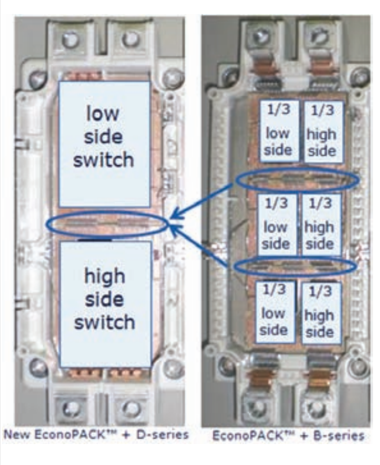


Figure 6: The difference of the system wire bonding between the EconoPACK+ D-series (left) and its predecessor (right) is exemplary shown for one segment per module

plating or additional cleaning is not required, therefore US welding of bare copper is the best possible technology from environmental point of view. By US welding of two identical partners, i.e. copper, the final result is a true metallurgical bond with the highest possible conductivity of the interconnection. As a consequence of both partners having the same Coefficient of Thermal Expansion (CTE), delamination effects of these joints are eliminated.

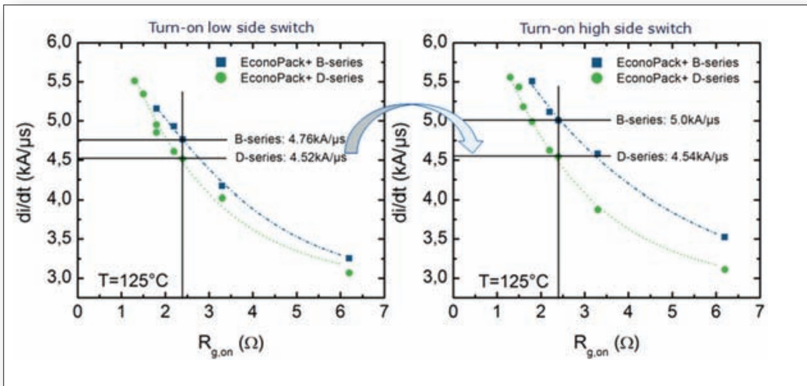


Figure 7: Turn-on of IGBT; di/dt=f(R_{gon}) for the new D-series FS300R12OE3 compared to the B-series FS300R12KE3

Optimized internal structures

Following the unwritten rule >>form follows function<< the DBC structure within the module is completely changed according to the electrical needs. In the new D-series, the layout of six larger substrates instead of nine smaller ones per power module is implemented (Figure 6). The reduction from nine down to six DBCs results in getting rid of one group of bond wire interconnections which reduces losses by reducing the resistivity.

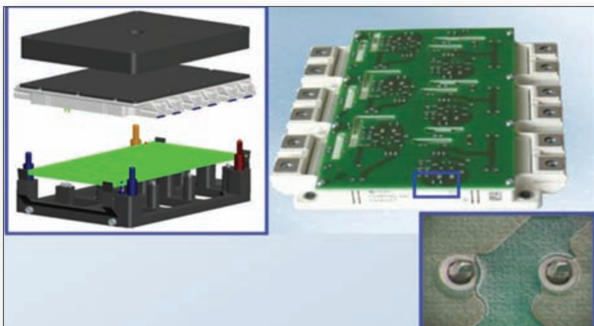
In addition to the reduction of the ohmic resistances, the IGBT and the associated reverse diode, build by paralleled single chips, are located in close vicinity on each of these big DBCs. This shortness of the distance results in a homogeneity of the current sharing and in an increased robustness of the diode by an increased surge current capability. Comparing the layout regarding the switching speed of the IGBTs, the new layout of top and the bottom switches leads to outstandingly symmetrical conditions.

As it is shown in Figure 7, an adjustment of the external gate resistance (or slightly reduction) is needed to the have a similar switching speed compared to the previous B-series. Based on this, similar turn-on losses and EMI behavior is reached. The losses during turn-off are unchanged due to a well known inherent IGBT behavior.

Reliable control connections

The EconoPACK+ redesign also takes care of the inverter system costs by providing reliable and solder less auxiliary contacts with PressFIT [5] technology. In Figure 8 the EconoPACK+ and the PressFIT tool is shown in the left part and in the right part the module with a pressed respectively mounted PCB on top is depicted. Analysis for today established soldering processes in combination with standard PCBs was deeply investigated also by an independent institute. The investigation results confirmed that the PressFIT contacts also provide the flexibility for today s established solder processes, if it is required by the user.

Figure 8: EconoPACK+ and the PressFIT tool on the left; pressed in PCB on the right



Conclusion

The increase in power density within standardized power module designs can no longer simply be achieved by the introduction of higher performance Silicon. Much more attention has to be paid on how the gain in performance can be made usable. The benefits of increased power density can only be achieved by an overall solution approach, including all functional groups within the module.

Higher reliability, increased current, future-proof design for upcoming chip generations and the integration of these features in a standardized footprint are the main challenges for a power module design. Furthermore a simple handling and mounting and the long term availability of the power devices are the main driver for new developments beside electrical aspects. All these aspects are addressed within the new EconoPACK+ D-series.

Beyond that the series allow for the use of today established mounting and assembling processes. All the previously described advantages also result in the possibility to increase the rated current. With this upgrade, the new EconoPACK+ is prepared for the requirements in power electronics for the next decade.

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Power Electronics Packaging Revolution Without Bond Wires, Solder and Thermal Paste

Power module packaging is driven by the ever increasing demand for higher power densities, reliability improvements and further cost reductions. The known reliability limitations of traditional solder joints and bond wires are holding back significant power density increases made possible thanks to higher junction temperatures and the future utilization of wide bandgap devices. Today, silver sintering has already started to replace the solder joint between chip and DBC substrate, leaving one major reliability bottleneck: the bond wire interface on the chip surface. **Peter Beckedahl, Manager Application and Concepts, Semikron, Nuremberg, Germany**

For some years now, the elimination of bond wires in power modules has been under discussion in industry and academia. Most of the new packaging approaches have been based on soldered or welded bumps, as well as on embedded interconnection technologies. The innovative packaging technology, named SKiN Technology, presented here takes the silver (Ag) sinter joint and applies it to all remaining interconnections in a modern power module. In addition to the double-sided sintering of power chips, the entire DBC is sintered to the heat sink. The resulting device has a very high power density and demonstrates remarkable thermal, electrical, and reliability performance compared to traditional packaging technologies.

Sinter technology

Silver sintering is an established technology which has started to replace the soldering of chips to DBC substrates in mass production. Thanks to its unprecedented reliability and thermal behavior, it makes power modules better suited to higher temperatures and demanding applications such as electric vehicles and wind turbines. However, two issues remain unaddressed: how to replace wire bonding on the chip top side, and how to connect the power module to the heat sink.

SKiN Technology resolves both these matters by using Ag sinter technology for all interfaces. The chip surfaces are sintered on the top side to a flex layer and the chip bottom to a DBC substrate, which in turn is sintered to a heat sink or base plate. Figure 1 shows a schematic drawing of this packaging technology. The special flex foil has a metal base power layer which is comparable to bond wire diameter in thickness and serves to connect the chip top surface. A thin metal layer on top represents the gate and sensor tracks which are connected to the power layer by vias. The two metal layers are insulated from each other by polyamide. The top layer can also be used for SMD components such as temperature sensors and gate resistors. The second sinter joint connects the back of the chip to a standard DBC substrate. All standard IGBT and diode chips can be used for this process, they need just an additional noble metal contact treatment on the chip top side.

The third joint connects the back of the DBC using large-area Ag sintering to an Aluminum (Al) pin fin water-cooled heat sink. The power terminals are sintered to the DBC in the same process step, resulting in a power module in which all interconnections are made with Ag sinter joints. The main advantages of the new SKiN Technology and its performance improvements are as follows:

- Power Density: The use of an Ag sinter layer instead of thermal paste will increase the power density as a result of the reduced thermal resistance chip to coolant. The large-area metal connection on the chip top surface will further improve the heat spread of the die.

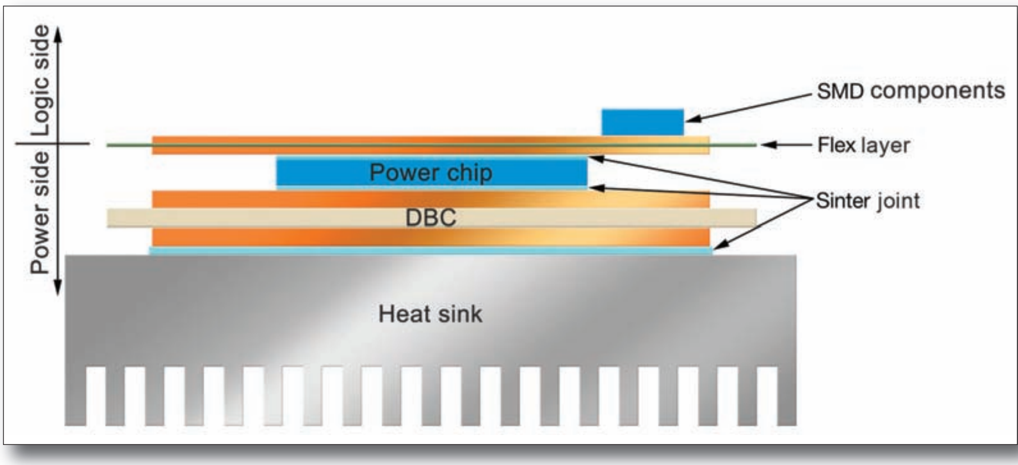

Figure 1: A schematic drawing of SKiN device

- Reliability: The replacement of Al bond wires by sintered flex foil will increase the power cycling capability thanks to better CTE (coefficient of thermal expansion) compatibility of the materials used, and the large-area connection between chip surface and contact medium.
- Electrical Properties: The use of the sintered flex foil instead of the Al bond wires will increase the maximum surge current rating of the dies as a result of the increased cross-section and area of the chip surface contact. In addition the module stray inductance is decreased due to a reduced loop geometry and wide traces.

Power module design

The prototype design used for this performance comparison is a 600V, 400A half-bridge power module with an aluminum pin fin heat sink.

The chipset of the prototype samples consist of 2 x 200A, 600V IGBT and 1 x 275A, 600V CAL freewheeling diode per switch. The power terminals are placed on the opposing short sides of the heat sink. The auxiliary contacts from the IGBT to the gate driver are provided by the flex layer itself, which is extended across the long side of the DBC (see Figure 2).

In order to benchmark the new packaging concept not only with traditional power module designs, identical devices have been built with standard Al bond wires for the die surface contact. To obtain maximum performance, each chip is contacted with 12 bond wires (see Figure 3). The surface of the diode is contacted with three stitches per wire; the IGBT with four stitches.

A significant difference between the flex layer and bond wire design is the contact area of the chip surface. While the bond wires are in contact with around 21 percent of the total metallized chip area only, the flex design exhibits a contact area of 50-85 percent, depending on the chip type.

Thermal resistance

The maximum power dissipation of the semiconductors is limited by the maximum junction temperature (T_j), the coolant temperature (T_a), and the thermal resistance (Rth) from chip to cooling medium according to the following equation:

$$P_v = \frac{(T_j - T_a)}{R_{th(j-a)}}$$

Especially in automotive applications where coolant temperatures above 85°C are needed, the temperature difference to the maximum allowed junction temperature becomes small which leads to reduced power densities and the need to reduce the thermal resistance to a minimum.

The new power module meets these requirements with a fitting solution: a high-density pin fin Al heat sink and an Ag sinter joint between the DBC substrate and the heat sink. No thermal paste is used, which has a significant contribution in the thermal performance of standard packages.

The measurements were performed using a three-phase automotive inverter setup (Figure 4) with a 50 percent glycol mixture and 70°C coolant temperature. The water inlet and outlet is on the left-hand side; distribution through the three modules is obtained using three parallel flow channels.

For the test all IGBTs are electrical

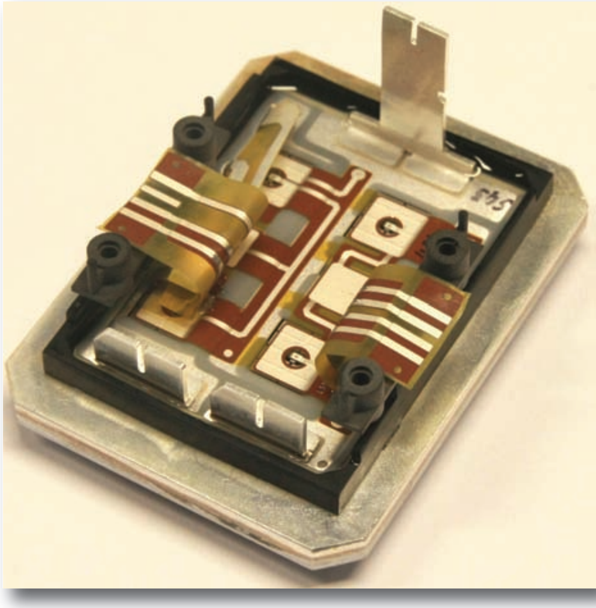

Figure 2: **SKiN half-bridge 600V/400A module**

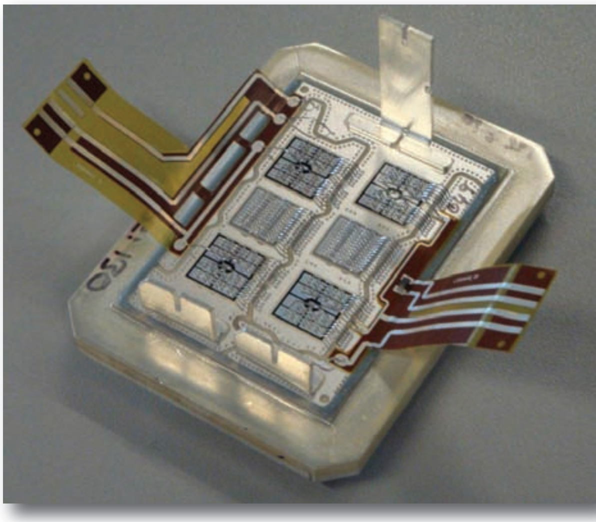

Figure 3: **Benchmark module with bond wires**

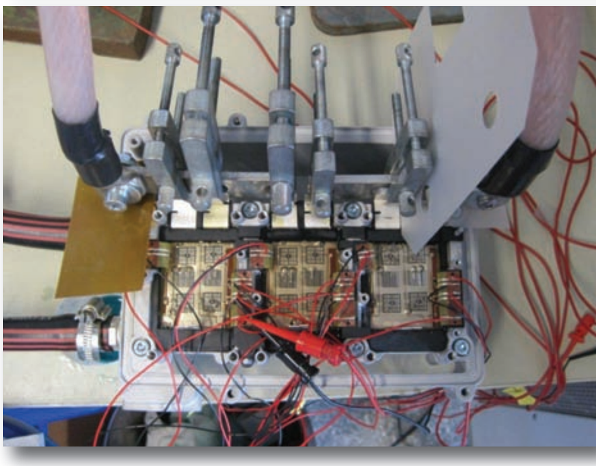

Figure 4: **Inverter setup used to measure thermal resistance**

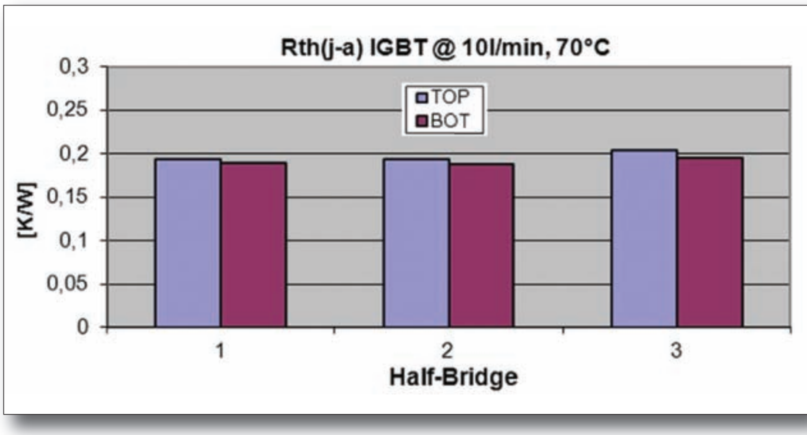

Figure 5: $R_{th(j-a)}$ of the six IGBT switches

connected in series and heated by an adjustable DC current. In this way it is possible to measure the power losses as well as the junction temperatures most accurately since it is not disturbed by switching transients.

The difference in thermal resistance (junction to water $R_{th(j-a)}$) between the upper (TOP) and lower (BOT) IGBTs, as well as the variation between the half-bridges is less than 10 percent and is shown in Figure 5. The lower switch of a half-bridge has a slightly better thermal resistance than the upper switch. This is due to the larger DBC copper area beneath these chips which leads to better thermal spread. This effect is well known in power module designs due to layout restrictions.

A summary of the thermal results is given in Table 1.The total thermal resistance $R_{th(j-a)}$ is exceptionally good, while the pressure drop remains at a very low level. A figure of merit is given in the second column were the thermal resistance is multiplied by the total chip area. This figure can be used for an easy comparison to competing solutions.

At a coolant temperature of 70°C, a flow rate of 10l/min and a maximum junction temperature of 150°C, it is possible to draw 205W/cm² chip area out of the system. Traditional high-power inverters with thermal paste between the power module and the water cooler reach just 100-150 W/cm² chip area. Please note that the flow rate in Table 1 is given for three half-bridges with parallel water paths. The flow per half-bridge is only one third of the total flow rate. Of course it is also possible to arrange the design with a serial coolant flow through the three phases which will lead to an even higher power density.

The question remains as to how a traditional module would perform if it were mounted on the same high-density Al pin fin cooler used for the SKiN module. To investigate this, thermal simulations were performed where the Ag sinter joint between DBC and heat sink was replaced by a thermal paste layer of only 20µm. Such a thin thermal paste layer is only possible using sophisticated pressure contact modules without baseplate, like the SKiiP or SKiM power module family. Modules with baseplate would require a much thicker thermal past of 80-150µm. The simulation results confirmed the large impact that the thermal paste layer has. Even for a layer of just 20µm, the total thermal resistance will increase by 23-30%, depending on the coolant flow rate.

SKiN Module		Benchmark Module	
Sample	A	Sample	A
Top	2666	Top	2092
Bot	2690	Bot	2108
Top	2691	Top	2105
Bot	2662	Bot	2096
Top	2696		
Bot	2662		
Top	2691		
Bot	2656		
min	2656	min	2092
max	2696	max	2108
mean	2677	mean	2100
	127%		100%

Table 2: Diode surge forward current (I_{FSM}) comparison

Surge forward current

The diode surge forward current (I_{FSM}) was measured using a standard half sine wave current surge of 10ms duration at 25°C. The results for maximum peak current level before destruction are displayed in Table 2.

The surge current rating of the flex layer module is 27 percent higher than the bond wire module. Due to the larger cross-section and shorter track length in the flex layer design, the surface contact fuses later than the bond wire module.

This behavior is particularly important for active front-end or generator applications, since it compensates for the reduced chip area which has been

SKiN Module IGBT			
Flow	$R_{th(j-a)}$	$R_{th(j-a)}$*A	Pressure Drop
	K/W	Kmm²/W	mbar
5l/min	0,225	45	30
10l/min	0,194	39	90
15l/min	0,182	36	185

Table 1: Summary thermal resistance

made possible from the improved thermal behavior of the integrated pin fin cooler.

Power cycling

Power cycling is the main qualification test to validate the lifetime required by the application mission profile owing to cycling loads. The most demanding applications are electric and hybrid vehicles, elevators, as well as wind turbines. The failure modes for power cycles are a combination of the typical bond wire lift-off and solder joint degradation in the layers below the chips. What cause of failure dominates depends on numerous factors such as cycle time and chip size. The replacement of the solder with a sinter layer has already eliminated one failure mode, leaving only the bond wire as the remaining reliability weak point. Single-sided sintered power modules have already in the past demonstrated a 2-3 fold improvement in power cycling.

Power cycling tests were performed on both module types under identical conditions with $\Delta T_j = 110$K (40°C to 150°C) and a complete cycle times of 14 seconds. The control strategy for the power cycling test was a fixed time adjustment, which is the harshest and most realistic test mode since it does not compensate for any type of degradation during the test.

Figure 6 shows the preliminary test results. The power cycling results for the benchmark modules are well within the expected curve (blue line) for single-sided sintered modules in the range of 60k cycles. The results for the SKiN power module by far exceed the target curve (red line), which is already 20 times higher than the industrial standard (green line). The modules passed more than 700k cycles until failure. In addition, short power cycles with a ΔT_j of 70K (80°C to 150°C) were started. Here the modules have already passed 3 million cycles. Tests will be continued to EOL (end of life).

The preliminary results demonstrate the unprecedented reliability of the new double-sided sintered power module. The target was exceeded, resulting in a 70-fold improvement in performance over the industrial standard and a ten-fold

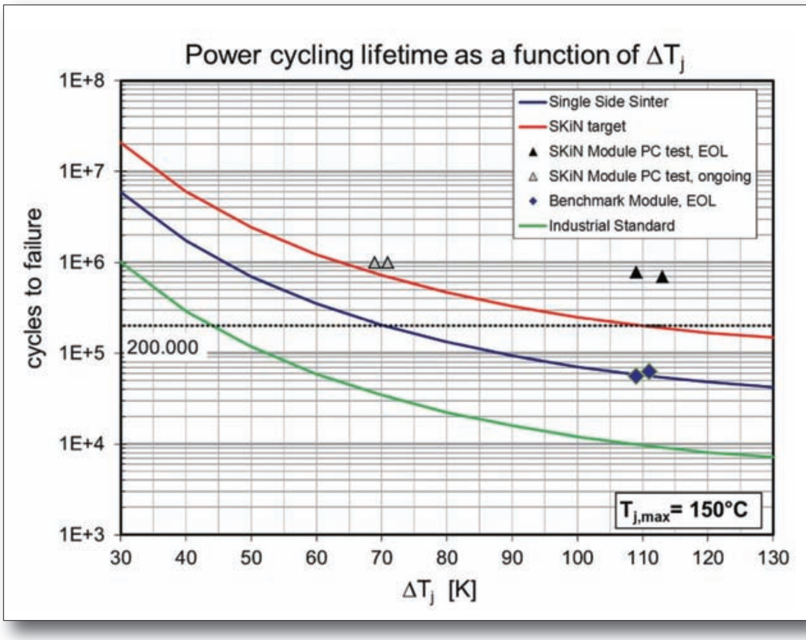

Figure 6: Preliminary power cycling results

improvement over the single sided sintered benchmark module.

It is important to mention that these results are from standard 600V IGBTs with a chip thickness of only 70µm and a standard Aluminum top side metallization. Only an additional thin noble metal surface finish is required. The SKiN packaging technology does not require any major changes in chip metallization materials or layer thickness.

Conclusion

SKiN Technology is a new packaging technology without bond wires, solder layers and thermal paste. All interconnections to chip top and bottom surface, DBC to heat sink and power terminals are made using Ag sinter joints. The bond wires have been replaced by a special flex foil which increases the chip surface contact area by a factor of 4.

In order to demonstrate the exceptional performance improvements of the overall system and in particular the flex foil, a comparison with a benchmark module featuring conventional Al bond wires was performed. Thanks to the elimination of thermal interface materials and the integration of a high-performance pin fin heat sink, it is possible to double the power dissipation in comparison to conventional designs. The elimination of the thermal paste layer alone leads up to a 30 percent improvement in the total thermal resistance junction to water. Owing to the modified geometry and increased chip contact area, a 27 percent increase in diode surge forward current capability has been achieved.

The power cycling performance demonstrates an unprecedented 70-fold improvement over the industrial standard and a 10-fold improvement over the single-sided sintered benchmark module. Further activities are underway in order to exploit the new possibilities of the dual-layer flex foil. These are, in particular, a further improvement in thermal resistance resulting from double-sided cooling and the integration of passive and active components for gate drive, current and temperature sensing.

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Demonstration of 10kW SiC Half Bridge DC/DC Converter

In PEE's Special Session at PCIM 2011 the results of a 10kW transformer isolated DC/DC converter using 1.7kV SiC MOSFETs were presented. The converter is a half-bridge topology operating at 32kHz hard-switched with a link voltage of 1kV. An efficiency of 97.1% was demonstrated and was achieved without extensive optimization. The characteristics of the 1.7kV SiC MOSFET, design details of the converter, and measured results are presented in this article. **Robert Callanan, Cree Inc., Durham NC USA**

The recent commercial introduction of the SiC MOSFET [1] represents one of the most significant advances in power electronics in the past 25 years. Simple topologies that have been considered impractical with Silicon switching components become practical with the SiC MOSFET.

This is especially true with the 1.7kV SiC MOSFET which has an unprecedented combination of low conduction loss and low switching loss. A key factor in accelerating the adoption of these devices is the ability to provide a generic but meaningful means of adequately demonstrating the key advantages of this technology. This means operating the device under full power conditions which usually require the use of a high power source and load. Unfortunately, this is most inconvenient when the power levels are 10kW and above.

Figure 1: **1.7kV SiC MOSFET with 1.7kV, 10A JBS diode in TO-258 package co-pack**

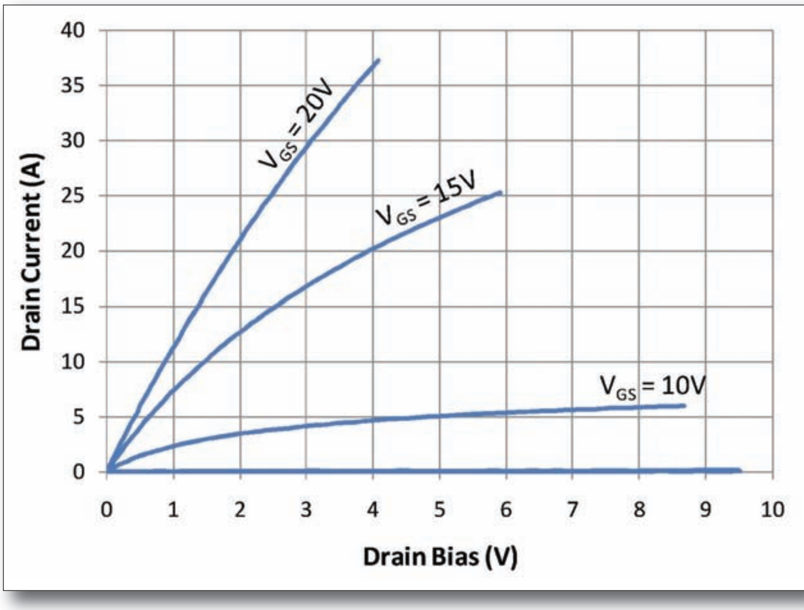

Figure 2: **Forward I-V characteristics of 1.7kV MOSFET with V_{GS} of 0V, 5V, 10V, 15V and 20V**

The approach taken in this work [2] was to construct a DC/DC converter and feed the output current back to the input similar to what is done for motor/drive testing. The converter delivers full power, but the power source need only deliver the circuit losses. This approach also gives a direct measurement of the total system power loss. Power conversion systems requiring 1.7kV switches typically utilize Si IGBTs or a multiplicity of Si MOSFETs. The switching loss of 1.7 kV Si IGBTs operating under hard switched conditions can efficiently operate at relatively low frequencies (~ 4kHz). Higher frequencies can be achieved by employing resonant topologies to mitigate the tail current losses. However, this requires additional resonant components and increases the RMS currents in the power components. Another alternative for 1.7kV high frequency applications is to use multiple lower voltage Si MOSFETs in a multi-level topology. Hard switching was employed at 32kHz with a 1kV link to show high frequency operation under these conditions is easily achieved without reverting to resonant or multi-level techniques to achieve good efficiency at this operating frequency.

1.7kV SiC MOSFET

MOSFETs fabricated in 4H-SiC with capabilities for blocking in excess of 1.7kV and conducting 20A continuous current have been recently presented in the literature [3]. The switch consisted of a 1.7kV MOSFET and a 1.7kV 10A SiC JBS diode co-packed in a TO-258 package (see Figure 1). The DMOSFET die size is 4.08mm x 4.08mm, the JBS diode die size is 2.70mm x 3.81mm. The forward characteristics of the MOSFET are presented in Figure 2. The on-resistance of the device is less than 80 mΩ with 20V gate drive. Breakdown starts to occur at

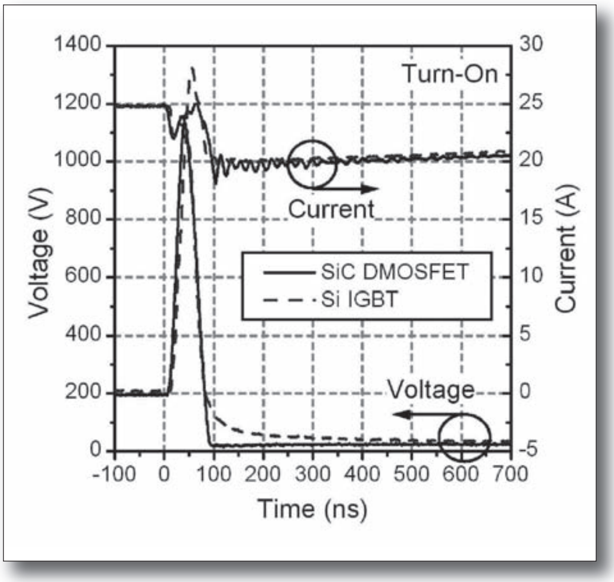

Figure 3: Turn-on characteristics

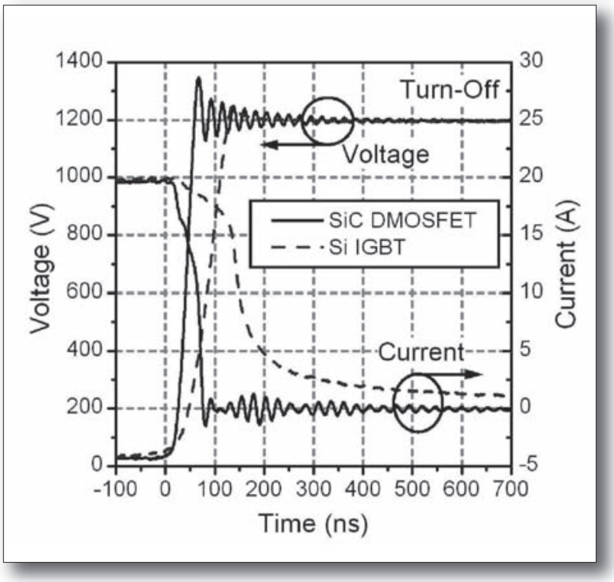

Figure 4: Turn-off characteristics

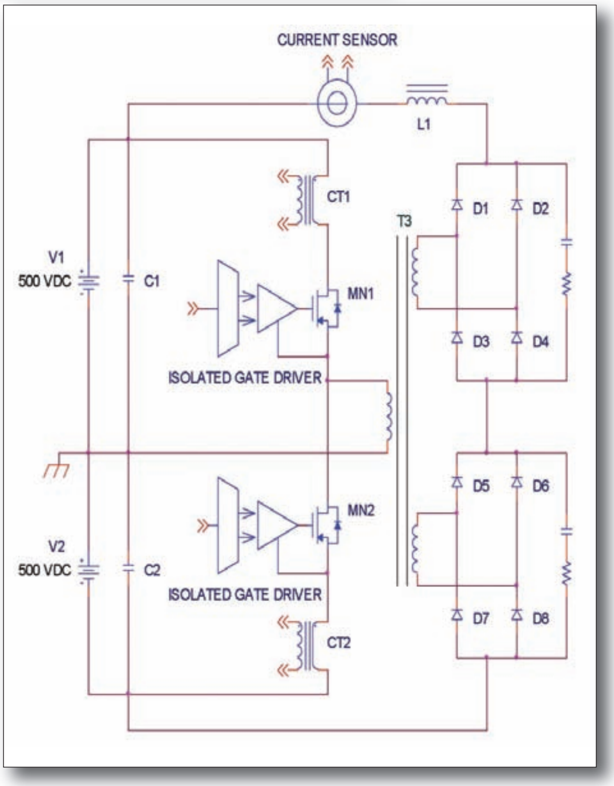

Figure 5: 10kW MOSFET demonstrator schematic diagram

2kV and the leakage at zero gate bias is less than 15nA at 1.7kV.

The turn-on and turn-off switching characteristics of the SiC MOSFET compared to a 1.7kV 34A Si IGBT [2] are shown in Figures 3 and 4 respectively. As shown in Figure 3, the SiC MOSFET voltage fall is very crisp and does not have the tail present in the Si IGBT voltage fall. Figure 4 illustrates that the SiC MOSFET does not have a current tail whereas the Si IGBT does resulting in significantly higher turn-off loss.

Demonstrator design

The purpose of the demonstrator is to exercise the aforementioned SiC MOSFET under high power conditions. The topology chosen for this demonstrator is a half-bridge hard-switched DC/DC converter. The half-bridge was chosen for two reasons. First, it demonstrates a totem-pole of two switches. This is the fundamental building block for high power inverters and motor drives. Second, it is very easy and convenient to construct; the split DC link can be realized by two commonly available DC power supplies that can both be referenced to ground. The schematic of the circuit is shown in Figure 5.

The topology shown is a hard-switched half-bridge transformer isolated DC/DC converter operating at 32kHz. Input power is provided by two series connected 500V DC power supplies (V1, V2) to construct a 1kV DC center tapped link. The half-bridge consists of a pole of two 1.7kV SiC MOSFET and 1.7kV 10A JBS co-packs (MN1, MN2), each driven by isolated gate drivers. The gate drivers provide a +20V/-5V gate drive pulse. Current transformers CT1 and CT2 sample the switch current. The two secondaries feed two series connected bridge rectifiers. The conservative two-bridge approach was chosen to provide ample margin for reverse voltage overshoots. The bridge rectifiers are comprised of commercially available Cree C2D10120A 1.2 kV 10A SiC JBS diodes. The output of the bridge rectifiers feeds inductor L1. The output current of the converter is fed back to the input as shown. The controls were implemented with a standard Texas Instruments UC3825A pulse to pulse current mode controller. The current mode controller provided pulse to pulse peak current control for the two switches. The current through each switch is sensed by two current transformers (CT1 and CT2). A Hall-effect current sensor is used to sample the current delivered by the converter. An error amplifier compared the value to a reference to regulate the delivered current back into the 1kV link to

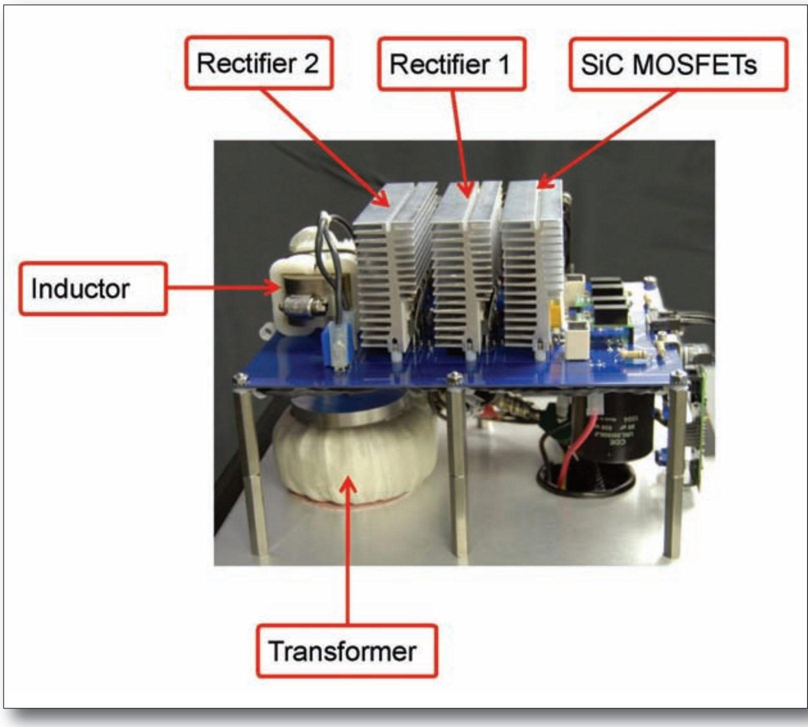

Figure 6: **10kW MOSFET demonstrator hardware**

a nominal 10A DC. This results in 10kW of delivered power from only two SiC MOSFETs.

The actual hardware is shown in Figure 6. The power semiconductors are mounted on standard heat sink extrusions using forced air cooling. The 10kW step-up transformer employed a Vacuumschmelze T60004-L2080-W436 nanocrystalline toroid core. The dimensions of the core were ID=80mm, OD=63mm H=25mm with a cross sectional area of 1.62cm^2. The maximum operating flux density was 0.49T. The windings were comprised of Litz wire consisting of 210 strands of AWG 36 wire. The primary was 42 turns wound two in hand and the secondaries were 50 turns. Transformer cooling was accomplished by conduction to base plate. The output inductor L1 is 880µH and utilized a Metglas AMCC-32C core with 38 turns of the aforementioned Litz wire. No attempt made to mitigate effects of fringing flux. Cooling of the output inductor employed a combination of natural convection and a small amount of forced air.

Demonstrator results

The DC/DC converter delivered 10.44kW at 1kV DC with only 308W of loss. Figure 7 shows the output waveforms of the half-bridge inverter taken at the common point of MN1 and MN2. The blue waveform is the output voltage showing a 1.022kV peak to peak amplitude. The red waveform is the output current showing 23.77 A RMS. The distribution of loss is listed in Table 1. The table lists measured loss as is and optimized loss with a few basic modifications.

The switching loss for both SiC MOSFETs was 34W and conduction loss was 42W for both devices. This equates to 17W switching loss and 21W conduction loss per SiC MOSFET (38 W total losses for each device). Note, the modest amount of SiC MOSFET switching loss shows that hard-switching operation at frequencies higher than 32kHz are definitely possible. The 60W of transformer loss breakdown was 10W core loss and 50W conductor loss.

The Litz wire was not selected for minimum loss. Therefore, a simple change in Litz wire design would result in a reduction of loss by perhaps 10W. The 112W of rectifier and snubber loss breakdown was 33W for each bridge and 46W for the snubber. This can obviously be improved by going to a single bridge with a more efficient snubber. The projected reduction in loss would be approximately 66W. The 56W of inductor loss breakdown was 39W core loss and 17W conductor loss. The 17W conductor loss breaks down to 5W for the DC current component and 12W for the AC component. As previously mentioned, no attempt was made to mitigate fringing flux effects. The inductor loss can be reduced by replacing the Metglas core with a nanocrystalline cut core and by using a multi-gapped design to minimize the fringing flux effects. These changes would reduce the inductor power loss by approximately 20W. The net effect of these modifications would reduce the total power loss from 308W to 212W with a resulting improvement of efficiency at 10.44kW from 97.1% to 98%. More aggressive techniques can be used to increase the efficiency further.

The SiC MOSFET heatsink temperature rise was only 28.8°C. The worst case rectifier heat sink rise was only 17.1°C. The hottest component was the transformer. An experiment was done where forced convection cooling was used and the transformer surface temperature dropped to approximately 38°C, only 13°C temperature rise.

Conclusions

The 1.7kV SiC MOSFET has an unprecedented combination of low conduction loss and switching loss. The demonstrator shows how two of these

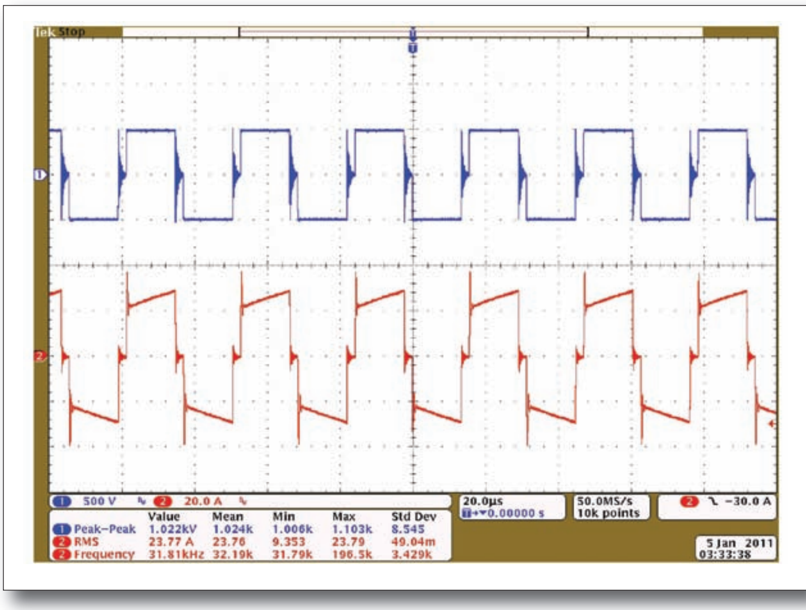

Figure 7: **Half-bridge inverter output waveforms at 32kHz (blue = voltage 500V/div, red = current 20A/div, time = 20µs/div)**

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Table 1: Loss distribution of 10kW SiC DC/DC converter

Component	Loss	
	Measured	Optimized
SiC MOSFETs Switching	38 W	38 W
SiC MOSFET Conduction	42 W	42 W
Transformer	60 W	50 W
Rectifiers & Snubbers	112 W	46 W
Inductor	56 W	36 W
Total Loss	308 W	212 W
Efficiency @ 10.44kW	97.1%	98%

1.7kV SiC MOSFETs can easily realize a 10kW, 1kV hard-switched DC/DC converter operating at 32kHz with an efficiency of 97.1% without extensive optimization. Higher efficiency can be achieved through some basic modifications. The modest switching loss of the SiC MOSFET allows higher switching frequencies using hard-switched topologies is definitely possible. This technology enables substantial improvements in size, weight, and efficiency in all aspects of power conversion such as 690V motor drives, auxiliary power converters for traction, solar inverters and wind applications to name a few. This performance utilizing a very simple and robust half-bridge hard-switched topology would be difficult, if not impossible, using Silicon IGBTs.

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Multiphase DC/DC Converters Save Power in Data Centers

The need to reduce the power dissipation in data centers will be a major focus for the next several years. Designers of POL DC/DC converters for almost any kind of system face many challenges due to the multiple constraints of limited space and cooling within a given enclosure, as well as the need for high efficiency throughout the entire load range. Despite having to navigate through this myriad of constraints, many of the recently introduced multiphase regulators provide a simple, compact and efficient solution. By moving toward the diverse multiphase topologies, designers can effectively save space, simplify layout, lower capacitor ripple current, improve reliability and reduce the amount of power wasted as heat.
Bruce Haug, Senior Product Marketing Engineer, Power Products, Linear Technology Corporation, Milpitas, USA

The electricity consumption of data centers worldwide has become an important issue in recent years as demands for Internet services grow significantly. Data centers can serve up web pages, enable social networking, stream media, provide music and video downloads, allow Internet access, and run simulations. They also provide computing power for traditional and private users for banking and other financial transactions. Data centers fill rooms, floors or even entire buildings that house computer, storage and networking equipment. The aggregate electricity used for data centers doubled worldwide from 70 billion kWh/yr in 2000 to 140 billion kWh/yr in 2005, and continues to grow at an average of 16.7% per year, with the Asia Pacific region (without Japan) being the only major world region with growth significantly exceeding that average [1].

Higher efficiency power conversion

The computers used in data centers, commonly called servers, are similar to PC architectures, with a CPU, ASICs, FPGAs and memory. However, unlike PCs, servers in data centers are packed together as densely as possible and use substantial amounts of electricity, producing heat, which must then be dissipated. Power is delivered to these servers via uninterruptible power systems (UPS), typically followed by a distributed power system and then step-down DC/DC converters for point-of-load (POL) powering. These power delivery methods are not 100% efficient and produce copious amounts of heat as well. This heat must be carefully and continuously managed to keep the systems running within their specified operating temperature ranges. Regardless of the type and efficiency of the cooling system, heat must be removed from the data center in some way. To do so requires additional energy to operate the cooling infrastructure.

The data centers' incremental overhead power consumption, due to inefficiencies and cooling systems is estimated to be equal to the amount of power that is consumed by servers, storage and networking. The user of a single PC, workstation, or laptop doesn't see system heat generation as a concern, but for data centers, managing this thermal overhead is as important as the servers themselves. If system power is reduced, then the available overhead can handle a greater IT load and perform more useful work in the same power envelope.

As the data center power demand continues to increase, higher efficiency power conversion is required to reduce the amount of power wasted as heat. Smart multiphase controller technology is an excellent solution for high current POL applications. This architecture allows a high current regulator to achieve well over 90% efficiency at full load. However, most designs do not address the need for higher efficiency at light to medium loads. Wasted power at a light to medium load is just as important to save as wasted power at heavy loads.

Most embedded systems are powered via a 48V backplane. This voltage is normally stepped down to a lower intermediate bus voltage of 24V, 12V or 5V to power the racks of boards within the system. However, most of the sub-circuits or ICs on these boards are required to operate at voltages ranging from sub-1V to 3.3V at currents ranging from tens of milliamps to hundreds of amps. As a result, point-of-load DC/DC converters are necessary to step down from either of the 24V, 12V or 5V voltage rails to the desired voltage and current level required by the sub-circuits or ICs.

It is clear that the growing demand for increased current at ever decreasing voltages is driving power-supply development. Much of the progress in this area can be traced to gains made in power conversion technology, particularly improvements in power ICs and power semiconductors. In general, these components contribute to enhancing power supply performance by permitting increased switching frequencies with minimal impact on power-conversion efficiency. This is made possible by reducing switching and on-state losses thereby increasing efficiency while allowing for the efficient removal of heat. However, the migration to lower output voltages places more pressure on these factors, which in turn, creates significant design challenges.

Multiphase topology

Multiphase operation is a general term for conversion topologies where a single input is processed by two or more converters, where the converters are run synchronously with each other but in different, locked phases. This approach reduces the input ripple current, the output ripple voltage and the overall RFI (radio frequency interference) signature, while allowing high current single outputs, or multiple lower current outputs with fully regulated output voltages. It also allows smaller external components to be used, producing a higher efficiency converter and also providing the added benefit of

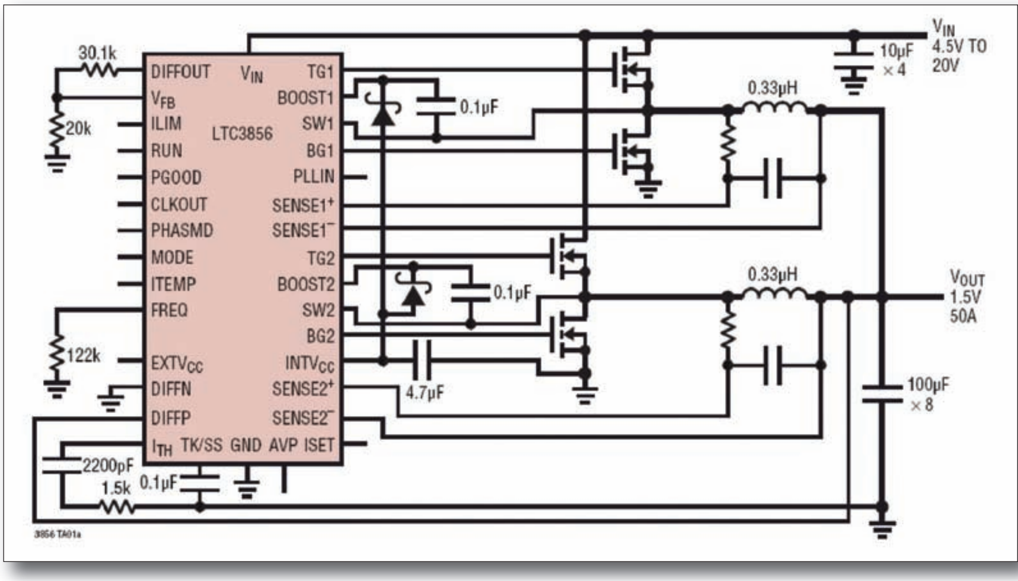


Figure 1: **High output current 1.5V/50A application schematic**

improved thermal management with less cooling.

Multiphase topologies can be configured as step-down (buck), step-up (boost) and even as a forward converter, although generally the buck regulator is the more prevalent application. Conversion efficiencies of up to 95% from 12V in to 1.xV out are commonplace today.

At higher power levels, scalable multiphase controllers reduce the size and cost of capacitors and inductors using input and output ripple current cancellation caused by interleaving the clock signals of several paralleled power stages. Multiphase converters help minimize the external component count and simplify the complete power supply design by integrating PWM (pulse width modulation) current mode controllers, remote sensing, selectable phasing control, inherent current sharing capability, high current MOSFET drivers plus over-voltage and over-current protection features. The resulting manufacturing simplicity not only helps improve power supply reliability, but it is also scalable. Such systems can be expanded up to 12 phases for high current outputs as high as 300A.

Linear Technology has several multiphase DC/DC controllers, including the LTC3856 and LTC3829 single output synchronous step-down controllers for high current POL conversion. Not only can these parts increase full load efficiency, but they also have an optional Stage Shedding™ feature that decreases light to medium load power loss as well. The circuit in Figure 1 shows a typical LTC3856 application schematic for developing a 1.5V/50A output from a 4.5V to 14V input voltage using two phases. Figure 2 shows a typical LTC3829 application schematic for developing a 1.2V/75A output from a 6V to 28V input voltage with three phases.

The LTC3856 has two channels and up

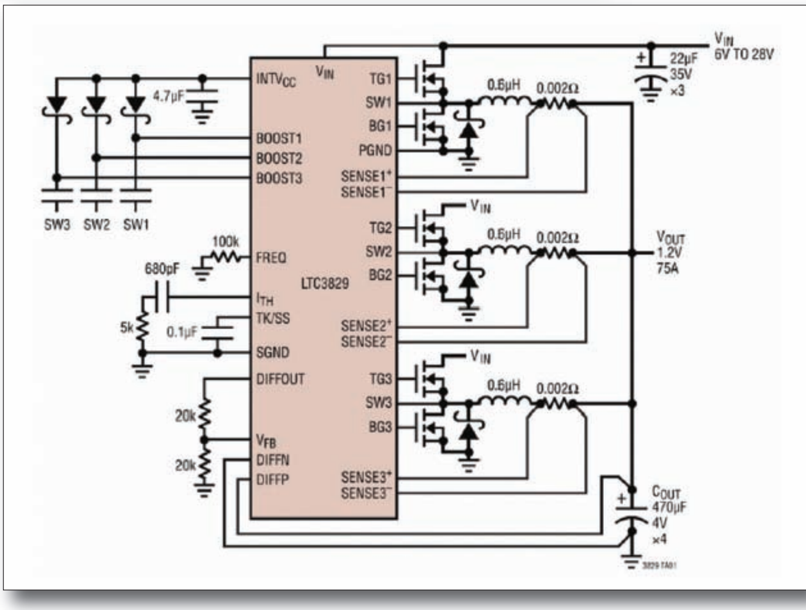


Figure 2: **High output current 1.2V/75A application schematic**

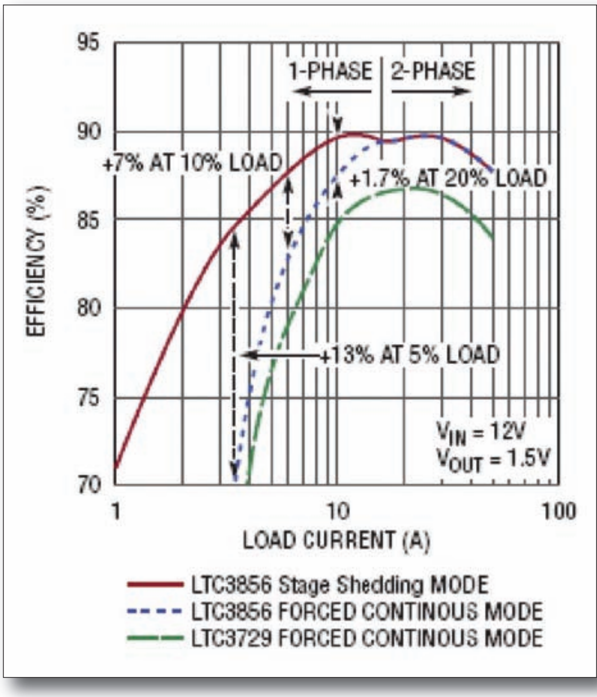


Figure 3: **LTC3856 efficiency curve with stage shedding phase vs. an older controller**

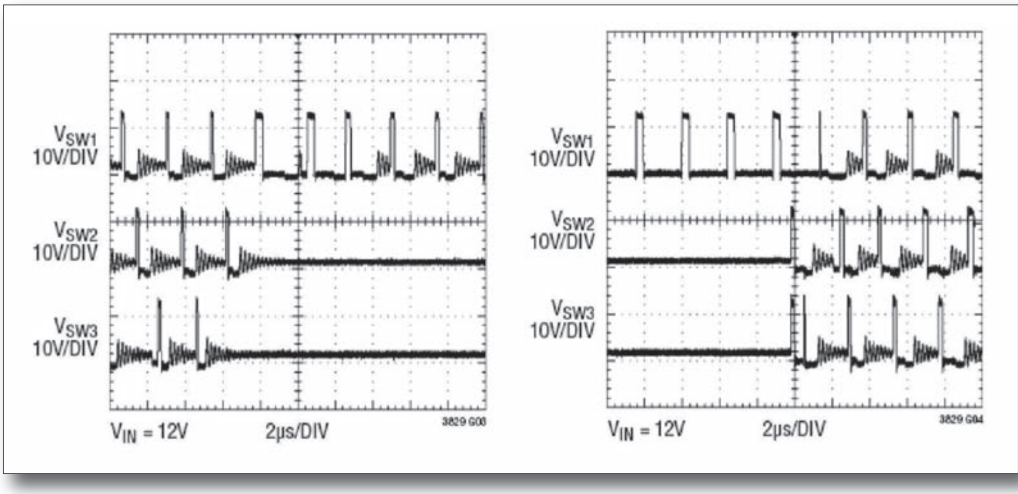


Figure 4: Going into stage shedding (left) and coming out of stage shedding

to 12 phases possible with multiple ICs. The LTC3829 has three channels and can operate at up to 6 phases when used with two ICs. The onboard differential amplifier provides true remote output voltage sensing of both the positive and negative terminals, enabling high accuracy regulation independent of IR losses in trace runs, vias and interconnects.

These controllers operate with all N-channel MOSFETs from input voltages ranging from 4.5V to 38V, and can produce ± 0.75% accurate output voltages from 0.6V to 5V. The output current is sensed, monitoring the voltage drop across the output inductor (DCR) for highest efficiency or by using a sense resistor. Programmable DCR temperature compensation maintains an accurate over current limit set point over a broad temperature range. The powerful onboard gate drivers minimize MOSFET switching losses and allow the use of multiple MOSFETs connected in parallel. A fixed operating frequency can be programmed from 250kHz to 770kHz or synchronized to an external clock with its internal PLL. A minimum on time of just 90ns makes the LTC3729 and LTC3856 ideal for high step-down ratio/high frequency applications.

Stage shedding operation

At light loads, switching-related power losses normally dominate the total loss of a switching regulator. Eliminating the gate charge and switching losses of one or more of the output stages during a light load will significantly increase efficiency.

Stage Shedding allows one or more phases to be shut down to reduce switching related losses during a light load condition and is typically used when the load current is reduced to less than 15A. The overall efficiency can be increased by up to 13%, as shown in Figure 3. This figure also shows the efficiency of an older comparable LTC3729 2-phase controller. Due to the stronger gate drive and shorter dead time, the LTC3856 can achieve 3-4% greater efficiency than the LTC3729 over the whole load range.

Stage shedding operation is triggered when the onboard feedback error amplifier output voltage reaches a user-programmable voltage. At this programmed voltage, the controller shuts down one or more of its phases and stops the power MOSFETs from switching on and off. This ability to program when stage shedding takes place provides the flexibility to determine when to enter this mode of operation. The diagrams in Figure 4 show the SW waveform and how the LTC3829 goes into and out of stage shedding operation.

The LTC3856 and LTC3829 can operate in any of three modes: Burst Mode® operation, forced continuous or Stage Shedding mode, all of which are user selectable. At heavy loads of greater than 15A, these devices operate in constant frequency PWM mode. At very light loads, Burst Mode operation can be selected and produces the highest efficiency at load currents of less than 0.5A. Burst Mode operation switches in pulse trains of one to several cycles, with the output capacitors supplying energy during internal sleep periods.

Active voltage positioning

The LTC3856 and LTC3829 also have Active Voltage Positioning (AVP), which reduces the maximum voltage deviation during a step load and reduces the power dissipation at heavier loads further increasing its efficiency. Figure 5 shows the difference in behavior between the circuit in Figure 1 with and without AVP. Without AVP, the maximum voltage deviation for a 25A step load is 108mV. With AVP, the maximum voltage deviation is 54mV for the same 25A step load. In addition, the output voltage drops by 54mV with AVP when the output current goes from 25A to 50A, resulting in a lower 2.7W dissipation by the load.

Literature

[1] Worldwide electricity used in data centers, Jonathan Koomey, Lawrence Berkeley National Laboratory, 2008

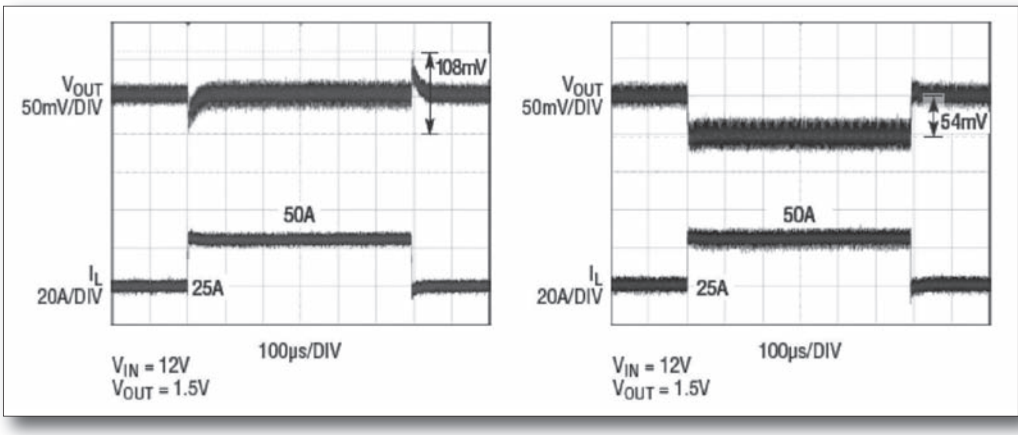


Figure 5: Load step characteristics without (left) and with Active Voltage Positioning

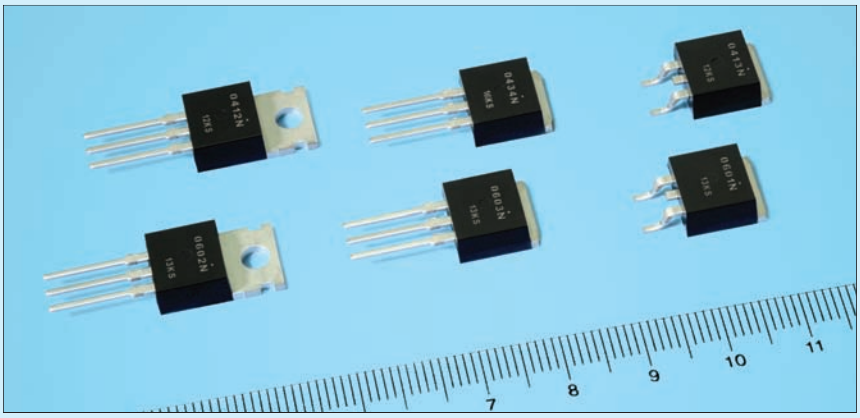
Super Capacitor Manager

Texas Instruments introduced the industry's first fully integrated Li-Ion battery management integrated circuit (IC) for super capacitor charge control. This single device provides comprehensive features for managing charge control; measuring capacitance and effective series resistance (ESR); and protecting either 2-, 3-, 4- or 5-series super capacitors with individual capacitor control, or up to 9-series capacitors with stack control.

The bq33100 maximizes functionality and safety, while increasing ease of use and cutting the solution cost and size for super capacitor applications.

www.ti.com/bq33100-preu

Cordless Power Tool MOSFETs



Renesas Electronics now offers high-current Power MOSFETs for motor drive in consumer products, such as cordless power tools and power-assisted bicycles. In recent years, the market for cordless power tools has seen an increase - especially among high-end models - in the use of brushless motors and other power efficiency measures to increase battery life. The power supply circuit of a typical power tool contains six Power MOSFETs, and there is increasing demand for MOSFETs with low on-resistance. Thus the company has designed six new low-loss power MOSFETs to accommodate large currents of up to 100A.

The 40 V N0413N has an on-resistance of 2.7 mΩ, and the 60 V N0601N of 3.3 mΩ (V_{GSS} = 10 V standard value in both cases) in TO-220AB and TO-262 and the surface-mount TO-263 packages.

www.renesas.eu

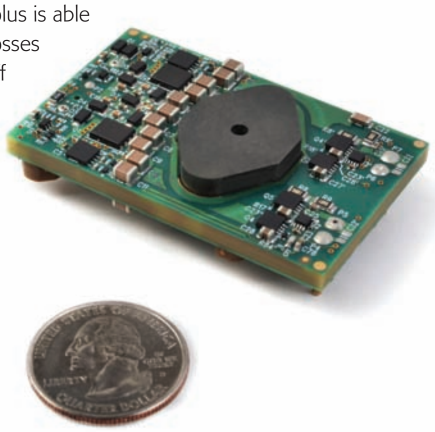
Automotive 3-Phase MOSFET Pre-Driver IC

The new A4933 from Allegro MicroSystems Europe is an automotive-grade 3-phase MOSFET pre-driver IC for the control of brushless DC motors in applications such as electronic power steering systems, engine cooling fans, transmission actuators and hydraulic pumps. The device is primarily targeted at extreme applications where high power, high torque and high temperature combine to require a MOSFET pre-driver that is able to deliver large MOSFET gate drive and switching capabilities. It is particularly suited to use in 3-phase systems, especially those which use sinusoidal control of the motor phase currents. This commutation method provides smooth operation, which reduces audible noise and minimises torque ripple at the load. Key features of the A4933 include an integrated charge pump that provides full gate drive for battery voltages down to 7 V and reduced gate drive for battery voltages as low as 5.5 V; a top-off charge pump that enables 100 % PWM; an adjustable dead time that can be regulated by the user; an adjustable drain-to-source monitor; and improved fault diagnostics that enhances the ability to decode and identify faults. The A4933KJPTR-T is available in a 48L eLQFP small-profile thermally efficient package with exposed pad.

www.allegromicro.com/en/Products/Part_Numbers/4933/4933.pdf

720 W Isolated DC/DC Quarter Brick

CUI Inc introduced the engineering release and initial sampling of the NQB isolated DC/DC quarter brick. The 720 W intermediate bus converter will initially support an input range of 36-60 V with an output of 12 V and will provide an efficiency greater than 96%. The NQB product will eventually support a wider input range as well as an output of 9.6 V. Additional features include options for DOSA footprint compatibility, remote on/off, and load share capability. CUI's Solus Topology integrates a conventional buck converter into a SEPIC converter to form a totally new SEPIC-fed buck converter; a patented single stage topology with one magnetic element, one control switch and two commutation switches that are PWM controlled. With lower voltage and current stresses in the topology coupled with an inherent GCE (gate charge extraction) process, Solus is able to reduce switching turn-on losses by 75% and switching turn-off losses by 99% on the control FET when compared to a conventional buck converter. The topology further increases total efficiency by distributing the energy delivery into multiple paths, reducing circuit conduction losses by nearly 50%.



www.cui.com

PV Cell Bypass Protection Schottky Rectifiers

Vishay Intertechnology Inc. expanded its offering of Trench MOS Barrier Schottky rectifiers with 12 new 45 V devices in three power package options that feature a wide range of current ratings from 10 A to 60 A. With low forward voltage drops down to 0.33 V typical at 10 A, the rectifiers are optimized for use in solar cell junction boxes as bypass diodes for protection. The devices include the dual-chip V(B,F)T1045CBP, V(B,F)T2045CBP, V(B,F)T3045CBP, and V(B,F)T6045CBP. Each device is offered in the power TO-220AB, ITO-220AB, and TO-263AB packages. All rectifiers feature a maximum operation junction temperature of 150°C and ≤ 200°C maximum junction temperature in DC forward current without reverse bias (t ≤ 1 hour). The TO-263AB package offers a moisture sensitivity level (MSL) of 1, per J-STD-020, LF maximum peak of 245°C. The TO-220AB and ITO-220AB packages feature solder bath temperatures of 275°C maximum, 10 s, per JESD 22-B106, and are halogen-free according to the IEC 61249-2-21 definition.

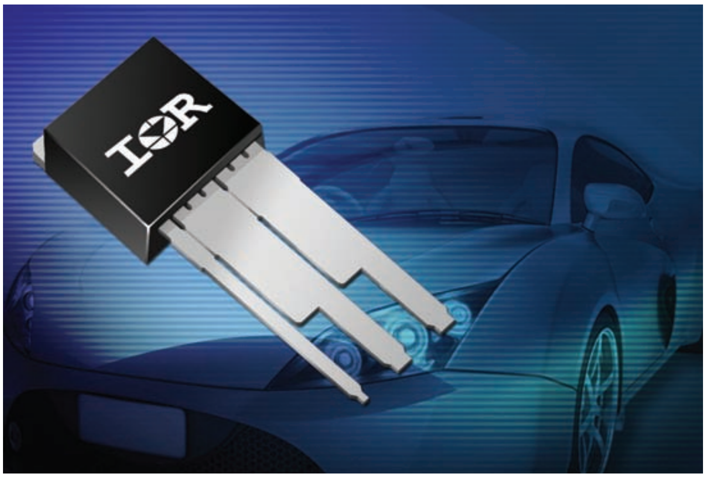
www.vishay.com

60 V PowerTrench MOSFET

Fairchild's new FDMS86500L N-Channel, PowerTrench(r) MOSFET is designed specifically to minimize conduction loss, switch node ringing, and to improve the overall efficiency of DC/DC converters. Through an advanced package and silicon combination, the device provides low on-resistance (2.5mΩ at V_{GS} = 10 V, I_D=25 A) in an industry-standard 5mm x 6mm Power 56 package. Additionally, the FDMS86500L, using shielded-gate MOSFET technology, provides very low switching losses (Q_{gd} 14.6 nC typ.). Other features include enhanced body diode technology engineered for soft recovery, MSL1 robust package design, 100 percent UIL tested and is RoHS compliant.

www.fairchildsemi.com/ds/FD/FDMS86500L.pdf

Automotive MOSFETs in WideLead Package



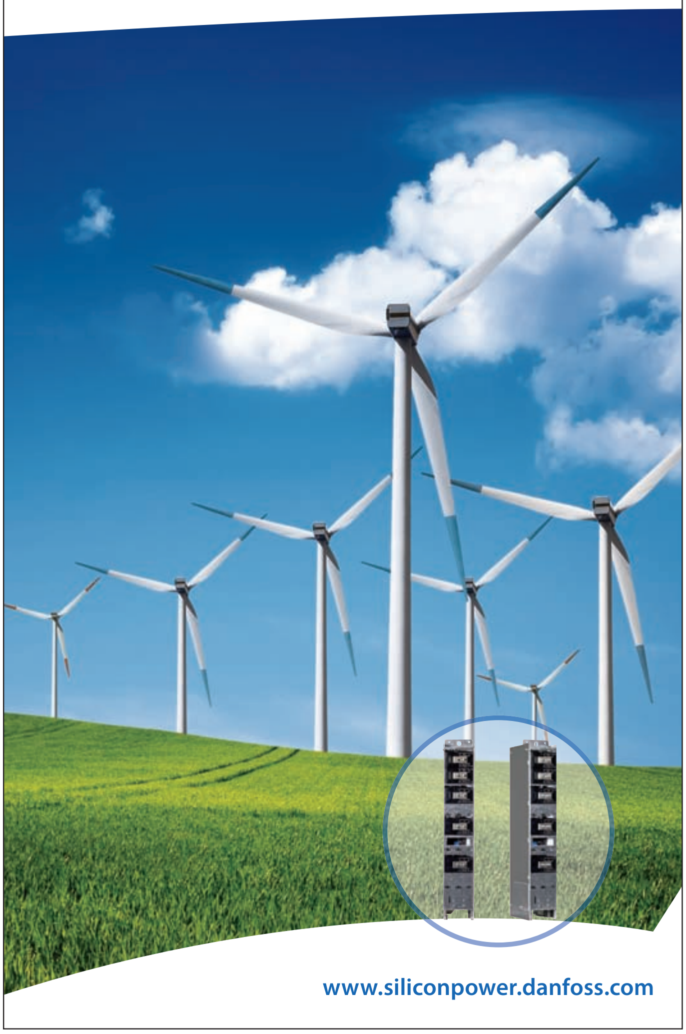
International Rectifier offers a new family of automotive qualified MOSFETs housed in a novel WideLead TO-262 package that reduces lead resistance by 50 % compared to traditional TO-262 packages while offering 30 % higher current. Designed for generic heavy load/high power through-hole applications requiring low on-state resistance, Electric Power Steering and battery switches used in internal combustion engine (ICE) cars, and micro and full hybrid vehicles, the new automotive MOSFETs offer significant performance improvements while being compatible with existing design standards. In standard TO-262 through-hole packages, source and drain leads can add up to 1mΩ of resistance, in addition to the on-state resistance of the MOSFET. The new WideLead TO-262 through-hole package reduces lead resistance to less than half a mΩ, greatly reducing conduction losses and heating in the leads to deliver 30 % more current carrying capability than a traditional TO-262 package for a given operating temperature. Under evaluation, the lead temperature of the WideLead was 30 % cooler than the standard TO-262 at DC currents of 40 A and 39 % cooler at 60 A. Furthermore, other packaging enhancements allow the WideLead to deliver 20 percent lower on-resistance compared with the same MOSFET in a standard TO-262 package. The devices are qualified according to AEC-Q101 standards. Spice models are available on request.

www.irf.com

Gap Pad VO Ultimate with Higher Thermal Conductivity

The Bergquist Company has added Gap Pad VO Ultimate to its Gap Pad VO range of highly conformable thermal interface materials, providing higher thermal conductivity of 1.3 W/m-K for customers needing the most efficient thermal management for optimum system reliability. Gap Pad VO Ultimate is easily compressed, having a Young modulus of 90 kPa, thereby minimising pressure on components and providing low-stress vibration damping. Its high conformability, as with other Gap Pad VO materials, ensures excellent interfacing and wet-out characteristics even when surfaces have high roughness or uneven topography. The rubber coated fibreglass carrier of Gap Pad VO Ultimate eases handling and provides high puncture, shear and tear resistance. Its slight inherent tack minimises shifting during assembly.

www.bergquistcompany.com/pdfs/dataSheets/PDS_GP_Ultimate_10.pdf



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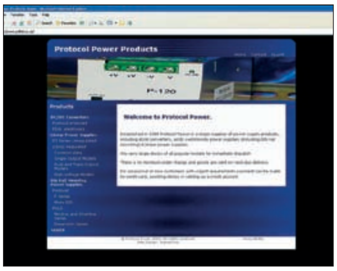

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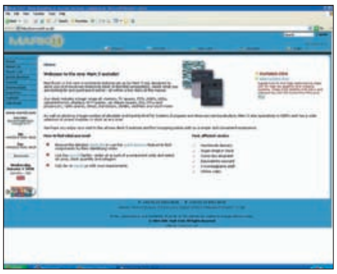

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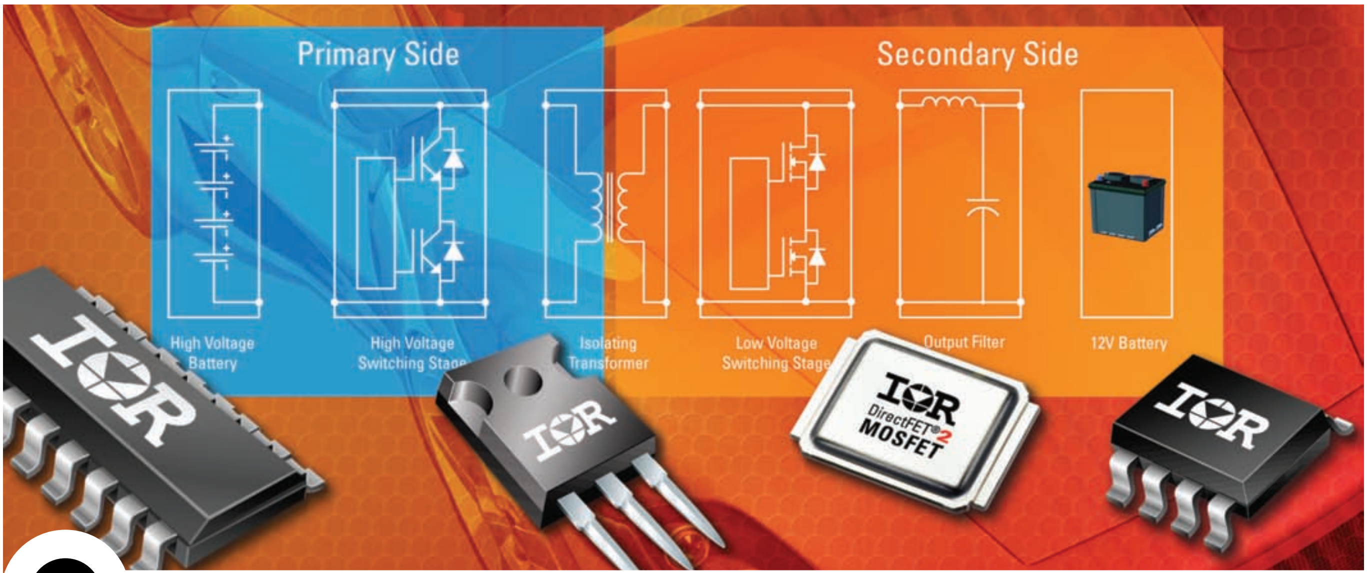

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AUIRF7669L2	100 V	4.4 m	114 A	81 nC	DirectFET L
AUIRF7759L2	75 V	2.3 m	160 A	200 nC	DirectFET L
AUIRF7739L2	40 V	1 m	270 A	220 nC	DirectFET L
AUIRF7736M2	40 V	3.1 m	141 A	83 nC	DirectFET M

600V High Voltage IC for Switching Stage Drivers

Part Number	Description	Output Current	V_{CC} UVLO	Package
AUIRS2191S	High Speed High and Low Side	+3.5 / -3.5 A	8.2 V	SOIC16N
AUIRS21811S	High Speed High and Low Side	+1.9 / -2.3 A	8.2 V	SOIC8

600V Automotive IGBTs for Switching Stage

Part Number	I_C @TC=100°C	$V_{CE(on)}$ typ.	Package
AUIRGP35B60PD	34 A	1.85 V	TO-247
AUIRGP50B60PD1	45 A	2.00 V	TO-247

25V Low Voltage IC for Switching Stage Drivers

Part Number	Description	Output Current	Package
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AUIRS4427S	Dual Channel Low Side	+2.3 / -3.3A	SOIC8
AUIRS4428S	Dual Channel Low Side	+2.3 / -3.3A	SOIC8

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