

POWER ELECTRONICS EUROPE

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POWER PACKAGING

New Thermal Design Options
Drive Power Density

Converter housed in Package

ChiP Technology

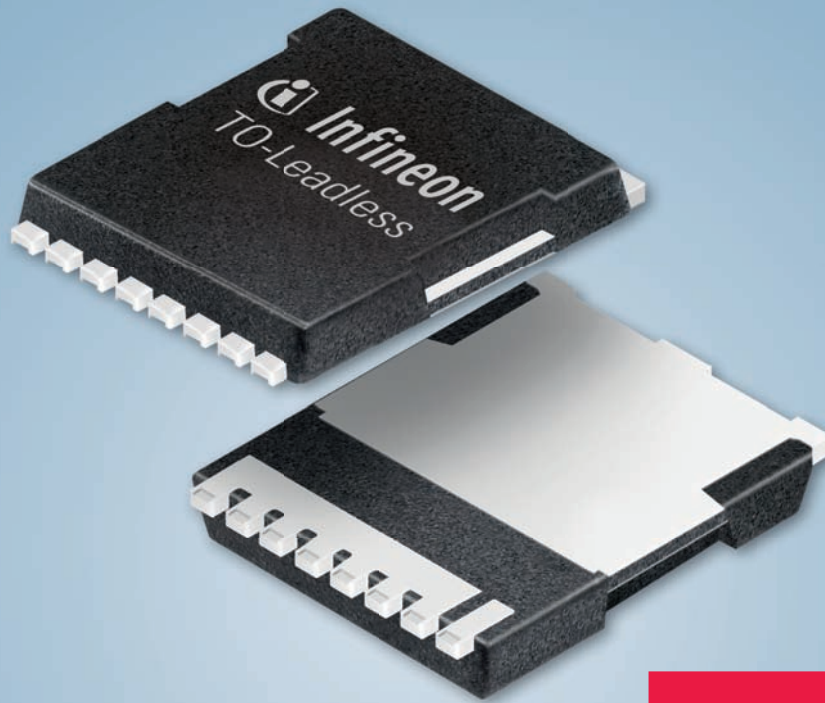
*Increasing power density
while increasing efficiency*



THE EUROPEAN JOURNAL
FOR POWER ELECTRONICS
-----AND TECHNOLOGY-----

Also inside this issue

Opinion | Market News | Industry News
Solar Power | Energy Harvesting
Products | Website Locator



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TO-Leadless

A Package Optimized for High Current Applications



Infineon's new TO-Leadless package is especially designed for high current applications such as forklift, light electric vehicles, e-fuse, PoL (Point of Load) and telecom where highest efficiency and reliability are required. 300A continuous current can now be handled using just one single part. Furthermore, compared to D²PAK 7pin, this significantly smaller package with 60% size reduction offers a very compact design and a substantial reduction of 30% in the footprint.



Key features and benefits

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 - Enables highest efficiency and system cost reduction
- Highest current capability up to 300A
 - Requires less cooling
- Reduced package parasitics
 - Enables improved EMI-performance
 - Lower package losses



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Market News

PEE looks at the latest Market News and company developments

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Industry News

COVER STORY



New Thermal Design Options Drive Power Density

With every generation, electronic products shrink while functionality expands and performance improves. Despite efforts to hold the line on product power dissipation, pressure to increase power density in energy-management subsystems continues unabated. This trend, unfortunately, exacerbates the challenging thermal design task product development teams already face. A new packaging approach for two-sided cooling is Vitor's new ChiP (Converter housed in Package) technology, which presents similar thermal resistances through top and bottom surfaces. Analogous to semiconductor wafer fabrication, individual ChiP-based components are arrayed to utilize 100 % of the PCB material, with no area lost to lead/pin attach. The array is then sawn into individual 'chip-scale' components with no superfluous, non-value-added packaging, thus minimizing space used in customer designs. ChiP packaging supports power-management functions such as AC/DC conversion with PFC (power-factor correction); isolated bus conversion; DC/DC conversion; buck, boost, and buck-boost regulation; and PoL current multiplication. Full story on page 18.

Cover image supplied by Vitor Corporation

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Solar Inverter Performance Improvement Utilizing 650 V HighSpeed 3 IGBT Power Modules

For applications which require an output filter or have a boost/buck choke, higher switching frequencies can lead to advantages on system level. One application where both can be found is a solar inverter. At the state-of-the-art efficiency and power density, high cost pressure can be observed for solar inverters. In this article, the difference between the 650 V IGBT3, 650 V IGBT4 and the 650 V HighSpeed 3 (HS3) IGBT from Infineon Technologies used in power modules will be described. It will be shown that due to the device design, the 650 V HS3 IGBT provides a superior performance and can be used as a highly efficient switch.

Jens De Bock and Christian R. Müller, Infineon Technologies AG, Warstein, Germany

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Power Module Design for an Efficient Three-Level Utility Grid Solar Inverter

The race to achieve highest efficiency had engineers turning to innovative topologies and new components such as SiC to take the lead. In parallel, after years of dormancy, old but very innovative ideas such as the mixed-voltage NPC topology have been rediscovered and put to good use in many solar inverter applications. Surprisingly, all these efforts have focused on the power range up to 100kW, while standard two-level topologies with low switching frequencies continue to dominate in the range beyond 100 kW. The new power module design transcends the limitations associated with >100 kW power inverters to accommodate high switching frequencies and innovative topologies based on standard Si components. **Michael Frisch and Temesi Ernő, Vincotech Germany and Hungary**

PAGE 28

The Power and Potential of Piezoelectric Energy Harvesting

The process of piezoelectric energy harvesting – that of converting mechanical energy into electrical – has rapidly gained momentum in recent years for a number of reasons, primarily due to its energy efficiency and environmental benefits. There has been considerable development in applications utilising piezoelectric innovations, alongside advances in ultra low power electronics, meaning energy harvesting is no longer viewed as being a potentially unreliable source of energy transfer, capable of only low power output. While alternative energy harvesting technologies are available, such as thermoelectric or electromagnetic energy, some have a reputation for unreliability and are not always capable of providing the consistent source of energy needed.

Fred Pimparel, Technical Manager, Morgan Technical Ceramics, Stourport, UK

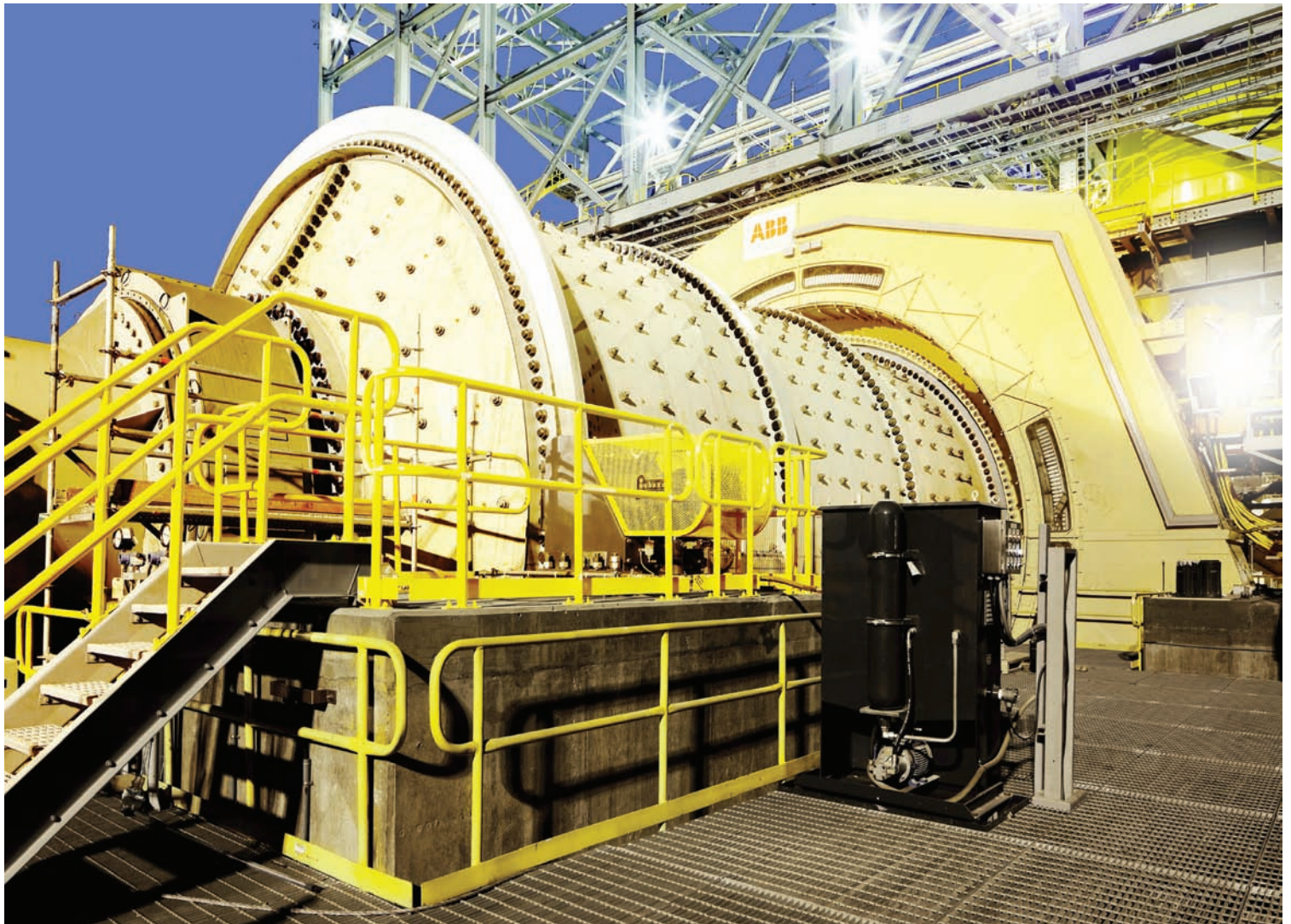
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Products

Product Update

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Website Product Locator



Thyristors enabling energy savings of 30%?

Definitely.



ABB Semiconductors' Phase Control Thyristor (PCT) has been a key component in the high power electronics industry since its introduction almost 50 years ago. Common PCT applications range from kilowatt DC-drives to gigawatt converters for high-voltage direct current transmission (HVDC). The use of PCT powered converters enables significant energy savings. ABB's thyristor portfolio includes both PCT and bi-directionally controlled thyristor (BCT) press-pack devices with ratings of 1,600 to 8,500 volts and 350 to 6,100 amperes.

For more information please visit our website: www.abb.com/semiconductors



Next Steps in Power

frequency and high temperature operation. Capturing these two added-values remains an issue as no existing set of technologies can fully answer that request now. The path to success for SiC large implementation will necessarily go through new packaging solutions. Numerous bottlenecks need to be unlocked: chip bonding, metallic contact technique, gel filling, encapsulant, EMI, and so on.

The power electronics downturn in 2012 was with -20 % quite severe. The market suffered from the global economic downturn combined with external factors. Now, at the end of 2013, the market conditions have recovered. However, the SiC device market kept on growing with a +38 % increase year to year. SiC technology is now commonly accepted as a reliable and pertinent alternative to the Silicon world and most power module and power inverter manufacturers have already included it in their roadmap.

There are now more than 30 companies worldwide which have established a dedicated SiC device manufacturing capability with related commercial and promotion activities. Virtually, all other existing Silicon-based power device makers are also more or less active in the SiC market but at different stages. Last year has seen the ramp-up of some companies, such as Rohm, MicroSemi, GeneSiC or STMicro, facing CREE and Infineon, prefiguring a new market shaping in the coming years. Raytheon, Ascatron, IBS, RFID and Fraunhofer IISB have decided to launch SiC foundry services or contract manufacturing services. This business model establishment addresses the demand of future SiC fabless and design houses that may look for specific manufacturing partners. It will also probably act as a possible second source for IDMs in cases of production overshoot.

In Asia, Panasonic and Toshiba are now clearly identified as contenders, along with Mitsubishi Electric, now developing SiC power modules. Fuji Electric's new SiC line is now running within the Japanese national program. No Chinese device maker has emerged yet, however, according to the huge investment plan in R&D, Yole Développement's analyst suspects new IDMs will soon enter the business. In the US, Global Power Device and USCi have now strongly affirmed their intentions to take market share.

The SiC industry is now reshaping, starting from a discrete device business mutating into a power module business. Originally, this was initiated by Powerex, MicroSemi, Vincotech or GeneSiC with hybrid Si/SiC products, then other players such as Mitsubishi, GPE and more recently Rohm or Cree have reached the market with full-SiC modules. This trend will become dominant in the coming years as integrators require power modules in most of their mid and high power systems. Yole Développement forecasts that SiC-based power module demand could exceed \$100 million by 2015 and top \$800 million in 2020 depending on whether or not the auto industry will adopt SiC. SiC equals high

The next step is GaN. The use of wide bandgap materials such as SiC or GaN strongly increases the performances of power transistors in terms of breakdown voltage, power density, maximum operating junction temperature and switching speed. Among these technologies, GaN on Silicon high electron-mobility transistor (HEMT) structure are very attractive in term of performances versus cost. In the case of low voltage GaN transistors, the switching speed is in the range of few nanoseconds. Therefore, transistors based on Gallium Nitride can operate at switching frequency more than ten times higher compared to Silicon transistors. However, reverse conduction is still a problem, and no GaN discrete diode is commercially available to be used in antiparallel in order to keep a high figure of merit for the assembly. Under these conditions, switching losses as well as on state losses must be characterized and estimated. Solutions and concepts for high-frequency power electronics of the future shall be developed in the collaborative project "GaN-resonant – Efficient, highly compact high frequency power electronics with GaN transistors", which is sponsored by the German Federal Ministry for Education and Research (BMBF). "GaN-resonant" will be funded with around 1.2 million euro over the next three years by the German Federal Ministry for Education and Research (BMBF) in the context of its funding announcement "Power Electronics for Increasing Energy Efficiency". The project goal is to develop a resonant DC/DC converter with GaN transistors, which is to operate with switching frequencies well above 1 MHz and a nominal power of 3 kW. The simultaneous occurrence of extremely high switching frequencies and high transmitted power requires the use of special, innovative inductive components. The development of such devices makes up a significant part of the collaborative project. Due to high power losses, the solutions available today limit the technically practical switching frequency. Thus, the existing solutions are not suitable for future applications, which demand both a substantially higher power density and a higher efficiency at the same time. This accomplishment can only be realized by innovations in the area of inductive components (core materials and geometries, winding structures and cooling concepts).

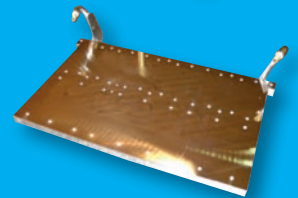
Thus the power electronics industry and also PEE faces new challenges in the years to come, and Silicon technology probably will catch up as can be seen in our feature articles. Enjoy reading.

Achim Scharf
PEE Editor

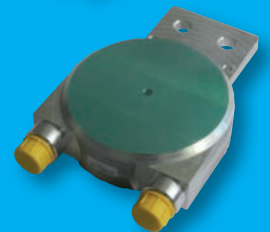
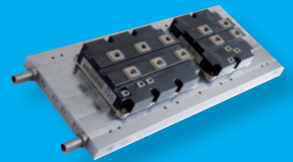
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Power Supply Market to Grow After Disappointing 2012

After declining in 2012, the global market for merchant power supplies is forecast to grow by 2.4 % in 2013. This rebound is being driven by rising demand in the tablet PC, smartphone, LED lighting and server markets, according to market researcher IHS.

Tablet PCs and smartphones

both use external power adapters, which represent the fastest growing segment of the merchant power supply market. The tablet PC market is still dominated by Apple Inc., although its market share has eroded as competing manufacturers have released

more products. The market for power supplies for tablet PCs is calculated to grow by \$250 million from 2012 to 2014, with no signs of demand slowing.

The smartphone market continues to expand strongly as consumers purchase the latest models from manufacturers such

as Apple and Samsung. Further demand is coming from the developing markets where 3G—and in some cases, 4G networks—are being rolled out. Such developments will spur the market for power supplies for smartphones to expand by 40 % from 2012 to 2014, although growth projections for the longer term are much lower.

The markets for power supplies used in LED lighting and server and storage applications also are projected to be key growth drivers in the coming years. The adoption of LED lighting is forecast to drive the market for power supplies used in lighting applications to almost triple in five years.

The rise of cloud computing is forcing companies to invest heavily in information technology (IT) equipment, specifically increased server and storage capabilities in datacenters. This equipment has complex and demanding power requirements, creating a valuable opportunity for power supply manufacturers. This will help grow the market for power supplies in server and storage applications by \$500 million in five years.

However, these four applications account for only about 25 % of the total power supply market. Large, traditional markets such as industrial and telecommunications continue to suffer from a lack of investment and low business confidence which reduces demand for power supplies needed for new equipment and machinery. It is forecast that these two markets in particular will suffer from weak end-equipment demand for the foreseeable future with revenue not returning to the 2011 estimated value for a projected four years. To ensure growth and recovery in the coming years, suppliers must identify and target lucrative markets that will provide them with future opportunities as demand remains low in many of the traditional areas upon which suppliers have depended.

SUBSTITUTE FOR TRANSFORMERS – 5 LETTERS



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Power Supply WebDesigner

Fairchild Semiconductor has enhanced its Power Supply WebDesigner (PSW) – an online design and simulation tool that provides complete designs in under a minute – to include power train discrete (MOSFET/IGBT/Rectifier) device power loss and efficiency analysis tools.

Intended for 100 W to 3 kW designs as a function of input and output conditions, these new modules provide designers power factor correction (PFC), phase-shifted full-bridge plus secondary side synchronous rectification (PSFB+SR) power train discrete device analysis, and the matrix of device combinations associated with these topologies. From user-specified electrical and mechanical specifications, the new modules provide a combination of power discrete semiconductors, transformer and inductor design values, as well as a bill of material (BOM). It also provides a dashboard view of the converter's system and device power loss, device junction temperature, and further component fine-tuning over the operating conditions. As with other PSW modules, designers using the tools can accept default recommended values, or spend time optimizing the important details to

their unique design needs. They can get quick, accurate estimates on design performance, and refine design choices as they go. The tools also allow them to spend the time to perform detailed simulation analysis and learn the insights of how their design and its hardware prototype will work with higher degree of confidence.

These new modules save designer's time when evaluating various combinations. Rather than spending the typical one-week-per-combination bench testing time, PSW can simulate each combination quickly and accurately – typically ~2 % difference over line and load conditions between tool and hardware measurement results. When a design is complete, PSW creates a BOM which can be sent to their procurement department or instantly procure the components online, saving time on documentation or sourcing parts elsewhere. Additionally, they can save their design for future reference or pass the design on to other team members.

[www.fairchildsemi.com/
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Research Project on 3 kW Resonant GaN Converter

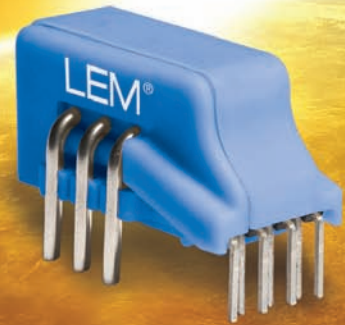
Highly modern power transistors based on gallium nitride (GaN) enable power electronic switches to operate at much higher switching frequencies compared to those based on silicon (Si). An increased power density per volume and per weight, reduced costs, less material use and, in the case of a mobile system, increased system efficiency are among the advantages. Solutions and concepts for high-frequency power electronics of the future shall be developed in the collaborative project "GaN-resonant – Efficient, highly compact high frequency power electronics with GaN transistors", which is sponsored by the German Federal Ministry for Education and Research (BMBF). "GaN-resonant" will be funded with around 1.2 million euro over the next three years by the German Federal Ministry for Education and Research (BMBF) in the context of its funding announcement "Power Electronics for Increasing Energy Efficiency".

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(www.ise.fraunhofer.de), the SUMIDA Components & Modules GmbH (<http://www.sumida-components.com>) and the Liebherr Elektronik GmbH (www.liebherr.com) are involved in the collaborative project "GaN-resonant". The project goal is to develop a resonant DC/DC converter with GaN transistors, which is to operate with switching frequencies well above 1 MHz and a nominal power of 3 kW. The simultaneous occurrence of extremely high switching frequencies and high transmitted power requires the use of special, innovative inductive components. The development of such devices makes up a significant part of the collaborative project. Due to high power losses, the solutions available today limit the technically practical switching frequency. Thus, the existing solutions are not suitable for future applications, which demand both a substantially higher power density and a higher efficiency at the same time. This accomplishment can only be realized by innovations in the area of inductive components (core materials and geometries, winding structures and cooling concepts).

In the area of control, synchronous to the applied switching frequency, new problems arising due to the higher frequencies will be addressed in the collaborative project. Such issues include, for example, broadband data acquisition and signal processing. In order to exploit the advantages of a high switching frequency, the computing power used to control the DC/DC converter must be increased by a similar amount as the switching frequency or parts of the control must be carried out with analog devices.

The field of aeronautical electronics is one possible application area for the resonant voltage converter under development. In this field, compactness and low weight are of utmost importance. The amount of harmful emissions, which are of particular concern especially at high elevations, can be reduced by decreasing the system's weight. With its higher power density, the electronics are also well-suited for other mobile applications. Low space requirements, low cooling demand and low weight are decisive criteria for the mobility sector. Another use is found in the power supply for server farms or communication electronics in general. Today the worldwide energy consumption for the communication infrastructure has reached immense proportions. In addition to saving material with this technology, the power loss can also be reduced. This leads not only to increased efficiency but also to lower cooling demands.

www.ise.fraunhofer.de

New Catalog on Adhesives for the Electronic Industry

New, easy to read, 32 page catalog offers performance and processing data on Master Bond's line of epoxy, silicone, polyurethane, silicate based and light curing compounds. These products provide solutions to PCB assembly, die-attach, conformal coating, surface mount, lid sealing, chip and wire bonding applications. Convenient, efficient and reliable packaging options are also reviewed.

Products are available as liquids, pastes, films and preforms. Electrically insulative, thermally conductive and electrically conductive grades are listed. Pertinent mechanical, electrical, thermal and chemical resistant properties are shown. Additionally, information is provided on viscosity, cure speed, working life, color, etc. This catalog is available for immediate download in PDF format or in print.

www.masterbond.com/catalog/adhesives-electronic-applications

Extended GaN Distribution

Global electronic components distributor Digi-Key announced new inventory of Gallium Nitride (GaN) power management products from Efficient Power Conversion (EPC).

EPC was the first to introduce enhancement-mode Gallium-Nitride-on-Silicon (eGaN®) FETs as power MOSFET replacements in applications such as point-of-load converters, Power over Ethernet (PoE), server and computer DC/DC converters, LED lighting, cell phones, RF transmission, solar micro-inverters, and class-D audio amplifiers. "Gallium Nitride shows tremendous promise within the semiconductor space, as the power density benefits over Silicon provide a unique opportunity for designers," said Digi-Key's VP Mark Zack. "Digi-Key makes it easy for engineers to develop state-of-the-art power conversion systems with our enhancement-

mode GaN transistors as replacements for their less-efficient Silicon transistors. Their ability to support our customers from prototype to production has been invaluable as the adoption rate of our technology continues to grow," said Alex Lidow, EPC's CEO. New eGaN products are being released frequently, from the EPC2016 and EPC2018 power transistors, to the EPC9017 development board. In addition, EPC has released the EPC800x family of high-speed products that are blurring the line between Power and RF Transistors. For designers interested in evaluating the new EPC800x family of devices, EPC has released the EPC9027 development board, which features the EPC8007 device and the LM5113 gate driver IC in a half bridge configuration.

www.epc-co.com, www.digikey.com

Smart Meter Reference Platform

Designers of smart meters can now reduce time to market, raise the bar for higher accuracy, and secure their designs with Capistrano, a smart grid reference platform from Maxim Integrated Products.

Powered by the company's Zeus metering SoC, Capistrano protects designs with advanced cryptography, physical attack detection, and life-cycle security schemes. Protecting more than just the smart meter, the security technology is capable of securing



any distributed node in the smart grid. Additionally, the high integration in Capistrano makes it versatile - it simplifies smart grid designs by integrating four complex processors: an applications processor, metering microcontroller, metering front-end/DSP, and

security coprocessor. It also offers highest accuracy - 0.1% over a wide current range of 8000:1. The combination of advanced measurement, powerful security tools, and efficient processing allows Capistrano to support evolving application design requirements. "More than 100 million smart electricity meters are expected to be shipped in 2014," said Jacob Rodrigues Pereira, IHS analyst for smart utilities infrastructure. "For designers, security, improving smart meter time to market, and adapting to changing policy requirements will all be critical." Kris Ardis, Maxim' Executive Director of Energy Solutions added: "Capistrano provides an excellent toolbox for building tomorrow's smart grid."

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Smart Measurement Solutions

Synchronous Rectification for Industrial Applications

System designers can now achieve more efficiency across a wide industrial voltage range with the MAX17503 synchronously-rectified DC/DC step-down converter from Maxim Integrated Products. By integrating two MOSFET switches and eliminating an external Schottky diode, the MAX17503 operates from 4.5 V to 60 V, delivers up to 2.5 A output current and is specifically designed for industrial control and automation applications.

The device features a peak-current-mode control architecture with a MODE feature that can be used to operate the device in pulse-width modulation (PWM), pulse-frequency modulation (PFM), or discontinuous-conduction mode (DCM) control schemes. PWM operation provides constant frequency operation at all loads, and is useful in applications sensitive to switching frequency.

PFM operation disables negative inductor current and additionally skips pulses at light loads for high efficiency. DCM features constant frequency operation down to lighter loads than PFM mode, by not skipping pulses but only disabling negative inductor current at light loads. DCM operation offers efficiency performance that lies between PWM and PFM modes. The low-resistance, on-chip MOSFETs ensure high efficiency at full load and simplify the layout.

A programmable soft-start feature allows users to reduce input inrush current. The device also incorporates an output enable/undervoltage lockout pin (EN/UVLO) that allows the user to turn on the part at the desired input-voltage level. An open-drain RESET pin provides a delayed power-good signal to the system upon achieving successful regulation of the output voltage.

The switching frequency can be programmed from 200 kHz to 2.2 MHz by using a resistor connected from the RT pin to SGND. The internal oscillator of the device can be synchronized to an external clock signal on the SYNC pin. The external synchronization clock frequency must be between $1.1 \times f_{sw}$ and

$1.4 \times f_{sw}$, where f_{sw} is the frequency programmed by the RT resistor. The minimum external clock pulse-width high should be greater than 50ns.

Protection features

The device is provided with a robust overcurrent protection scheme that protects the device under overload and output short-circuit conditions. A cycle-by-cycle peak current limit turns off the high-side MOSFET whenever the high-side switch current exceeds an internal limit of 3.7A (typ). A runaway current limit on the high-side switch current at 4.3A (typ) protects the device under high input voltage, short-circuit conditions when there is insufficient output voltage available to restore the inductor current that was built up during the ON period of the step-down converter. One occurrence of the runaway current limit triggers a hiccup mode. In addition, if due to a fault condition, feedback voltage drops to 0.58 V (typ) any time after soft-start is complete, and hiccup mode is triggered. In hiccup mode, the converter is protected by suspending switching for a hiccup timeout period of 32,768 clock cycles. Once the hiccup timeout period expires, soft-start is attempted again. When soft-start is attempted under overload condition, if feedback voltage does not exceed 0.58 V, the device switches at half the programmed switching frequency. Hiccup mode of operation ensures low power dissipation under output short-circuit conditions.

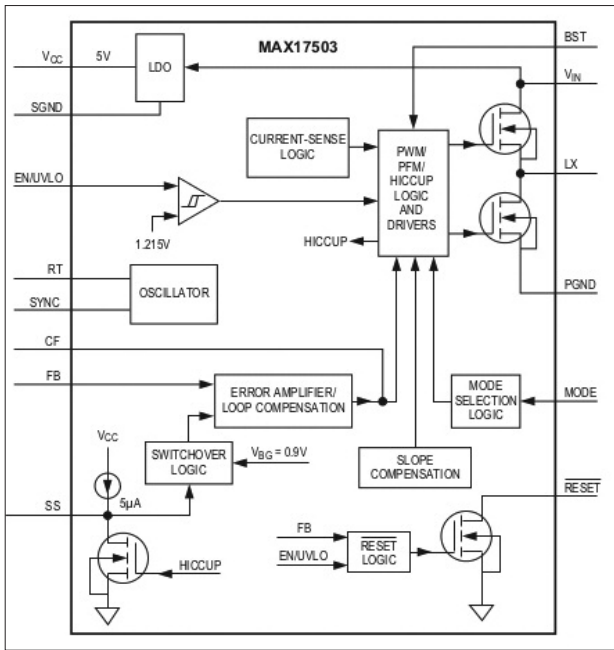
Thermal-shutdown protection limits total power dissipation in the device. When the junction temperature exceeds +165°C, an on-chip thermal sensor shuts down, allowing the device to cool. The thermal sensor turns the device on again after the junction temperature cools by 10 K. Soft-start resets during thermal shutdown.

PCB layout guidelines

All connections carrying pulsed currents must be very short and as wide as

Industry's most efficient
high-voltage DC-DC converter
MAX17503

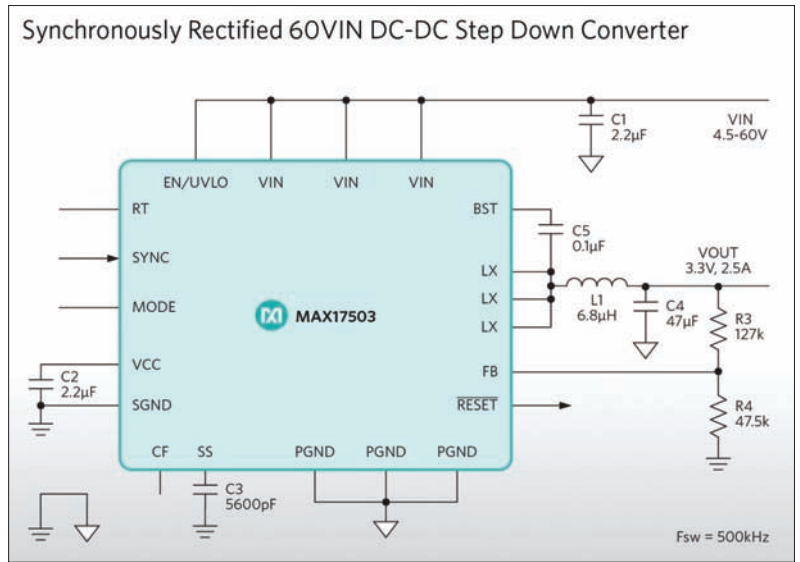
**Synchronous
rectified DC/DC
converter
MAX17503 for
industrial
applications**



ABOVE: MAX17503 block diagram

possible. The inductance of these connections must be kept to an absolute minimum due to the high di/dt of the currents. Since inductance of a current carrying loop is proportional to the area enclosed by the loop, if the loop area is made very small, inductance is reduced. Additionally, small-current loop areas reduce radiated EMI.

A ceramic input filter capacitor should be placed close to the VIN pins of the



ABOVE: Typical schematic for a 60 V input application

IC. This eliminates as much trace inductance effects as possible and gives the IC a cleaner voltage supply. A bypass capacitor for the VCC pin also should be placed close to the pin to reduce effects of trace impedance.

PCB layout also affects the thermal performance of the design. A number of thermal vias that connect to a large ground plane should be provided under the exposed pad for efficient heat dissipation. For a sample layout that ensures first pass success, the MAX17503 evaluation kit layout is available.

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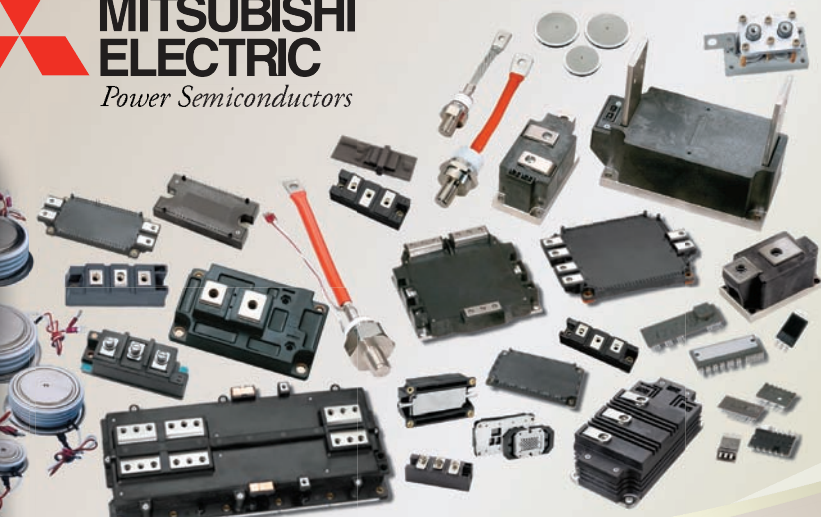
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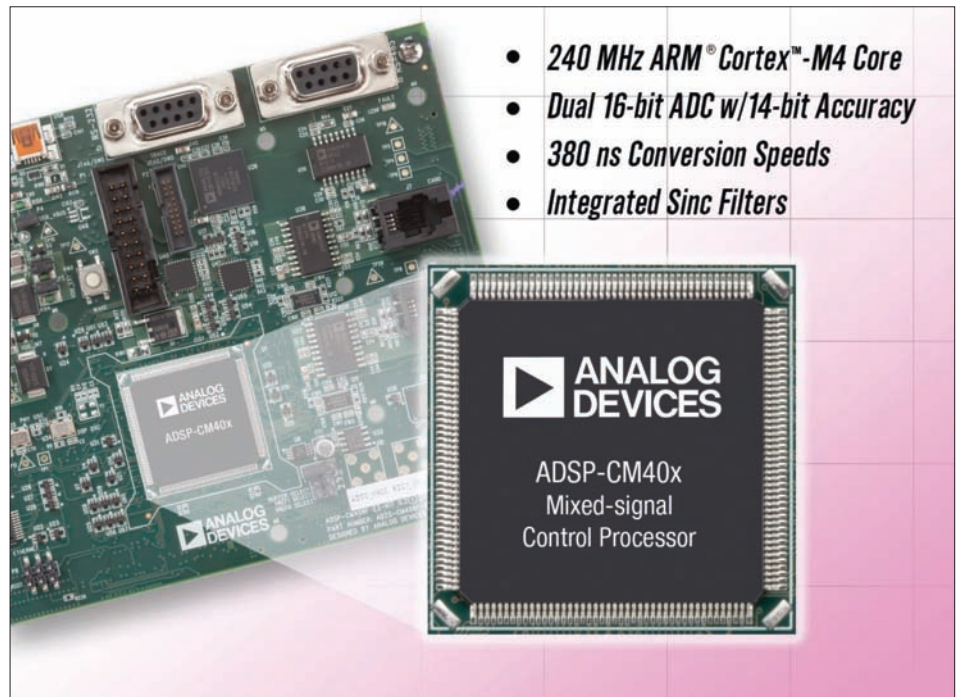


New Generation of Control Processors for Drives and PV Inverters

Equipment manufacturers require highly accurate, closed-loop control in servo, motor-drive, solar photovoltaic (PV) inverter and other embedded industrial applications to improve the energy efficiency and performance of their products. A new control DSP family along with reference designs from Analog Devices eases the design of motor and PV inverters.

Forty percent of the world's electric power is consumed by electric motors, and demand for higher levels of factory automation is driving the need for greater industrial-motor power efficiency and performance. In addition, solar PV has become the largest source of new generation capacity added to the global electricity grid - with a cumulative installation base of 100 GW - and is set to become the fastest growing source of renewable energy generation over the next decade. Increased measurement accuracy is driven by ever more stringent grid compliance requirements. This coupled with faster power control loops, fueled by the emergence of GaN and SiC power switching technologies, are combining to enable significant performance and cost improvements in the next generation of solar PV inverter topologies.

The ADSP-CM40x series is the first of a new generation of mixed-signal control processors for precision control applications. In addition to its 380-ns A/D conversion speeds, the ADSP-CM40x provides a number of other features such as a full sinc filter implementation to interface directly to isolated sigma-delta modulators (AD7400A/AD7401A) which are used in shunt-based current sensing system architectures. The availability of an on-chip sinc filter eliminates the



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- **380 ns Conversion Speeds**
- **Integrated Sinc Filters**

New DSP ADSP-CM40x eases the design of motor drives and PV inverters

cost and engineering resources required to implement that function in an FPGA. Combined with iCoupler® isolated products (gate drivers, sigma-delta converters, digital isolators and transceivers), simultaneous sampling A/D converters, resolver-to-digital converters and power-factor-correction controllers, solutions across the entire motor control signal-chain are available.

Through the use of MathWorks' ARM® Cortex™-M optimized Embedded Coder® and tool suites, system development is further enhanced by bringing designs from simulation to productized code implementation in an embedded platform.

Motor efficiency begins with the processor

The new ADSP-CM40x ARM Cortex-M4 family are bringing price/performance balance to a level where implementations of more sophisticated motor control algorithms such as FOC (field orientated control) are starting to gain traction in higher volume solutions. Specifically in terms of processor capability - built-in digital filter functions, high performance floating point capability, and extended mathematical capability all allow more complex and combined algorithms to create a better controller and control scheme, pushing the efficiency of motor drives.

Within the industry there is no doubt that the

enhancement of multiple observer models running real-time model based estimators will help to enhance performance of the drive, system efficiency and topology, and the deployment method of the design. Graphical systems like MATLAB/Simulink are today capable of easing the design flow and enhancing the development of new algorithms. These tools, together with the executing processors, enable a more complex deployment to be achieved. Processor-level enhancements related to core speed, A/D conversion resolution, and memory integration will afford designers the capability and precision to achieve greater quality and higher performance objectives while accelerating time to market.

With the recent introduction of ADI's ADSP-CM40x series of mixed signal embedded controllers, significant processing performance gains have been achieved in parallel with price point reductions to bring DSP performance to motor control applications. Motor system designers will leverage this performance profile to achieve greater system functionality and precision through the use of more advanced algorithms, which can be applied to accurately determine rotor shaft position and speed so as to eliminate the need for position/speed sensors in the system.

Along with the introduction of the new





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CM40x EZ-KIT

also

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AD2S1210
ADN4662
ADM6320
ADP3634
ADP121
ADP7102
AD8515
AD8646
AD8662

ADSP-CM40x Control Board

Evaluation board for drive inverters comprising 1200-V IGBT modules in the power stage

processor a reference design covering a high-voltage board comprising 600-V MOSFETs or 1200-V IGBT modules is available.

Isolation in PV inverters

A solar photovoltaic (PV) inverter converts electrical power from a solar panel and deploys it to the utility grid efficiently. DC power from the solar panels, which act like a DC current source, is converted to AC and fed onto the utility's grid in the correct phase relationship - with up to 98 % efficiency. The PV inverter conversion process can occur in one or more stages.

Stage 1 is typically a DC/DC conversion from the low voltage-high current solar cells that constitute

the panels, to the high voltage/low current levels compatible with the AC voltage of the grid. This stage may not be necessary, depending on the topology and if enough solar cells are connected in series, on the DC side, to ensure a stable high voltage under all load conditions.

In Stage 2, DC is converted to AC, typically using an H-bridge topology. PV inverter designs may use variations of the H-bridge, such as neutral-point clamping (NPC), to improve efficiency and reduce reactive power in the system.

Early solar PV inverters were simply modules that dumped power onto the utility grid. Newer designs emphasize safety, intelligent grid integration, and cost reduction. Designers are

looking to new technology, not used in existing solar inverter modules, to improve performance and reduce cost.

A key element is computer-based instrumentation and control, but an isolation barrier must protect measurement and computation circuitry from the power-handling circuitry—as well as from transient signals due to switching. Isolation technology such as iCoupler® can reduce cost, increase smart grid integration, and improve safety of solar PV inverters.

Transformers couple data between two separately powered circuits while avoiding any galvanic connection between them. The transformers are fabricated directly on chip using wafer-level processing. A high breakdown polyimide layer underneath the gold layer insulates the upper coil from the lower one. Input logic transitions, encoded using 1 ns pulses, are routed to the transformer's primary side. The pulses, coupled from one transformer coil to the other, are detected by the circuitry on the secondary side of the transformer.

In example, a pair of solar PV inverters are tied to a power bus that is connected to the grid, are independently measured and switched. Each solar panel is connected to its DC/DC step-up circuit, then to a DC/AC inverter.

The ADSP-CM40x controls the process, the AD7401A isolated ADC measures AC output current. The AD7401A iCoupler-isolated Σ-Δ-modulator ADC, continuously samples the voltage across the current shunt. Its output is a 1-bit data stream, which is isolated and fed directly into a DSP. The density of ones in the output stream represents the input amplitude, which can be reconstructed with a digital filter implemented in the DSP. To minimize power loss (and thermal errors due to self-heating) in the shunt, its resistance needs to be kept to as low a value as possible, at typically 1 mΩ. The very high resolution of Σ-Δ converters allows current shunt losses to be kept on par with traditional magnetic transducer solutions while achieving better accuracy and lower offset.

Isolation is required within solar PV inverter systems, primarily because of the high voltages appearing on an AC grid. The AC voltage, even in single-phase systems, can peak at 380 V. The AD7401A's isolation can handle bipolar voltage up to 561 V, which makes it suitable for this application. A key advantage to using the AD7401A is that its small package allows the ADC to be located very close to the actual AC current shunt, whereas the DSP may be some distance away - or even on another board in the system. This improves the accuracy and reliability of data in the measurement and control system. The ADC output data is sent to the DSP serially via a single-bit stream at a 16-MHz clock rate, supplied by the DSP.

Along with the introduction of the new processor a reference design covering a board comprising isolated drivers for GaN power switches is available.

Solar PV Inverter

Gate Drivers
- ADuM4223
- ADP3654

Sigma-Delta ADC
- AD7401A

RF Transceiver
- ADF7023

Amplifiers
- AD8656
- ADA4851
- AD8512
- AD8639

Isolated DC-DC
- ADuM6202

ADSP-CM40x EZ-KIT

ADSP-CM40x EZ-KIT plus PV Inverter

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- High Speed Isolated Driving of GaN Power Switches
- Hardware Harmonics Analysis for Grid feed-in quality

CM40x EZ-KIT

Voltage Regulators
- AD7104
- ADuM3472

REF/Temp Sense
- AD391
- ADA4381
- TMP36
- TMP05

Other
- ADP1864
- ADP1715
- ADM3202
- ADM3252E
- ADM3053

Evaluation board for PV inverters comprising isolated GaN drivers for the power stage

www.analog.com/cic

DC/DC Power Converter Solutions

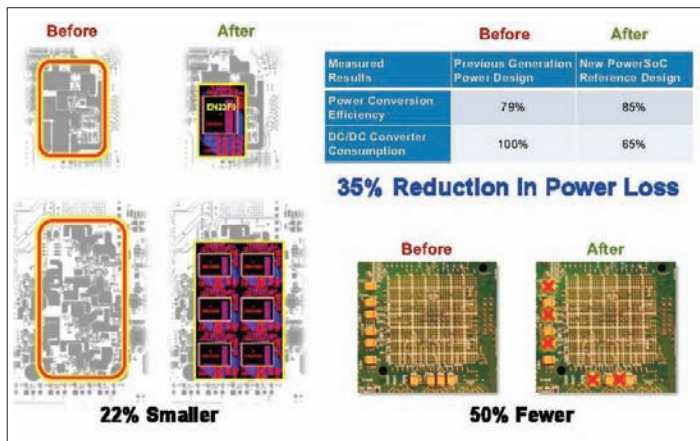
Improve System Power Efficiency

Altera announced four new reference designs that leverage the power technology obtained through its acquisition of Enpirion. The reference designs provide FPGA users and board developers turnkey power solutions that increase power efficiency by up to 35 %, reduce board area by up to 50 %, and reduce overall bill-of-material (BOM) bulk capacitance costs by up to 50 % compared to conventional solutions.

The power-optimized reference designs take advantage of Enpirion PowerSoC (power system-on-chip) DC/DC converters, which include integrated controllers, high-frequency power FETs and inductors in a very small package. Since up to five rails have to be powered in Field Programmable Arrays (FPGAs), proper sequencing of these rails is important. Altera's goal therefore is to offer optimized power supply for FPGA's featuring 90 % efficiency compared to 25 % with Low Dropout Regulators (LDOs). In May 2013 Altera has signed a merger agreement to acquire Enpirion in order to complement its FPGAs with integrated power conversion products known as PowerSoCs.

For high switching frequencies

The vertical VDMOS and trench MOS are more suitable for low-frequency, high-current applications, while the lateral LDMOS is more suitable for high-frequency, low-current applications. A lateral-trench MOSFET has the potential to apply at intermediate frequencies and currents. The gate-drain charge and on-resistance product ($Q_{gd} \times R_{ds(on)}$) referred to as the Figure-Of-Merit (FOM) characterizes the device performance. In general the trench MOSFET exhibits the highest FOM due to high gate charge, while the LDMOS has the lowest value. That's why Enpirion is focusing on lateral technology delivering low gate charge and thus a low figure-of-merit of 20. This figure provides a 40 % improvement over alternative LDMOS, 73 % versus VDMOS, and 33 % better than high performance GaN, according to Enpirion. The chosen 0.18 micron



Reduction in system size, bulk capacitors and power by using power SOCs for powering FPGAs compared to conventional solutions

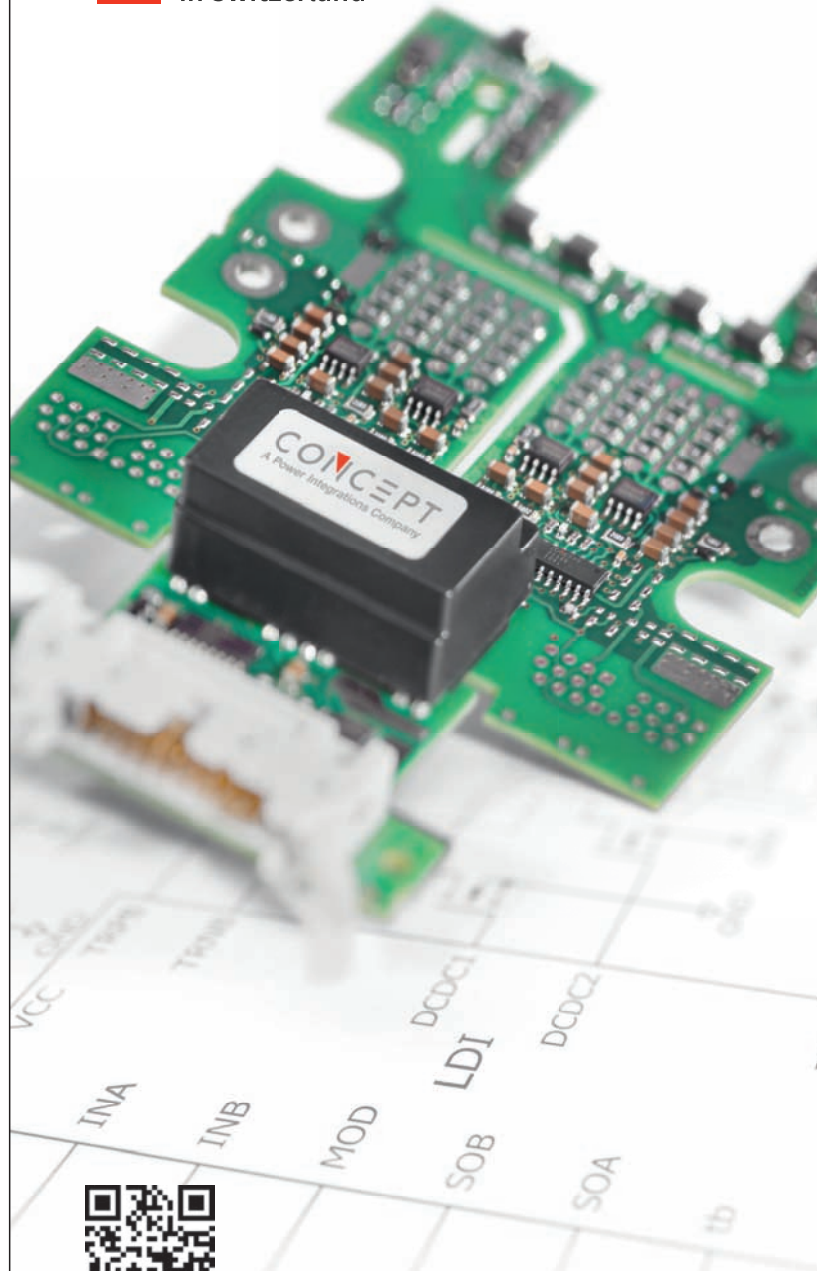
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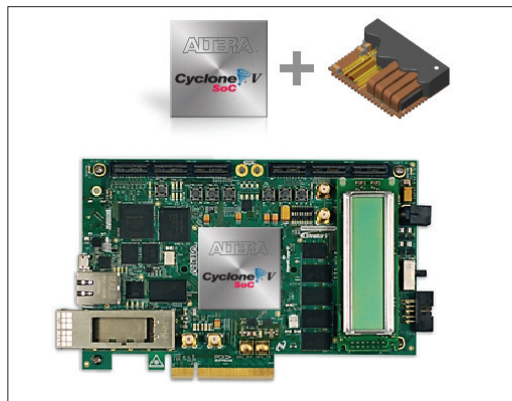
CONCEPT
A Power Integrations Company

LDMOS (CMOS) process normally uses 20 masking steps, two additional steps are required for the integrated power MOSFETs. That is a different approach building up the structure in a mainstream fab compared to discrete power MOSFETs requiring up to eight masking steps.

The development of a new magnetic alloy enables the miniaturization of passive magnetic components and their assimilation with integrated circuits at wafer level. So-called wafer level magnetics (WLM) present a leap in traditional technology, which will take magnetic components from their 3-dimensional discrete shape to a planar 2-dimensional thin-film form that can be deposited with standard wafer processes on top of CMOS wafers. WLM technology is fully qualified for full-scale mass production in a high volume foundry and enables the industry's first ever Power System-on-Chips based on electroplated wafer level magnetics. Developed with a view to achieving monolithic Power System-on-Chips, the WLM technology can be easily transferred to other micro-magnetic applications, for example micro-transformers for signal isolation, micro-electromagnets for life sciences, integrated magnetic sensors for navigation and PMICs for portable consumer applications.

Increasing the switching frequency allows the use of smaller inductors utilizing electroplated WLM materials that can be post-CMOS processed on 6- or 8-inch wafers. An amorphous Fe-Co based alloy called FCA has been developed, which is capable of operating at frequencies higher than 20 MHz with minimal attenuation of magnetic properties. With wafer electroplating methods, it is possible to cost-effectively deposit photolithographically defined FCA magnetic cores on Silicon wafers. FCA's high magnetic saturation makes it suitable for use as single or multiple layers in power circuits, where it is compatible with flip-chip, wire-bonding and solder reflow packaging methods.

A secondary energy storage element are the input and output bulk capacitors necessary to provide adequate filtering of AC components to meet specific voltage ripple requirements. Similarly the amount of bulk capacitance needed for a give ripple specification is inversely proportional to operating



Development kit comprising Cyclone FPGA and Enpirion Power SoC

frequency. Therefore similar, but smaller, gains in bulk capacitor density are achievable with increased operating frequencies since parasitic equivalent series inductance and self-resonant frequencies limit the theoretical reductions in size.

PowerSoCs are available from 4 A at 190 mm² die size to 15 A at 308 mm² at an input voltage range of 4.5 to 14 V and an output voltage range of 0.6 to 5 V.

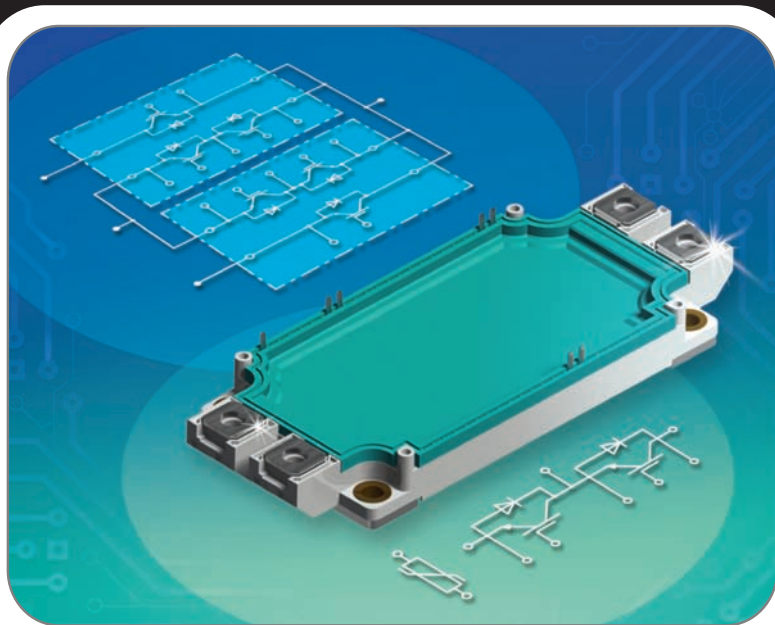
The power-optimized reference designs are offered as downloadable design packages and are demonstrated in hardware on development kits. A design package targeting Cyclone® V SoCs is available for download, with additional design packages targeting 28 nm FPGAs available later this year. Each design package contains the schematics for the FPGA's power circuits, application notes, bill-of-materials list, power tree layout guidelines and Gerber files for individual power components.

The individual PowerSoCs are still available for external customers.

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MIXB300PF1200TSF		1200	300
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MIXA600PF1200TSF		1200	600
MIXA600PF650TSF		650	490
MIXD600PF650TSF		650	600
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Automotive Graded Switcher Featuring Low Quiescent Current

Linear Technology announces a new 42 V/ 4 A synchronous step-down switching regulator. A unique Silent Switcher™ architecture reduces EMI/EMC emissions by more than 20 dB, well below the CISPR 25 Class 5 limit. Even with switching frequencies in excess of 2 MHz, synchronous rectification delivers efficiency as high as 96 % while Burst Mode® operation keeps quiescent current under 2.5 μ A in no-load standby conditions. Its 3.4 V to 42 V input voltage range makes it well suited for automotive and industrial applications.

As the power requirements in automotive power management applications continue to grow, the available space for power conversion solutions continues to shrink, requiring even higher power densities. Furthermore, the required electrical performance criterion of the switching regulators used in them becomes more demanding. For example, automotive applications running from the battery bus generally require a well regulated output voltage as low as 3.3 V, even if the input voltage can go down to 3.5 V in a cold crank or stop/start scenario and as high as 40 V in a load dump scenario. Similarly, high efficiency is important as it minimizes thermal design considerations while also maximizing battery run time in hybrids and electric vehicles.

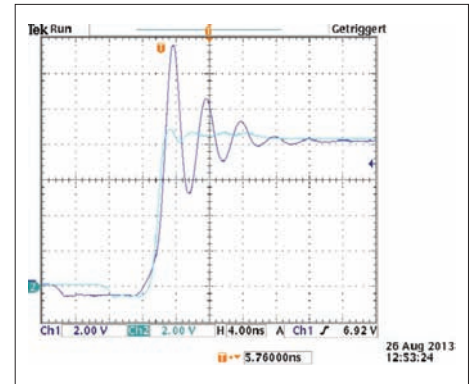
For applications such as security, navigation, safety and environmental control which are often

required to be always on, minimal quiescent current is critical so as not to drain the battery when the car is parked for extended periods of time. Reduced switching regulator EMI/EMC emissions are important to lower interference within the high density of electronics commonly found in automobiles. By using switching frequencies higher than 2 MHz, noise can be reduced in critical frequency bands such as AM radio while minimizing the size of external components. Finally, very robust short-circuit and overvoltage protection are necessary to ensure high system reliability.

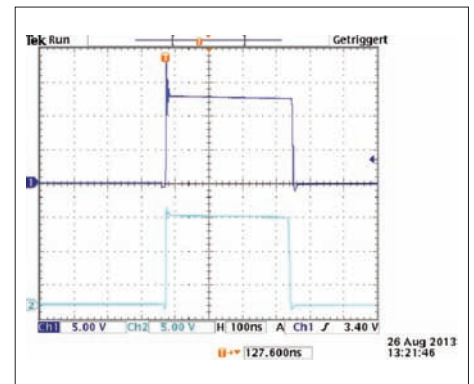
The LT8614 is the first synchronous step-down Silent Switcher architecture that has an input voltage range of 3.4 V to 42 V and delivers up to 4 A at voltages as low as 0.97 V. Its internal synchronous rectification delivers efficiencies as high as 96 %, eliminating any requirement for heat sinks while its Burst Mode® operation requires only 2.5 μ A of quiescent current, reducing the battery drain necessary for always on systems – very important since an average automobile covers around 100 ECUs (electronic control units). The LT8614 uses a unique control scheme to lower EMI/EMC emissions by over 20 dB. It also offers a minimum on-time of only 30 ns, enabling it to step-down from 16 V to 1.0 V with a switching frequency of 2 MHz. Additionally, it operates with only 200 mV at 1A of dropout under all conditions,

making ideal for applications which must withstand cold crank or soft-start scenarios.

The LT8614 utilizes internal top and bottom high efficiency power switches with the necessary boost diode, oscillator, control and logic circuitry integrated into a single die. Low ripple Burst Mode operation maintains high efficiency at low output currents while keeping output ripple below 10 mV_{PK-PK}. Other features include internal



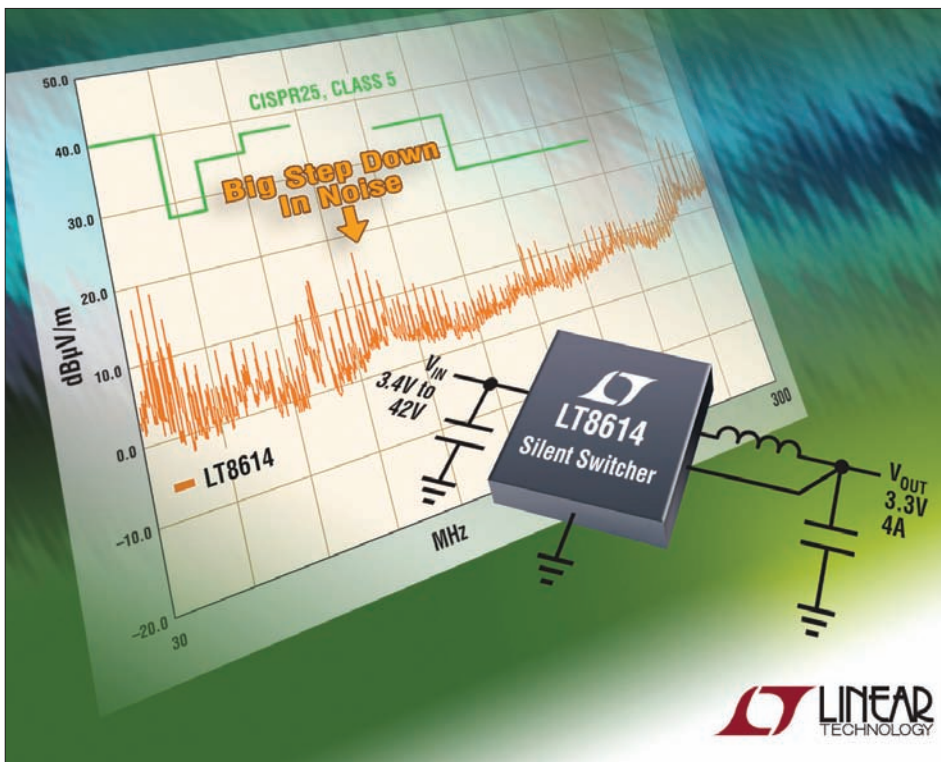
Silent switcher switching edges (lower – light blue) compared with previous switcher 8610 (upper – dark blue)



Silent switcher switch node (lower – light blue) compared with previous switcher 8610 (upper – dark blue)

compensation, a power good flag, output soft-start/tracking and thermal protection.

The LT8614EUDC is packaged in a 3 mm x 4 mm QFN package and is priced starting at \$4.25 each (1000er quantities). An industrial temperature version, the LT8614IUDC, is tested and guaranteed to operate from a -40°C to 125°C operating junction temperature and is priced starting at \$4.68 each. An automotive temperature version, the LT8614HUDC, is tested and guaranteed to operate from a -40°C to 150°C operating junction temperature and is priced starting at \$4.93 each.



Silent switcher 8614 exhibiting ultra low EMI emissions

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Issue 7 2013 Power Electronics Europe

New Thermal Design Options Drive Power Density

With every generation, electronic products shrink while functionality expands and performance improves. Despite efforts to hold the line on product power dissipation, pressure to increase power density in energy-management subsystems continues unabated. This trend, unfortunately, exacerbates the challenging thermal design task product development teams already face. A new packaging approach delivers more power in reduced space. **Gary Gill, Director VI Chip Product Line, Vicor, USA**

Heat from power components causes several problems - underperforming thermal designs result in high operating temperatures, which can reduce power-component reliability and, in dense applications, reliability of other nearby devices. In high-temperature environments, power derating reduces the amount of current a power component can deliver - a trait that can force system designs to be larger, heavier, and more expensive. Thermal designs that are inefficient near heat generating components - be they in the power-sourcing components or power loads - can force design changes elsewhere in the system. These include increased airflow requirements to maintain dissipative devices within their safe operating temperature range. Increasing a cooling system's airflow requirement also increases its energy use, increasing the system's operating costs.

Minimizing heat generation

The first line of defense, then, is to minimize heat generation throughout the power subsystem design. Minimize I²R losses, starting at the power entry point. For example, 400-VDC power distribution in data centers reduces copper losses in power feeds by a factor of 69 below those of 48-V distribution systems for the same size copper feeds. Smaller power savings are available with smaller feed dimensions, allowing system designers to split the savings between a system's acquisition and operating costs. 270-VDC distribution provides similar benefits in airborne systems.

Efficient power-subsystem designs minimize the number of conversion stages from power entry to point of load. They also take advantage of highly efficient power-conversion topologies. These include ZVS (zero-voltage switching) and ZCS (zero-current switching).

Minimizing the number of conversion stages while efficiently accommodating

high power-entry voltages challenges traditional converter designs. Fortunately, high voltage-ratio applications have inspired alternative power architectures and conversion topologies.

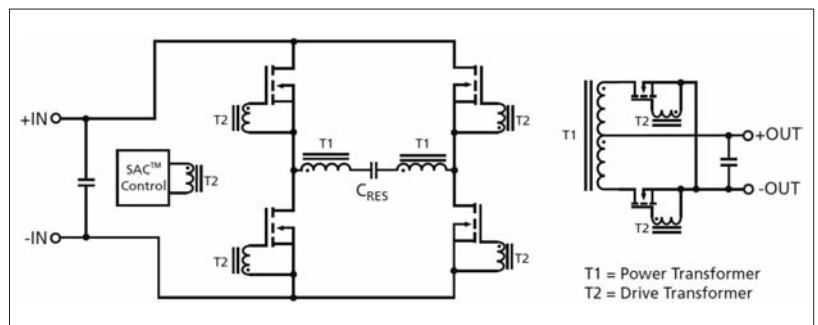
A SAC™ (Sine Amplitude Converter [1]) illustrates architectures that can provide high voltage-ratio conversion, high efficiency, and low output ripple (Figure 1). For example, Vicor's VTM implementation of the SAC topology can provide fixed voltage ratios between 1:1 and 40:1 allowing single-stage 48- to 1.2-V conversion for POL applications at up to 98 % efficiency.

This approach reduces output ripple by about 1/3, substantially reduces the noise

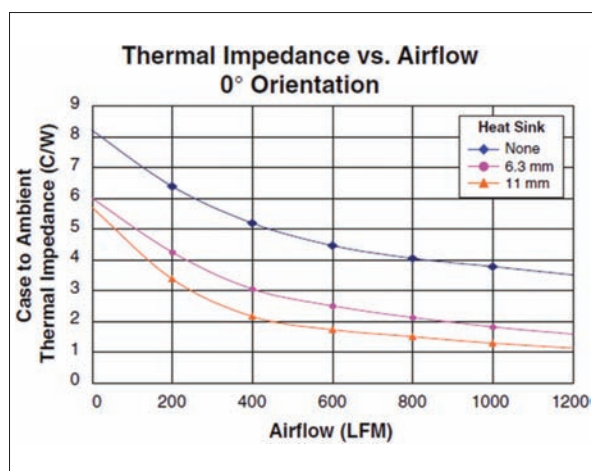
energy at harmonics of the switching frequency, and provides about five times faster load-step response than traditional topologies. Such performance reduces the need for output bulk capacitance, it also allows for a tighter circuit-board layout, which helps reduce I²R losses in the highest current section of the power subsystem - the point of load. Overall, taking advantage of such technologies can reduce heat-generating conversion losses by as much as 40 % compared to traditional power-conversion schemes.

Improving thermal design

No matter how efficiently your power



ABOVE Figure 1: A SAC™ (Sine Amplitude Converter) is a resonant topology that switches its power MOSFETS at fixed frequency at zero-crossing points. The topology reduces power dissipation and high-order harmonics



LEFT Figure 2: Heatsinks reduce case to ambient thermal impedance, shown here as a function of airflow over a representative encapsulated power module

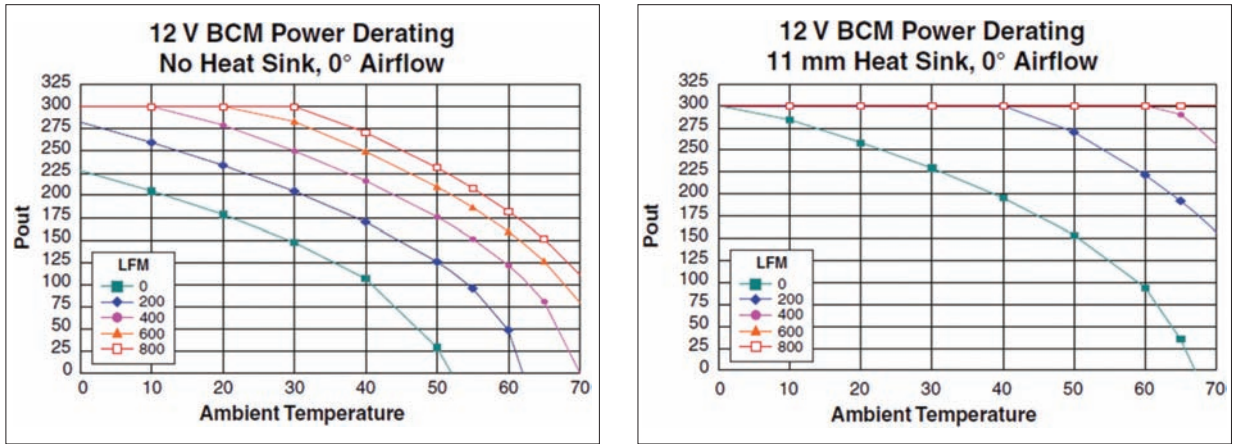


Figure 3: Derating curves, such as these for a Vicor 12-V BCM show the effect of airflow on realizable power capacity in designs with no heat sink (left) and with an 11-mm heat sink (right)

subsystem delivers energy, the residual dissipation and your ability to remove heat from the system limits power density. Once generated, there are two basic methods of removing heat from the power subsystem: convection and conduction.

The effectiveness of convection cooling - blowing air across the device's top surface - is a function of inlet air temperature, air flow rate, air flow impedances or disruptions, and the device's case temperature. Conduction cooling depends on a thermo-mechanical connection to draw heat from a high-temperature region to a cooler one. Its effectiveness derives from the device temperature, heat sink size and material, the thermal interface material and thickness, and the cool-region temperature (Figure 2).

For devices that use heat sinks contained within the system chassis, cooling is ultimately a two-stage process: conduction from device to heat sink and convection from heat sink to ambient. Thermal calculations must consider both stages. Some power-converter manufacturers mitigate this issue by providing heat sinks or references to commercial suppliers' catalog parts.

Design-support tools can range from simple tables and charts to sophisticated simulation software. Manufacturer's

thermal-performance graphs can provide quick and useful insight into a power component's performance under a variety of configurations and operating conditions. Derating curves for no-heat-sink operation (Figure 3 left) and for operation with manufacturer-specified heat sinks (Figure 3 right) allow to align thermal and electrical designs. They help coordinate these two aspects of product's performance at the very start of the design cycle and give the electrical- and thermo-mechanical-designers important data with which to balance design trade-offs.

General-purpose tools, such as FEA (finite-elements array) analyzers, can model and simulate virtually any configuration and thermal design. But FEA tools tend to be expensive and require specialized knowledge to use effectively. Product-centric analysis tools, by contrast, are often free of charge and take mere minutes to learn.

The trade-off is that these tools are usually specific to a particular manufacturer's product lines and may limit the thermo-mechanical configurations which can be simulated. This restriction, however, has a silver lining: by limiting the thermo-mechanical design, the manufacturer-supplied simulation tools can guide the user to those that the

manufacturer has developed and proven effective, potentially saving a substantial fraction of the thermal-design schedule and engineering costs.

One example of such simulation tools is Vicor's PowerBench™ simulator, which provides seven simulation types: VIN startup, EN (enable) startup, EN shutdown, VIN step, load step, steady state, and thermal. The Power Bench simulation environment provides an application circuit with user settable operating conditions for source and load and adjustable parameters for input- and output-circuit components (Figure 4). The thermal simulation shown provides means to select between designs using a 6.3-mm or 11-mm heat sink or a cold plate. The ambient temperature, circuit board temperature, air velocity, interface thickness, and interface conductivity can also be set. Among the output data the thermal simulation provides are the output power, power loss, efficiency, heat loss through the case, heat loss through the circuit board, and device operating temperature.

The simulation results from Figure 4 report that the circuit delivers 326 W to its load with an efficiency of 95.54 %, resulting in 15.21 W of power loss. The simulation calculates the power

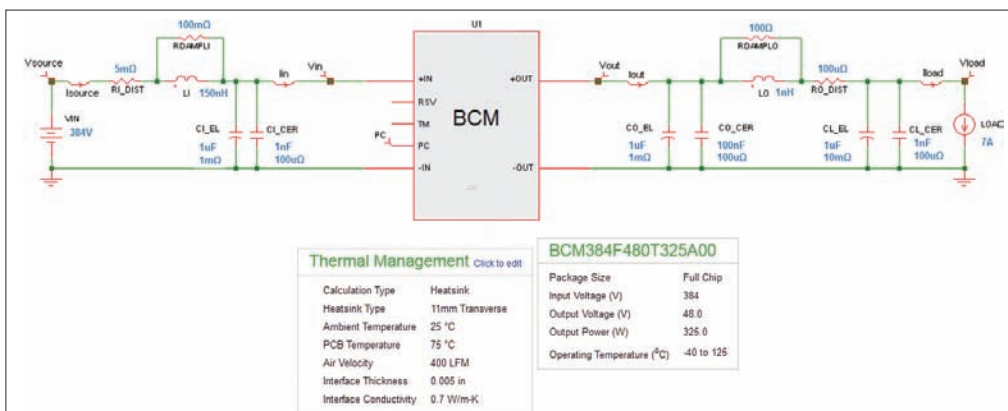


Figure 4: Vicor's Power Bench™ simulator is a powerful online design-support tool that includes thermal simulation among its seven simulation types

component's operating temperature under the stated conditions at 80°C - only 5 K warmer than the circuit board, indicative of the power converter's high efficiency and the heat sink's efficacy.

Power packaging

Most components, and certainly most power-dissipating components, within power conversion modules mount to the top side of the converter module's PCB. For simplicity, most product designs cool power modules and power ICs through their top surfaces.

There are, however, multiple heat sinking paths available. As product requirements drive power densities higher, thermal designs more sophisticated than simple topside cooling take advantage of other options.

In many power-converter structures, the majority of dissipated energy comes from power MOSFETs and power-carrying electromagnetic components. Fortunately, these parts usually connect directly to the pins that form the device's electrical and mechanical interfaces to the application PCB. The same pins can conduct heat out of a power converter's package if the underlying PCB design provides appropriate thermal features.

Through-hole mounting is more efficient than surface mount for heat conduction through the power package's pins, but both technologies can contribute to the product's thermal performance. The PCB's design must account for the additional heat from the power devices and the proximity of those devices to other dissipative components, such as processors.

New power packaging technologies and materials allow OEM designers to depart from topside dominant cooling. Power-train designs that arrange dissipative components symmetrically on both sides of a module's PCB coupled with highly thermally conductive packaging materials allow substantial cooling through the package's top and bottom surfaces. Additionally, this arrangement can shrink the module's layout, increasing power density while increasing efficiency by reducing I²R losses in the interconnecting copper traces.

One example of packaging currently available for two-sided cooling is Vicor's new ChiP (Converter housed in Package) technology, which presents similar thermal resistances through top and bottom surfaces. ChiP packaging supports power-management functions such as AC/DC conversion with PFC (power-factor correction); isolated bus conversion; DC/DC conversion; buck, boost, and buck-boost regulation; and PoL current

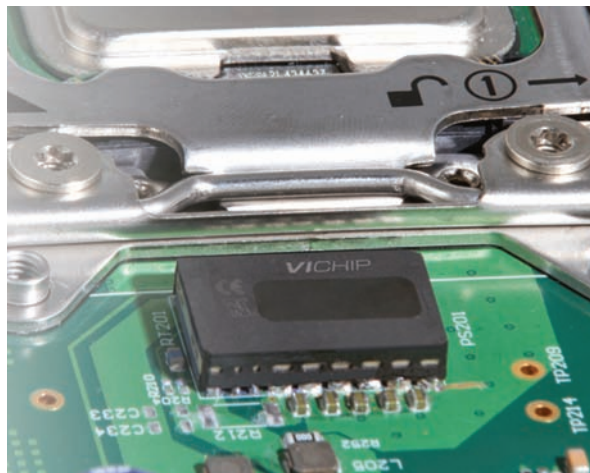


Figure 5: A 1323 size VTM current multiplier ChiP supports tight layout, supplying a processor directly from a 48-V bus with no PoL bulk capacitors

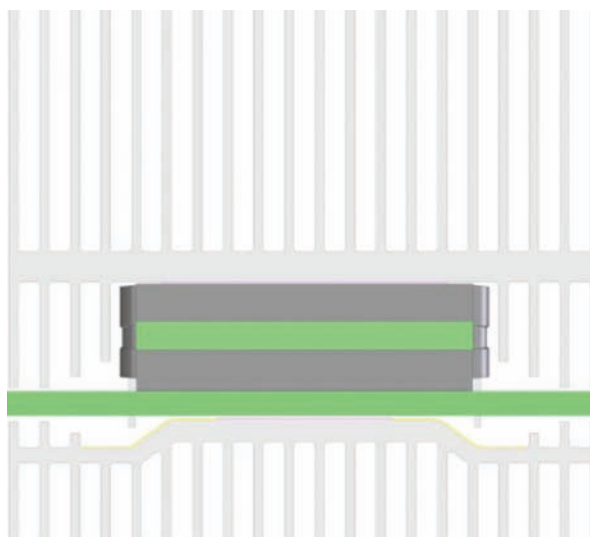


Figure 6: A thermal management cell-based design supports power densities in excess of 200 W/in³ and power outputs to 1.8 kW/cell. The design readily scales for larger systems of multiple cells

multiplication (Figure 5).

Power components exploiting ChiP technology can provide exceptional thermal performance in two-sided cooling applications [2] (Figure 6). The thermal-management cell, depicted schematically in the figure, targets an $R_{\theta JA}$ (junction-to-ambient thermal resistance) less than 0.66 K/W, allowing for dissipation greater than 60 W at 70°C ambient. The thermal-management cell concept supports power densities in excess of 200 W/in³ and outputs to 1.8 kW/cell with 400 VDC inputs under the same ambient conditions. The cell uses a single 40- x 40-mm fan to cool both top and bottom heat sinks and is inherently scalable for larger outputs.

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New ChiP packaging platform

The initial lineup of Vicor components based on the ChiP packaging platform includes five different package sizes, with more on the way. This is enabled by the underlying scalability of the ChiP manufacturing process.

Analogous to semiconductor wafer fabrication, individual ChiP-based components are arrayed to utilize 100 % of the PCB material, with no area lost to lead/pin attach. The array is then sawn into individual 'chip-scale' components with no superfluous, non-value-added packaging, thus minimizing space used in customer designs. The sawing process exposes "bar codes" from which interconnect terminals are formed. X- and y-dimensions are flexible, allowing low- or high-power converters, with additional flexibility in the z-axis to allow optimized magnetic transformer or inductor designs. The first entry in ChiP-based power component portfolio will arrive to market later this year, and will be targeted at datacenter, telecom and industrial applications.

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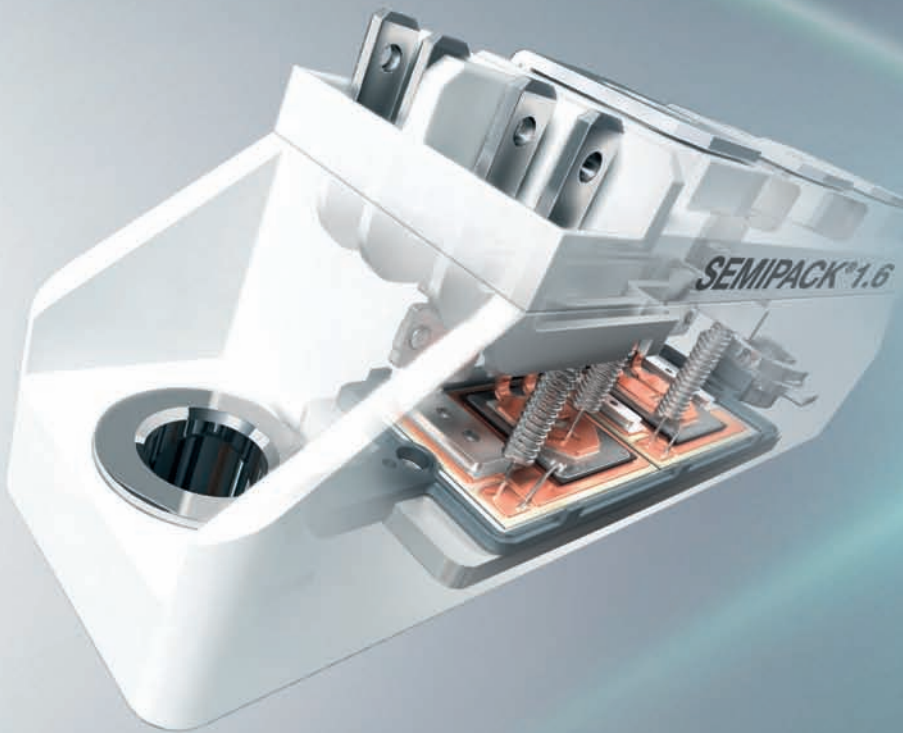
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Solar Inverter Performance Improvement Utilizing 650 V HighSpeed 3 IGBT Power Modules

For applications which require an output filter or have a boost/buck choke, higher switching frequencies can lead to advantages on system level. One application where both can be found is a solar inverter. At the state-of-the-art efficiency and power density, high cost pressure can be observed for solar inverters. In this article, the difference between the 650 V IGBT3, 650 V IGBT4 and the 650 V HighSpeed 3 (HS3) IGBT from Infineon Technologies used in power modules will be described. It will be shown that due to the device design, the 650 V HS3 IGBT provides a superior performance and can be used as a highly efficient switch. **Jens De Bock and Christian R. Müller, Infineon Technologies AG, Warstein, Germany**

The trench-field-stop technology is the most common concept for modern IGBTs with blocking voltages in the range of 600 V to 1200 V. This technology allows implementing devices with low on-state voltages and soft switching on the one hand and low switching losses and a MOSFET-like switching performance for high-frequency applications on the other hand. Within this technology, the device performance is mainly controlled by design parameters like cell geometry, chip thickness, and doping profile. For instance, by adjusting these parameters, devices with a high carrier density in the drift region can be implemented. Such devices provide a low $V_{CE\text{ sat}}$ and achieve low static losses. During the turn-off, a high carrier density leads to a slower clear out of the device and the dynamic losses are increased. Therefore, the performance of an IGBT can be either optimized for high-frequency applications like solar inverters or boosters, which need devices with low dynamic losses, or for low-frequency applications, which benefit from low static losses.

The HighSpeed IGBT is optimized for high-frequency hard-switching applications [1]. Therefore, this device is an ideal choice for power modules which are used in solar applications.

Electrical setup

For the measurements, a 650 V IGBT3, a 650 V IGBT4, and a 650 V HS3 IGBT with a nominal collector current of 50 A

were used. The electrical performance of the chips is determined by measuring the switching losses. For the measurement each chip was integrated in an EasyPACK 2B power module with an identical electrical circuit and a stray inductance of 17 nH. Due to the fact that the turn-on losses E_{ON} are mainly dominated by the free-wheeling diode used, all chips were operated with a 650 V emitter-controlled diode with a nominal current $I_F = 30$ A.

A setup with an integrated current probe and a stray inductance $L_\sigma = 25$ nH was used. The DC-link voltage was set to $V_{DC} = 400$ V, which is a typical voltage in the application and the chips were operated at

nominal collector current $I_c = 50$ A. To drive the IGBT, a gate-emitter voltage $V_{GE} = \pm 15$ V was used. All measurements were performed at $T_{vj} = 25$ °C.

Switching behavior and chip comparison

The switching behavior of the chips is measured with the setup described. The corresponding energies and the characteristic switching parameters are extracted from the turn-on and turn-off waveforms.

Figure 1 displays the switching losses for HS3 IGBT, IGBT3 and IGBT4 for identical switching parameters. R_G was modified in the way that $di/dt = 1.5$ kA/ μ s and dv/dt

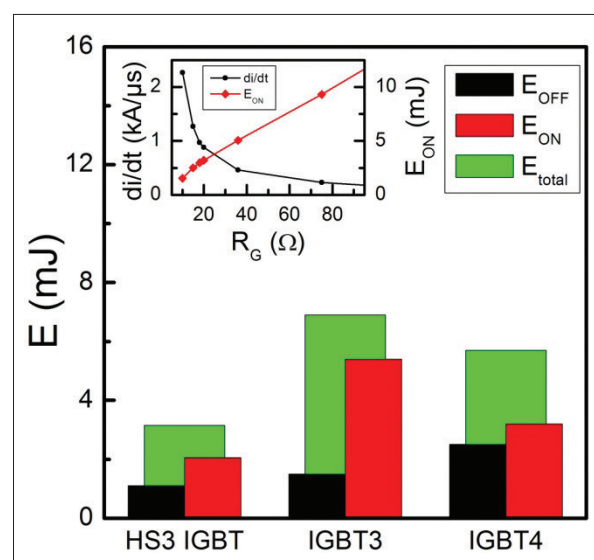


Figure 1: Comparison of the switching energies E_{ON} , E_{OFF} , and E_{total} with identical di/dt during turn-on and dv/dt during turn-off for HS3 IGBT, IGBT3, and IGBT4 (Inset: E_{ON} and di/dt of the HS3 IGBT versus R_G)

= 4.5 kV/μs were achieved during turn-on and turn-off respectively. The HS3 IGBT has the lowest switching losses E_{ON} and E_{OFF} and, in sum, E_{total} is less than half compared to the IGBT3. The inset shows E_{ON} and di/dt of the HS3 IGBT versus R_G . E_{ON} increases and, in turn, di/dt decreases with increasing R_G . Especially for $R_G < 20 \Omega$, $di/dt > 1 \text{ kA}/\mu\text{s}$ can be achieved whereas larger R_G lead to di/dt below 0.5 kA/μs.

The low turn-off losses indicate the superior switching performance of the HS3. Therefore, the HS3 IGBT is optimized for high-frequency applications and, with respect to the trade-off between E_{OFF} and $V_{CE,sat}$, provides low dynamic losses. With a high gate resistor the turn-on losses of the HS3 IGBT are quite high and, in turn, are attributed to the very low di/dt . To compensate for this, it is necessary to significantly decrease the turn-on gate resistor. One possible way for

implementation is to use a more sophisticated gate-driver design which allows operating the HS3 IGBT as a very efficient switch.

HS3 IGBT under operating conditions

Above it was shown, that the HS3 IGBT outperforms IGBT3 and IGBT4 in high-frequency applications. The upcoming question is how the HS3 IGBT performs under operating conditions. Under typical operating conditions in a solar inverter, the HS3 IGBT will mainly be operated with collector currents lower than the nominal chip current. In addition, the DC-link voltage may vary over a mentioned wide voltage range. Therefore, the switching losses of the HS3 IGBT are analyzed for DC-link voltages in the range of 150 V to 450 V and for collector currents up to the nominal chip current.

For the measurement, $R_G = 15 \Omega$ was used in the gate-driver circuit. Figure 2

shows the switching losses of the HS3 IGBT versus the DC-link voltage. For low V_{DC} , E_{OFF} is low and increases linearly with increasing V_{DC} , higher collector currents result in higher turn-off losses. In contrast to this, it is found that E_{ON} increases disproportionately with V_{DC} and I_C as well. For $I_C = 10 \text{ A}$, the slope of E_{ON} versus V_{DC} is almost constant. At $I_C = 30 \text{ A}$ and 50 A , a steeper slope for $V_{DC} \geq 300 \text{ V}$ is observed. In the inset, this disproportional increase is also identified for E_{total} .

These measurements show that, compared to the turn-on losses, the turn-off losses of the HS3 IGBT have minor impact on the device performance. Due to the disproportional increase of the turn-on losses for $V_{DC} \geq 300 \text{ V}$ at $I_C \geq 30 \text{ A}$, the highest efficiency can be achieved at low collector currents. The high turn-on losses for larger V_{DC} and I_C are attributed to a reduction of the di/dt . This effect is characteristic for the HS3 IGBT and is related to the device design. One way to compensate this effect is the reduction of R_G which, in turn, leads to a decrease of the softness.

When fast-switching devices are used, an upcoming requirement for the application is the reduction of the stray inductances in the setup [2, 3]. Hence both, module and setup must provide a low inductance to avoid parasitic effects. Two of the most common effects, closely related to stray inductances, are the over-voltage peak V_{Peak} on the collector-emitter voltage and the reduced switching losses due to the collector-emitter voltage drop during turn-off and turn-on, respectively.

Figure 3 displays the switching losses and the over-voltage peak of the HS3 IGBT versus the stray inductance of the setup for identical switching parameters, $di/dt = 1.5 \text{ kA}/\mu\text{s}$ and $dv/dt = 7.2 \text{ kV}/\mu\text{s}$ for $V_{DC} = 400 \text{ V}$ and $di/dt = 1.6 \text{ kA}/\mu\text{s}$ and $dv/dt = 6.0 \text{ kV}/\mu\text{s}$ for $V_{DC} = 300 \text{ V}$. With increasing L_r , the turn-off energy increases slightly whereas the turn-on energy decreases significantly. As a result, the total switching energy is reduced for larger L_r . This general trend is independent of the applied DC-link voltage. On the other hand, large L_r leads to a raise of V_{Peak} . As a consequence, the DC-link voltage in the application becomes limited. A countermeasure for this is to reduce the switching speed by increasing R_G , which in turn, results in higher switching losses.

Increasing the stray inductance of the setup reduces E_{total} of the IGBT due to the fact that the reduction of E_{ON} is more pronounced than the increase of E_{OFF} . However, parasitic effects like oscillations caused by resonance frequencies of the setup or the diode snap-off will lead to

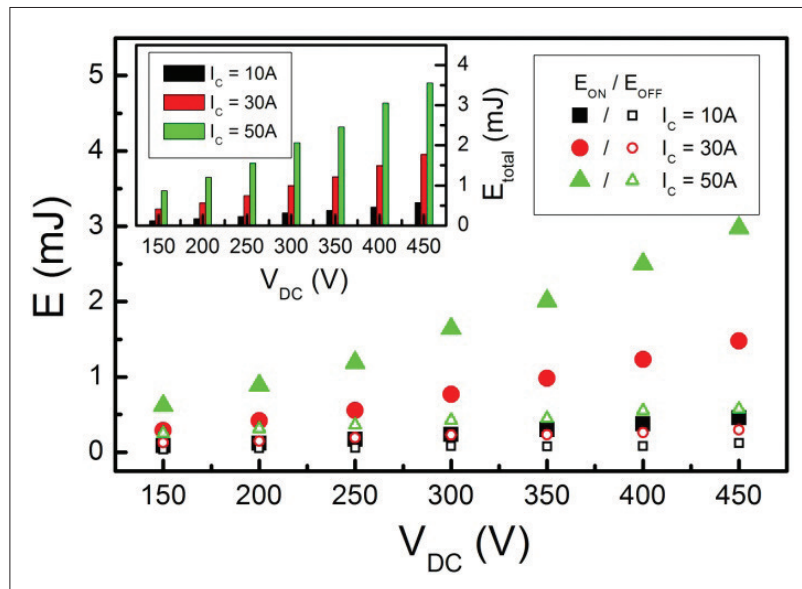


Figure 2: Switching energies E_{ON} and E_{OFF} of the HS3 IGBT versus the DC-link voltage for $I_C = 10, 30,$ and 50 A (Inset: E_{total} of the HS3 IGBT versus the DC-link voltage for $I_C = 10, 30,$ and 50 A)

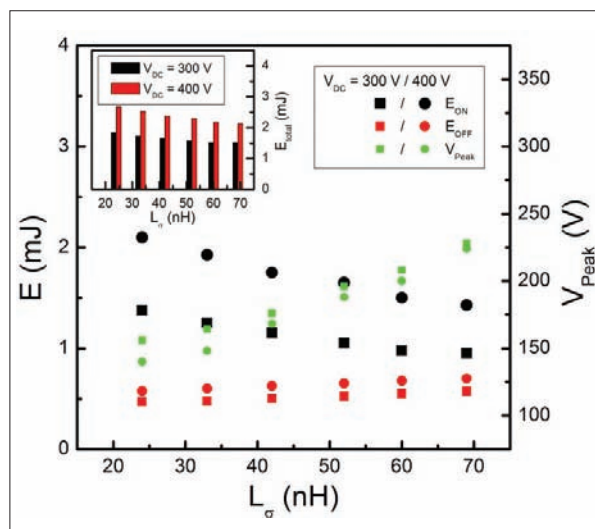


Figure 3: Switching energies E_{ON} and E_{OFF} and V_{Peak} of the HS3 IGBT versus the stray inductance for $V_{DC} = 300$ and 400 V (Inset: E_{total} of the HS3 IGBT versus the stray inductance for $V_{DC} = 300$ and 400 V)

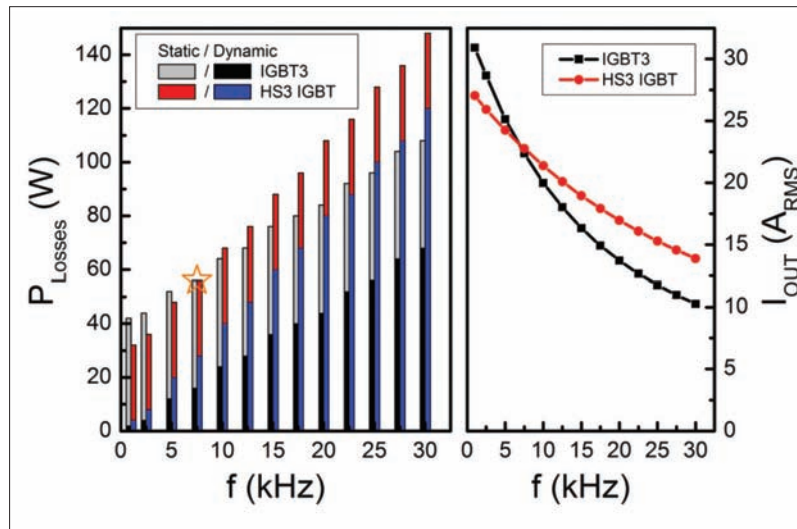


Figure 4: Simulated semiconductor power losses of HS3 IGBT and IGBT3 in an H-bridge inverter topology versus switching frequency (left). The simulated power losses are the power losses of the H-bridge inverter and not of a single chip. Maximum achievable output current versus switching frequency for HS3 IGBT and IGBT3 (right)

electromagnetic interference, which has to be considered in the application [4].

Simulated device performance

To analyze the device performance for different switching frequencies, the inverter performance was simulated using IPOSIM [5]. To ensure comparability, the dynamic losses of HS3 IGBT and IGBT3 shown in Figure 1 are considered. In the simulation, the output current of a single-phase H-bridge with an output power of 4 kVA was calculated under the following operating conditions: The output current I_{OUT} was set to 17.4 A RMS and a power factor of 1.0. The modulation index was 0.8 and the DC-link voltage was 400 V. For both devices, an identical thermal situation with a fixed heat-sink temperature of 80°C was used.

Figure 4 shows the simulated semiconductor power losses P_{Losses} in an H-bridge inverter under the operating conditions mentioned above. The analysis of the H-bridge inverter shows that the static losses of the IGBT3 are only about 70 % of the static losses of the HS3 IGBT. With increasing switching frequency f the dynamic losses become dominant. For $f =$

7.5 kHz, the overall losses of the HS3 IGBT are equal to the overall losses of the IGBT3 as highlighted in Figure 4. A further increase of the switching frequency amplifies this effect and it can be clearly seen that the advantage of the HS3 IGBT comes to the fore at higher switching frequency. On the right-hand side, the maximum achievable output current is displayed. For the calculation, the above mentioned operation conditions were used, whereas I_{OUT} was not fixed but limited by the maximum junction temperature of the devices.

With increasing frequency I_{OUT} decreases. At low switching frequencies, the IGBT3 provides higher maximum output current than the HS3 IGBT. For $f \geq 7.5$ kHz, the output current of the HS3 IGBT is higher than the output current of the IGBT3. The difference between I_{OUT} of HS3 IGBT and IGBT3 increases at higher switching frequencies.

Conclusion

In this article, a comparison of HS3 IGBT, IGBT3 and IGBT4 is presented. It is shown that the HS3 IGBT outperforms IGBT3 and IGBT4 in high-frequency applications by

providing up to a factor of 2 lower switching losses. To take advantage of the superior switching performance of the HS3 IGBT, an application-optimized operation mode is needed. Therefore, the operating current and the gate resistor have to be considered carefully. For the latter, one possible way is to use a more sophisticated gate-driver design.

The HS3 IGBT is a cost optimized highly efficient switch for high-frequency hard-switching applications like solar inverters or UPS. The results of the simulation support these findings and show that the HS3 IGBT should be considered as state-of-the-art switch for applications which are operated with switching frequencies exceeding 7.5 kHz.

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Power Module Design for an Efficient Three-Level Utility Grid Solar Inverter

The race to achieve highest efficiency had engineers turning to innovative topologies and new components such as SiC to take the lead. In parallel, after years of dormancy, old but very innovative ideas such as the mixed-voltage NPC topology have been rediscovered and put to good use in many solar inverter applications. Surprisingly, all these efforts have focused on the power range up to 100kW, while standard two-level topologies with low switching frequencies continue to dominate in the range beyond 100 kW. The new power module design transcends the limitations associated with >100 kW power inverters to accommodate high switching frequencies and innovative topologies based on standard Si components.

Michael Frisch and Temesi Ernő, Vincotech Germany and Hungary

Parasitic effects such as stray inductance and diodes' reverse recovery characteristics are the main obstacles to achieve high switching frequencies for ultra high efficiency solar inverter applications ranging beyond 100 kW. The overvoltage spike caused by parasitic inductance limits the turn-off switching speed. And increased turn-on switching speed comes at a high price - losses and increased electromagnetic interference (EMI) caused by the freewheeling diode's reverse recovery characteristics. The new power module design described here takes advantage of advances in power modules - for example, the 3-level topologies used in low-power solar applications - and exploits this parasitic inductance to reduce turn-on losses. Parasitic inductance at turn-off can be bypassed with low-inductive transient current management. A special topology for paralleling MOSFET with IGBT is

presented here to show how promising the prospects of this advanced new module design can be.

Standard 2-level inverters achieve around 95 % efficiency at 16 kHz, so a 200 kW inverter will suffer about a 10 kW loss. Power dissipation has to be reduced by 80 % to achieve the targeted 99 % efficiency. This can be done by minimizing switching losses in four 4 steps:

- Reduce the switched voltage with a three-level topology.
- Use a low inductive design that accommodates fast components.
- Achieve asymmetrical inductance, reduce turn-on losses and regenerate energy stored in the parasitic inductance.
- Capitalize on the benefits of advanced paralleling.

Why a three-level topology?

Three-level topologies are certainly known

for reducing switching losses ($P_D = \int I_{CE(t)} \times V_{CE(t)} \times dt$), but this is not their only advantage. The reduced current ripple halves the output filter effort and losses at the same PWM frequency.

Reducing the switched voltage also reduces switching losses by 50 %. An additional reduction is possible because of the freewheeling diode's lower voltage rating. With the benefit of a mixed-voltage neutral clamped converter (MNPC) topology, the freewheeling diodes' voltage rating is just half that of a two-level half-bridge. The blocking voltage drops from 1200 V to 600 V (Figure 1). The 600 V diodes' reverse recovery charge is much lower, which reduces turn-on losses. The total turn-on losses are calculated as the sum of the diode's reverse recovery losses and turn-on losses in the switch, which are also influenced by the freewheeling diode's recovery characteristics.

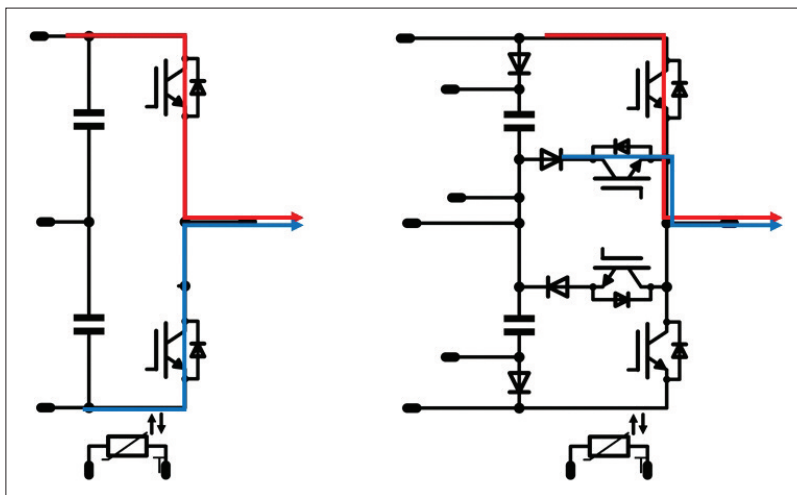
All this reduces total losses by 50 % (turn-on and turn-off) with a 3-level topology, and by 30 % to 60 % (turn-on) with 600 V diodes, depending on the switch's characteristics.

Low inductance for fast components

While fast diodes reduce turn-on losses, require fast switches a low-inductive design that solves the problem of voltage overshoot at turn-off

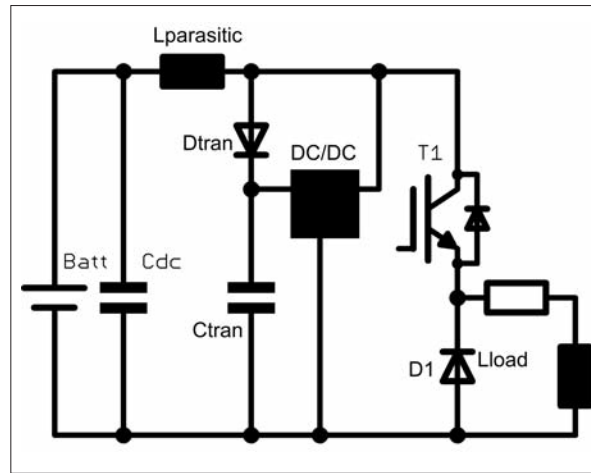
$$(V_{CE(peak)} = V_{CE} + L \times di/dt).$$

High inductance precludes the use of fast components with high di/dt at turn-off.



LEFT Figure 1: Switched current and freewheeling path in a 2-level inverter (left) vs. a 3-level MNPC inverter during a positive half wave

Figure 2:
Asymmetrical inductance in a switching circuit with stored energy regeneration



The overshoot dilemma increases with rising inductance (L) and switched current (I). Even lower inductance values are necessary to manage overcurrent and short-circuit problems. Reducing parasitic inductance also reduces voltage overshooting and turn-off losses. And it allows fast components to be used to accelerate turn-off, which is even more important to reducing switching loss. All this can reduce total turn-off losses by around 20 % to 60 %. Acceleration at turn-on also depends on the diode.

Regenerating Energy Stored in the Parasitic Inductance

The low inductive design and fast components already reduce switching losses, and the low-inductive environment also allows to exploit parasitic effects to further reduce switching losses and improve EMC. Inductance is very welcome at turn-on. However, ultra-low inductance is vastly preferable at turn-off – hence the term asymmetrical inductance.

The idea here is to make the most of parasitic inductance $L_{parasitic}$ at turn-on and avoid it altogether at turn-off. To this end, the diode D_{tran} consigns the energy stored in the parasitic inductance to the integrated capacitor C_{tran} during turn-off. The stored energy circulates in $L_{parasitic}$, D_{tran} and R_{tran} until it is dissipated in the parasitic resistor. Although we are able to relieve the semiconductor of switching losses with this circuit, some energy has to be dissipated in passive components. One way to increase overall efficiency is to regenerate energy stored in a DC/DC circuit (Figure 2).

The new asymmetrical setup's switching losses are lower. The overshoot at turn-off is minimized. Turn-off losses are lower. What's more, all switching losses are reduced. The circuit's reverse recovery behavior explains the lower turn-on losses. The reverse recovery current through diode $D1$ boosts the current of transistor $T1$ at turn-on. The current is reduced during

recovery, but the additional energy stored in the parasitic inductance $L_{parasitic}$ causes an overvoltage at the transistor's collector, so the energy will flow into the capacitor. This reduces the reverse current in the diode. The voltage drops in the transistor, resulting in significantly reduced switching losses.

Advantages of the Asymmetrical Inductance include superior switching performance with standard components - increased turn-on inductance reduces peak current in the transistor, which is a major source of EMI. No laminated bus bars required - increased inductance in the DC input is now welcome and will further reduce loss at turn-on. This means the expensive laminated bus bars used for a low inductive connection with the DC capacitor bank are no longer necessary. Reduced voltage swing of onboard capacitors - these capacitors are not discharged during turn-on, so their voltage swing and dissipation is drastically reduced. The transient diode eliminates any ringing between the DC link and the onboard snubber capacitors. Asymmetrical

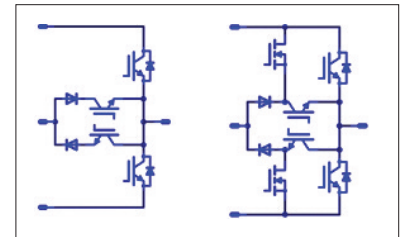


Figure 3: Mixed voltage NPC (left) and advanced paralleled NPC topology (right)

inductance reduces switching losses by 10 % to 30 %, depending on the parasitic inductance, while extending the safe operating range at turn-off (RBSOA).

Advanced paralleling

The goal is to bring together the benefits of standard NPC (lowest switching losses) and mixed-voltage NPC (Figure 3 left) (lower static losses) topologies with a paralleled fast component (e.g. a MOSFET) and a component with low voltage drop (e.g. an IGBT) to create an advanced paralleled NPC topology (Figure 6 right). This special circuit allows a 1200 V IGBT to be paralleled with 600 V MOSFETs. Both the MOSFET and the IGBT are turned on simultaneously. The MOSFET is the faster device, so the current at turn-on flows to it. The IGBT turns on with low voltage. The voltage drop in the IGBT is lower, so then most of the current flows to the IGBT. The MOSFET's gate signal is delayed at turn-off. The IGBT turn off, and then the MOSFET takes over the current and turn off with a delay of 0.2 μ s to 1 μ s.

To get access to those advantages are some challenges to be solved. At parasitic turn-on the MOSFET turns off quickly, so the high dV/dt could send voltage into the paralleled IGBT's gate. It is already off, so this could trigger a parasitic turn-on. This

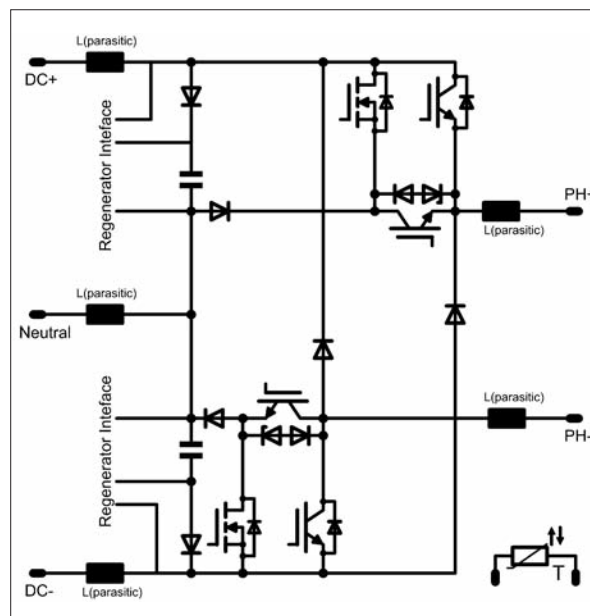


Figure 4: One phase of the 3-phase power module with advanced paralleled asymmetrical inductance, split output and regeneration interface

problem is remedied with a negative gate bias and/or a capacitor inserted between the gate and emitter.

Regarding IGBT tail current - current flows to the MOSFET after the IGBT switches off. The IGBT turns off at zero voltage, but it will conduct again if the space charge region is not fully rebuilt. Turn-off efficiency will suffer as a result of this tail current. This problem is fixed by setting an ideal delay time between the IGBT and MOSFET and/or selecting an IGBT with good zero-voltage turn-off behavior. Measurements show that the advanced paralleled NPC topology halves switching losses.

A power module with four efficiency improvements

Each of the four steps has been shown to be a viable improvement. And a module-based inverter solution proves how effective a combination of all four can be.

Figure 4 shows the inverter's circuit diagram (only one phase of three is shown). The inductance $L_{\text{parasitic}}$ represents the power module's stray inductance. The power module (Figure 5) incorporates all power semiconductors of the inverter, the snubber diodes and the snubber capacitors. The circuit converts DC voltage from the solar panel into a three-phase AC voltage for the public power grid. The inductors shown in the DC path ($L_{\text{parasitic}}$) represent the parasitic inductance in the DC power module's connection.

The three-phase inverter circuit and the output filter (inductor) convert DC current into a sinusoidal output current. The regeneration circuit connected to the inverter module regenerates the energy stored in the onboard capacitors.

Efficiency boost

The measured results serve to determine the efficiency of an inverter circuit. This calculation does not include losses of passive components such as the output

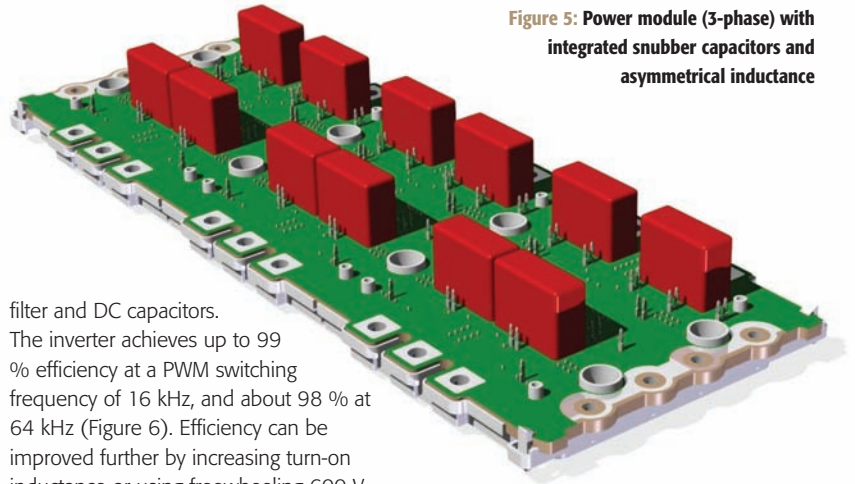


Figure 5: Power module (3-phase) with integrated snubber capacitors and asymmetrical inductance

filter and DC capacitors.

The inverter achieves up to 99 % efficiency at a PWM switching frequency of 16 kHz, and about 98 % at 64 kHz (Figure 6). Efficiency can be improved further by increasing turn-on inductance or using freewheeling 600 V SiC diodes in the neutral path. It is expected that the version with SiC diodes will reduce turn-on losses by around 30 % to 50 % (Figure 7).

Conclusions

Conventional power designs can be improved by revisiting the fundamentals of power electronics.

Multilevel topologies have been with us for many years to satisfy widespread demand for higher efficiency. This type of topology reduces switching losses by at least 50 %. The low-inductive design ensures fast, reliable turn-off in high-current power modules and reduces voltage overshoot. Low inductive designs provide the platform for all other ideas about incorporating fast components, high transients and reduced switching losses in high-power applications. Asymmetrical inductance drives down switching losses, EMI and effort for inverter hardware. Low inductive bus bars are no longer necessary. A flexible, low-cost cable connection may be used in the DC link. The parallel switch technology achieves highest efficiency at elevated switching frequencies of 50 kHz and beyond.

Further improvements with SiC freewheeling diodes in the neutral path is feasible

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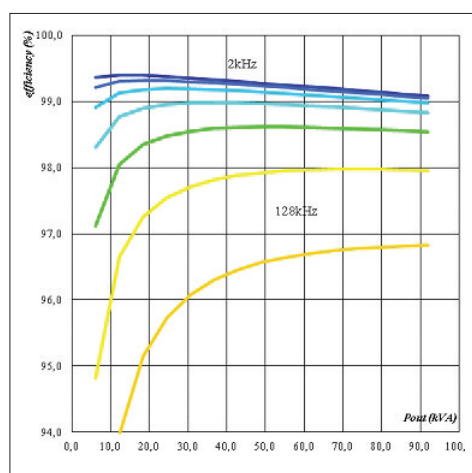
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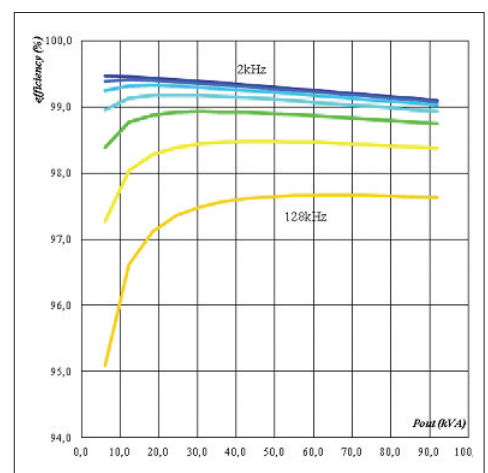
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LEFT Figure 6: Advanced paralleled NPC - efficiency vs. switching frequency in steps from 2 kHz to 128 kHz: It doubles with each step – 2, 4, 8, 16 kHz (blue), 32 kHz (green), 64 kHz (yellow), 128 kHz (orange)

RIGHT Figure 7: Estimated efficiency with SiC diodes in the neutral



The Power and Potential of Piezoelectric Energy Harvesting

The process of piezoelectric energy harvesting – that of converting mechanical energy into electrical – has rapidly gained momentum in recent years for a number of reasons, primarily due to its energy efficiency and environmental benefits. There has been considerable development in applications utilising piezoelectric innovations, alongside advances in ultra low power electronics, meaning energy harvesting is no longer viewed as being a potentially unreliable source of energy transfer, capable of only low power output. While alternative energy harvesting technologies are available, such as thermoelectric or electromagnetic energy, some have a reputation for unreliability and are not always capable of providing the consistent source of energy needed. **Fred Pimparel, Technical Manager, Morgan Technical Ceramics, Stourport, UK**

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some have a reputation for unreliability and are not always capable of providing the consistent source of energy needed. Fred Pimparel, Technical Manager, Morgan Technical Ceramics, Stourport, UK

Piezoelectric energy can be harvested by converting mechanical vibrations into an electrical charge, or by placing a material under significant strain through heavy pressure. These harvesters (Figure 1) generate electricity based on the amount of force used in compressing or deforming a material, as well as the amount and type of deformation on the material's crystal structure and the speed or frequency of compressions or vibrations to the material

(Figure 2). The potential for piezoelectric energy harvesting is therefore much greater than alternative energy harvesting technologies, with the components capable of delivering up to 70 % of their charge.

Huge market opportunities

In terms of market opportunities in the future, independent research from IDTechEx found that the energy harvesting market is expected to grow from £450 million in 2012 to more than £950 million by 2017 [1]. Tests are already being carried out for piezoelectric energy harvesters to be used in an extensive variety of

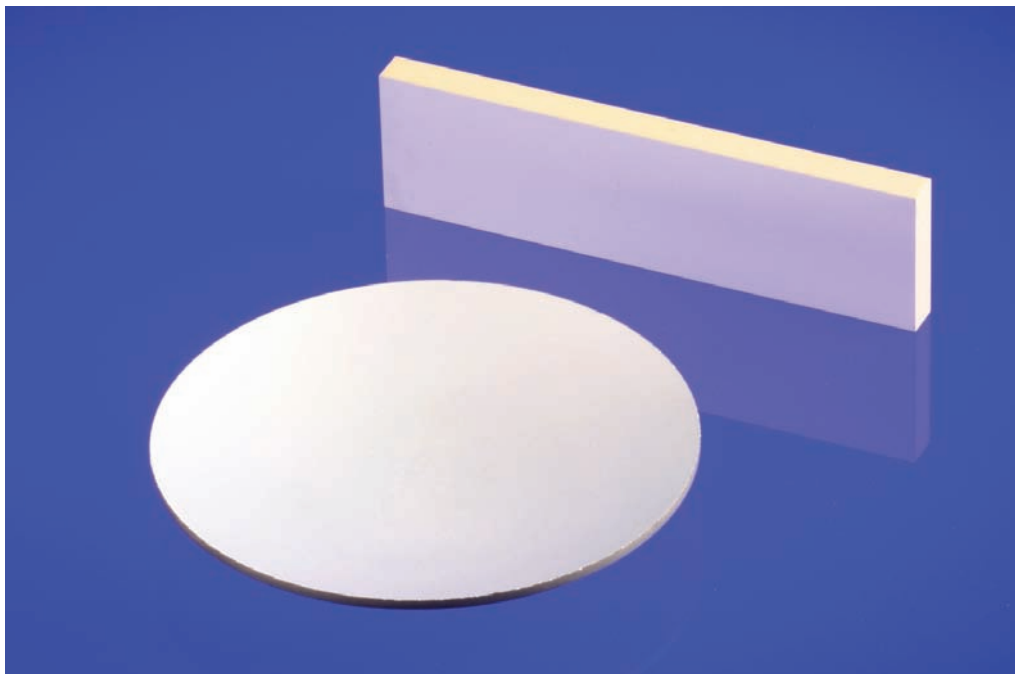


Figure 1: Pressure harvesters generate electricity based on the amount of force used in compressing or deforming a material

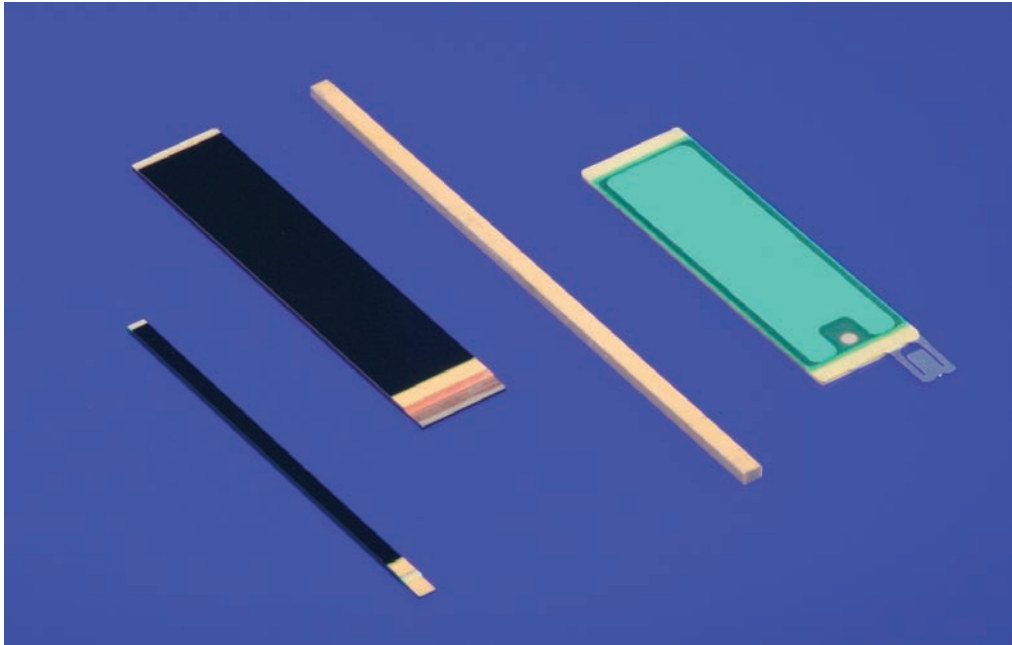


Figure 2: Example of vibration harvesters

applications. For instance, modules can be installed on roads or rail networks that react to heavy vehicles passing overhead, to generate energy that can be used to power LED lighting in signs or traffic lights. Industrial applications undoubtedly represent the biggest opportunity for piezoelectric energy harvesters, with electrical charge harnessed from vibrations in an engine shaft being just one key example. Industrial environments, such as oil and gas and manufacturing, will find energy harvesting a cost-effective alternative to wired infrastructure, which can be expensive. One of the greatest future challenges for piezoelectric energy harvesting is the ability to convert energy from broadband frequencies, harnessing a number of different sources of vibrations at various frequencies to produce a consistent supply of electric charge.

Choice of materials

The piezoelectric effect was discovered by Jacques and Pierre Curie in 1880. The French brothers learned that by subjecting certain crystals to mechanical strain, they became electrically polarized, with the degree of polarization proportional to the applied strain. The Curies also realized that these same materials deformed when exposed to an electrical field, which is now known as the inverse piezoelectric effect.

While quartz and ferroelectric crystals, such as tourmaline and Rochelle salt, are good examples of piezoelectric materials, ceramic lead zirconate titanate – more commonly known as PZT – is the most widely-used piezoelectric material used for energy harvesting. A key advantage of PZT materials is that they can be optimized to suit specific applications through their ability to be manufactured in any shape or

size. Furthermore, PZT materials are resilient, chemically inert and resistant to high temperatures and other atmospheric pressures – all key benefits considering the greatest opportunity for piezoelectric energy harvesting is in industrial applications. PZT products can be deformed repeatedly to generate energy and power devices, with typical applications being sensors and industrial equipment.

But how do piezoelectric ceramic materials generate power through the conversion of mechanical energy into electrical? The smallest of deformations can produce a measurable charge. As a result, a PZT cylinder can generate voltages that are high enough to draw a spark across an electrode gap. The energy created can then be stored in a capacitor and used to power a circuit or another application. However, there are a range of factors which govern the performance of any power generated in this way, including the shape of the PZT transducer, the style in which the transducer has been installed and the nature of the electrical load.

For instance, a PZT disc that is compressed between two metal surfaces will never be able to expand as readily as a long, narrow PZT cylinder, which is only constrained at its flat top and bottom ends, resulting in greater potential for the straight parallel sides to expand. Essentially, it is important to allow the material some freedom to expand radially, since energy generation is directly proportional to deformation. If the force that can be applied is limited, then the energy converted can be optimized by ensuring it is applied to a particular area where the material has the freedom to expand outwardly.

Another important consideration is the

impedance – the measure of opposition to the flow of an alternating current – of the load. When the current is created, it is important to match the electrical impedance of the piezoelectric component to the electronic recovery system, in order to maximize the energy transfer to the reservoir capacitor. The charge must be allowed to flow away quickly, otherwise the electrical field generated will tend to dissipate through the electronic components. As a result, applications subjected to a heavy pressure must be exposed to a fast 'impulse' to ensure the charge does not dissipate quickly. Furthermore, the choice and design of the electronic recovery circuit is of equal importance. It is essential to carefully consider components to minimize leakage currents and increase energy transfer efficiency.

Conclusion

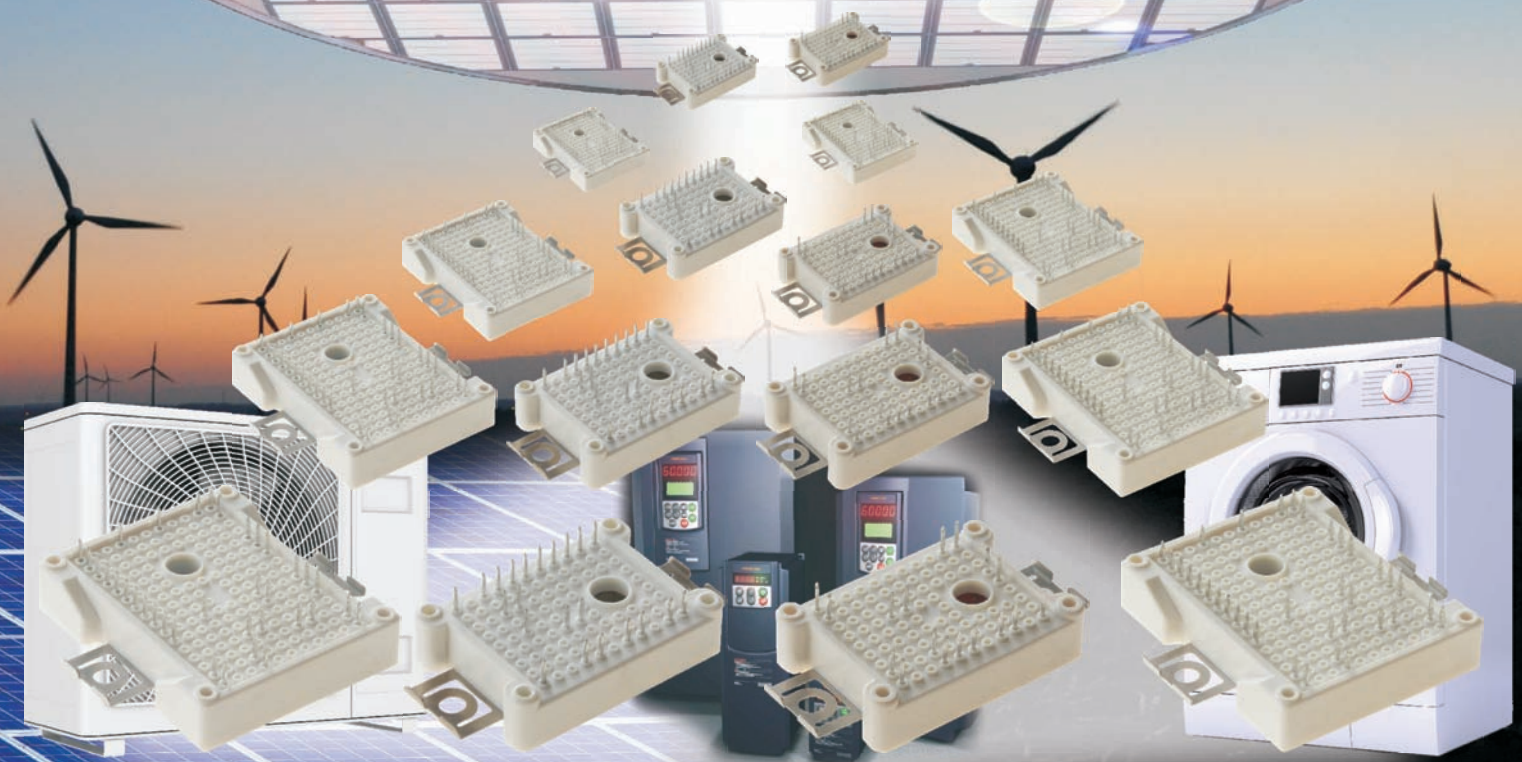
The advantages to piezoelectric energy harvesters are numerous. The process offers some of the highest efficiencies and power outputs by size and cost, and is therefore extremely appealing to those in search of an effective, high-performance solution. The environmental benefit is to substitute batteries and other means of charging, and their associated replacement costs, rather than solely focusing on saving energy.

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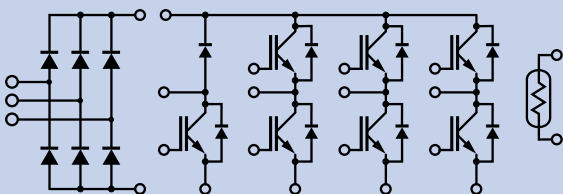
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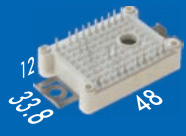

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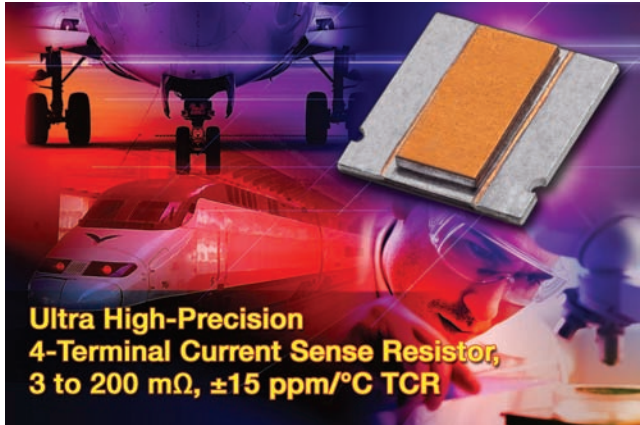
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Four-Terminal Current Sense Resistor

Current sense resistors are core passive components in analog circuits for demanding power applications. The devices measure the voltage drop across a resistive element created by the current through that element. In doing this, there are five issues commonly associated with inaccurate measurement: connection errors, external and internal temperature errors, frequency, load-life stability, and thermal EMF. Vishay's CSM3637P is designed to address all of these issues. The CSM3637P offers low TCR of ± 15 ppm/K from 3 m Ω to 100 m Ω and ± 25 ppm/K from 100 m Ω to 200 m Ω , and excellent frequency response to 50 MHz. The device's low TCR reduces errors



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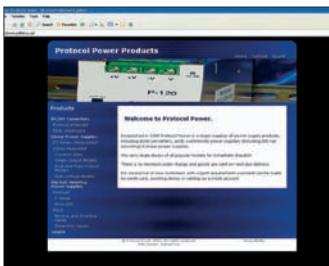
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Micrel introduces the MIC4604, a 85V Half Bridge MOSFET driver that features an integrated 85 V Bootstrap diode and programmable gate drive (5.5 to 16 V). These features make the MIC4604 a solution for battery operated motor applications including power tools and power DC/AC inverters. As an example, in battery powered motor drive applications, there is no need to boost the voltage to exceed the typical minimal gate drive of 9 V offered by other solutions; the MIC4604 allows operation from supplies as low as 5.5 V. In addition, the 85 V operating voltage offers plenty of margin which protects against voltage spikes that are present in motor drive and power supply applications, making the device suited for low voltage and high voltage applications. The MOSFET driver features 39 ns propagation delay and 20 ns driver rise/fall times for a 1 nF capacitive load. The low-side and high-side gate drivers are independently controlled. The MIC4604 also offers TTL input thresholds and includes a high-voltage internal diode that helps charge the high-side gate drive bootstrap capacitor. A robust, high-speed, and low-power level shifter provides clean level transitions to the high-side output. The MIC4604 is available in an 8-pin SOIC package and tiny 10-pin 2.5 mm x 2.5 mm TDFN package options. Both packages have an operating junction temperature range of -40°C to +125°C.

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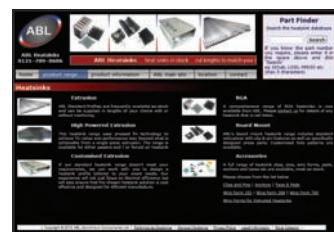
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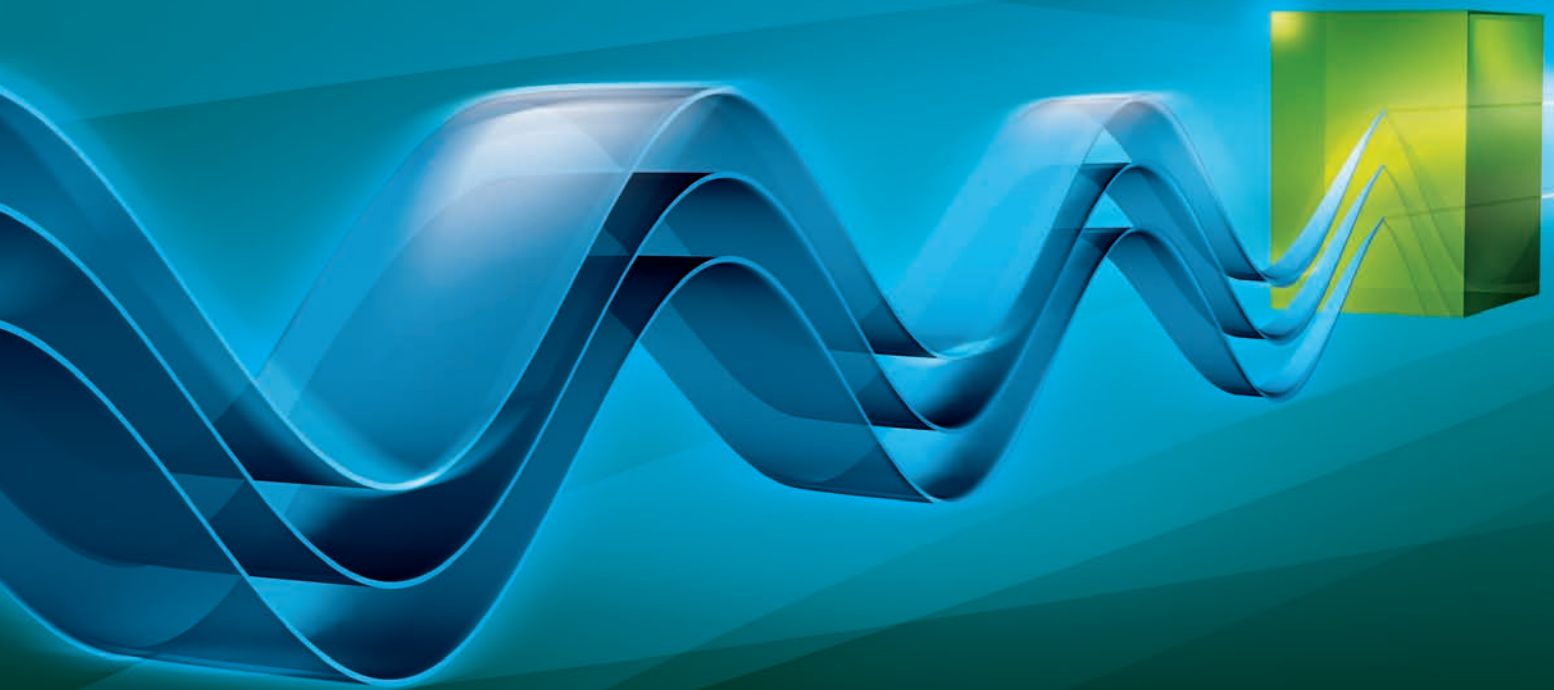
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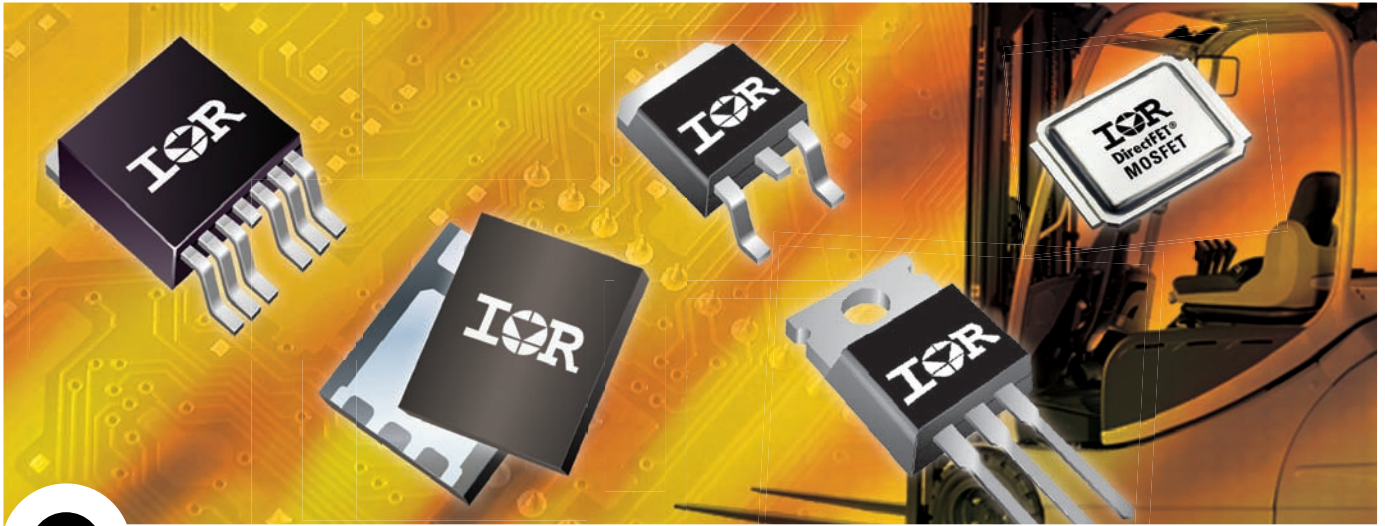
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