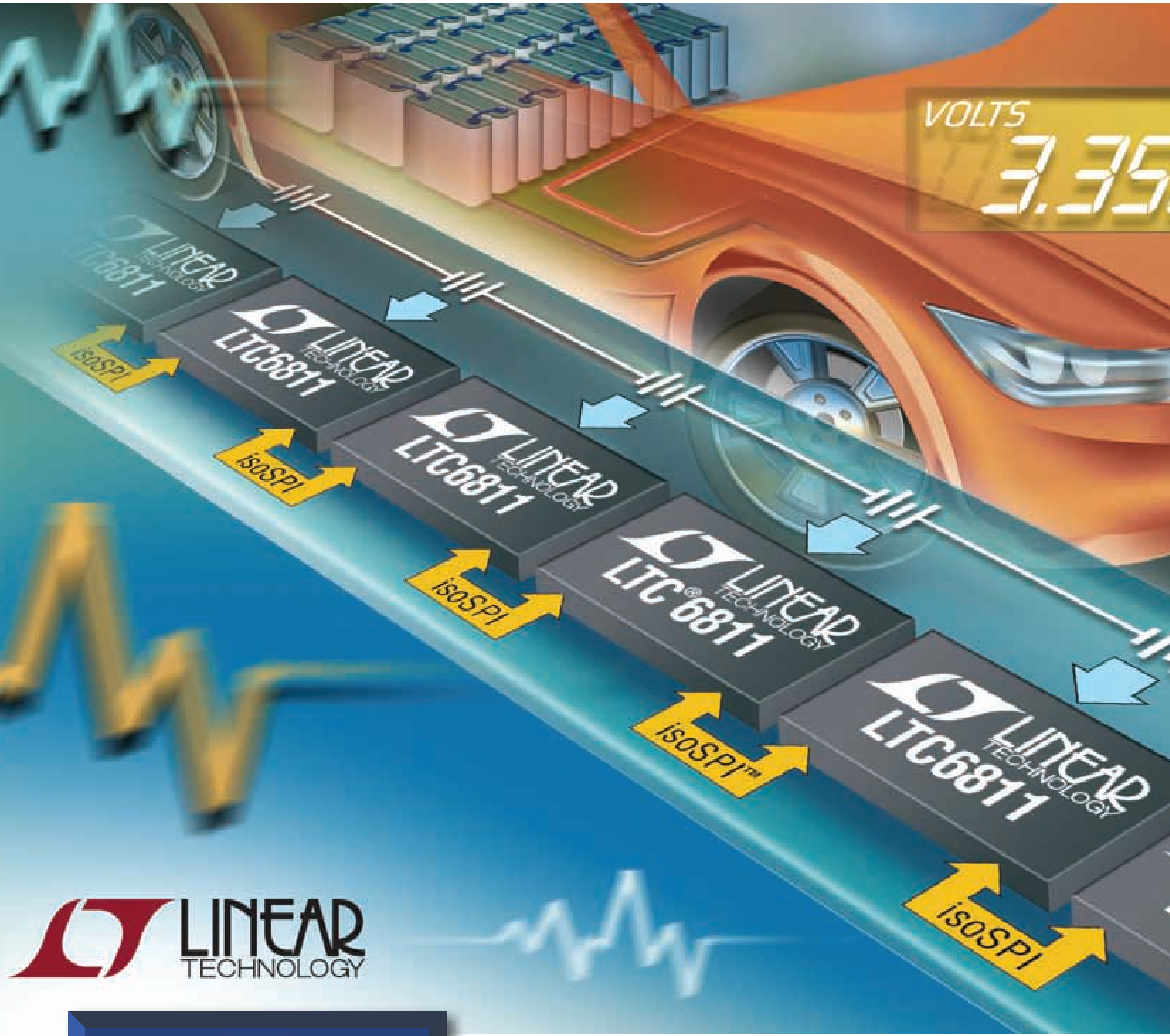
POWER ELECTRONICS EUROPE

ISSUE 1 – Feb/March 2016 www.power-mag.com

BATTERY MANAGEMENT

Maximizing Cell Monitoring Accuracy and Data Integrity



THE EUROPEAN JOURNAL FOR POWER ELECTRONICS AND TECHNOLOGY

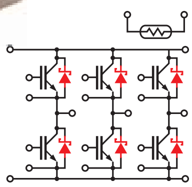
Also inside this issue

Hybrid IGBT Modules

Si-IGBT with SiC-Schottky diode

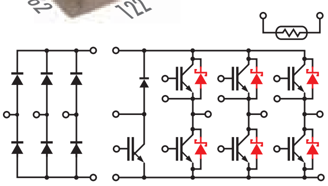
- Higher efficiency
- Higher output current
- Suitable for high switching frequencies
- Significant lower reverse recovery and turn-on losses

6-Pack



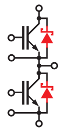
I_c	600 V	1200 V
100A		●

PIM



I_c	600 V	1200 V
35A		●
50A	●	●
75A	●	
100A	●	

2-Pack



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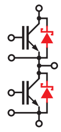
200A	●	
300A	●	
450A	●	



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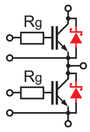
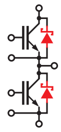
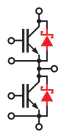
400A		●



I_c	1200 V	1700 V
550A		●
600A	●	

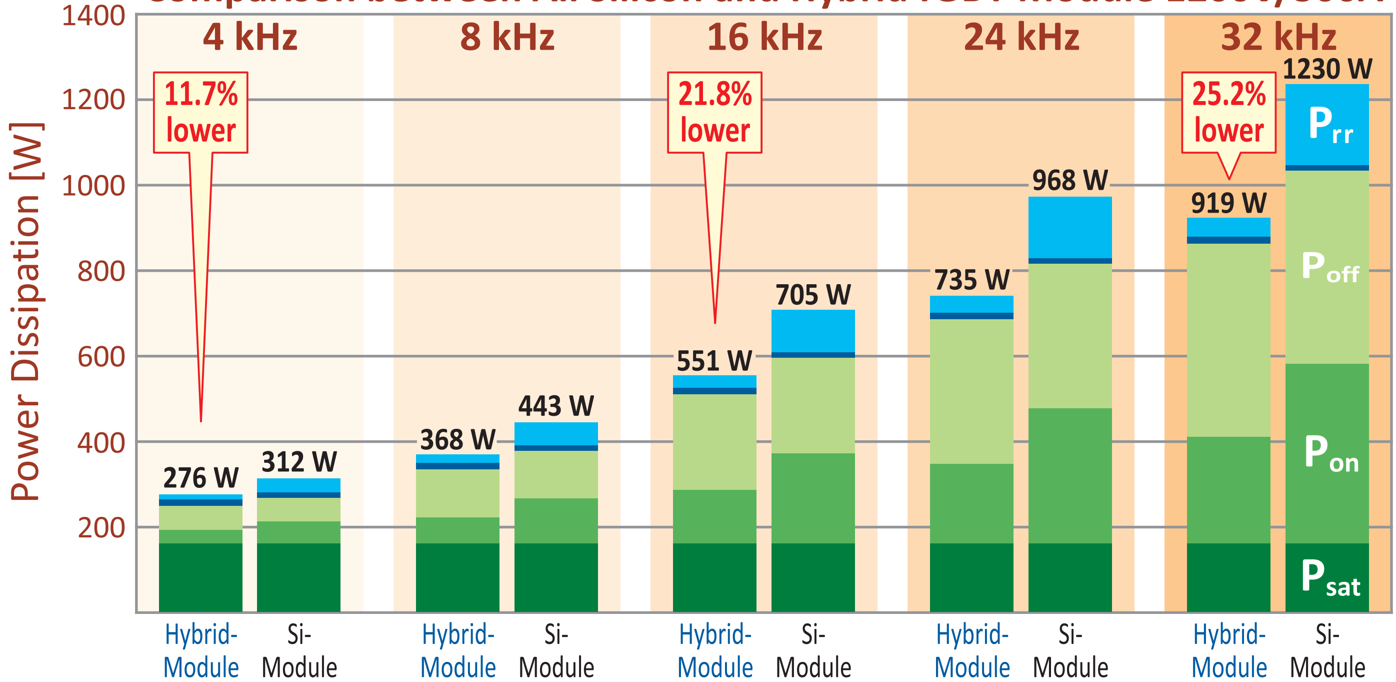


I_c	1200 V	1700 V
1200A		●



I_c	1200 V	1700 V
1000A		●
1400A	●	●

Comparison between All Silicon and Hybrid IGBT Module 1200V/300A



Conditions: 3 arms PWM • V_{CC} = 600 V • I_O = 212 A_{rms} • f_O = 50 Hz • cosφ = 0.9 • λ = 1.0

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Circulation and subscription: Power Electronics Europe is available for the following subscription charges. Power Electronics Europe: annual charge UK/NI £60, overseas $130, EUR 120; single copies UK/NI £10, overseas US$32, EUR 25.
Contact: DFA Media, 192 The High Street, Tonbridge, Kent TN9 1BE Great Britain.
Tel: +44 (0)1732 370340.
Fax: +44 (0)1732 360034. Refunds on cancelled subscriptions will only be provided at the Publisher's discretion, unless specifically guaranteed within the terms of subscription offer.

Editorial information should be sent to The Editor, Power Electronics Europe, PO Box 340131, 80098 Munich, Germany.

Printed by: Garnett Dickinson.

ISSN 1748-3530

The Power of GaN

In the early 1980's, the Silicon bipolar transistor was transformed into the mass production MOSFET. The 1990's saw the adoption of the IGBT, and the 2000's brought the superjunction MOSFET into volume. Now, an even more fundamental transition is underway as Silicon is overtaken by the introduction of SiC and GaN high performance, wide band-gap power products – according to a keynote speaker at APEC and PCIM 2016. The breakthrough performance of qualified products, with the subsequent application benefits of size and cost, is now fully appreciated by power system designers. As the 'eco-system' continues to mature, with new enabling topologies, control ICs and magnetic solutions, the transition will accelerate and transform the power electronics industry. According to market researcher Yole the power GaN market is expected to explode. The GaN-on-Si epi wafer market is still opened and many players are strongly competing. GaN-on-Si technology is very challenging.

To make GaN power electronics a commercial reality, it has to be cost competitive with Si-based power electronics. For this, GaN grown on 6" and 8" Si wafers is a must, as these wafer diameters allow to use conventional Si fabrication infrastructure. The growth of high quality GaN on Si is however very challenging, especially when trying to optimize the trade-off between breakdown voltage, GaN thickness, and current collapse. One of the major problems for GaN power devices is current-collapse phenomena, where the on-resistance is not recovered quickly after biasing the high-voltage stress. The phenomena become serious as increasing operation temperature and/or increasing breakdown voltage. This is caused by the deep-levels that decrease the carriers in the GaN material. At present, mainstream GaN power devices have a lateral structure. On the other hand, progress in vertical devices was slower than that for lateral devices because GaN substrates lacked quality for high voltage applications. However, GaN substrate can become applied to high breakdown voltage above 1kV, and the vertical devices have recently attracted additional research attention. The vertical structure has the advantages of current-collapse-free operation, small chip size, easy wiring and a high breakdown voltage. These characteristics are highly suited for high-power applications.

Long-term device reliability is critical for successful commercialization. A number of degradation mechanisms, such as inverse piezoelectric effect, peak electric field and hot electron damage, have been shown in the past to impact reliability. Among them, electrochemical oxidation plays a key role in inducing macroscopic defects and pits next to the gate electrode after long-term stress in the off-state. With proper passivation and field management, very stable devices have been achieved. But the main issues have been resolved and several companies have begun commercializing power devices.

During the past five years many power GaN devices have been launched by established companies such as International Rectifier (acquired by Infineon in late 2014), Panasonic, or start-ups such as EPC, GaN Systems, Transphorm and most recently Navitas Semiconductor. Recent 2015 and this year's conferences focuses more on power GaN applicatons. A monolithic GaN power IC 400 V / 200 W ZVS converter designed at HRL labs is projected to be able to switch at 100 MHz, with 50 times lower parasitic inductances by shrinking length of power loop 2.5 times and reducing distance between inductance canceling currents by 50 x. The GaN-on-insulator power IC is directly attached to a heat sink. The GaN-on-insulator power IC will have lower parasitic CDS and no substrate biasing. Interleaving converters will reduce current ripple and allow scaling to higher power. The 100 MHz GaN power IC converter should weigh 10 x less and consequently cost less than today's 100 kHz converters. Fully-monolithic GaN-on-Si half-bridges with integrated reverse-diodes have been designed at Fraunhofer Institute for Applied Solid State Physics (IAF) in Germany. The high- and low-side switches feature an off-state voltage of 600 V, an on-state resistance of 120 mOhm, and a reverse resistance of below 150 mOhm at corresponding drain currents of 30 A. This design will be demonstrated at PCIM. Decreased commutation times requires much reduced inductances inside power modules. French Dtalents proposes an optimal geometry of strip line layout everywhere inside the power module. Return conductors are made of copper foils mounted face to face in front of chips boundings. Increased width of conductors, and decreased thickness of insulation, leads to an inductance around only one Nano-Henry. And on the magnetic side a new ferrite material for GaN Resonant Transformers has been developed at SUMIDA Components & Modules. The rapid progress in GaN power semiconductors will lead to a further miniaturization of power electronic assemblies and subsystems. Inductive components have a significant impact here. The drastically increased frequency requires improved ferrite materials with lowest losses and transformer designs with unique construction technologies. With a governmental funded project a new DC/DC resonant converter should operate up to 3 kVA at frequencies >> 1 MHz.

"As Silicon reaches its performance limitations, other new entrants are delivering significantly greater performance with rapidly decreasing costs and hundreds of new applications in mainstream markets. Independent GaN companies will set the pace while established power Silicon producers will downplay the significance of the technology", predicts in his 2016 outlook Alex Lidow, EPC's CEO. Time will tell whether he is right.

More on GaN and other interesting power electronic topics on the following pages.

Achim Scharf
PEE Editor

WBG Technologies Open The Way To New Markets

0 million in 2020. "Driven by the SiC-based power devices market, the n-type SiC substrates market will grow from around $35 million2014 to $110 million in 2020, with a 21% CAGR", expects Dr Hong Lin, Technology & Market Analyst at Yole. 4" wafers are still preferred for power electronic applications. However, some suppliers are now able to provide bigger wafers with good enough quality for power devices - an 8" SiC wafer was demonstrated by II-VI in 2015.

The average price for 6" is still 2.25x higher than 4". However the price continues to decrease and will drop below the threshold in early 2016. The transition to 6" is beginning; in fact, ROHM announced already mass production on 6" wafers.

The n-type SiC substrate market player rankings have stabilized of late. Cree remains the market leader; then follow Dow Corning, SiCrystal (a ROHM company), and II-VI right behind.

Yole analysts identify now four Chinese SiC suppliers. "Their current announced capacity is more than 150,000 wafers per year, with further increases expected", asserted Hong. Moreover, in early 2015, TankeBlue demonstrated a 6'' n-type wafer. Thus the Chinese players should be considered as serious market challengers.

In parallel, power GaN is expected to explode: The GaN-on-Si epiwafer market is still opened and many players are strongly competing. GaN-on-Si technology is very challenging due to large lattice and the thermal coefficient expansion (CTE) mismatch of between Gallium Nitride and Silicon. That said, GaN-on-Si's main issues have been resolved and several companies have begun commercializing power devices based on this technology. Attracted by the device market's potential, players with different origins are active on the GaN-on-Si epiwafer open market and thinking of selling epiwafers to device players.

These players are Silicon substrate suppliers wanting to move up the value chain, for example Siltronic, device foundries like Episil that want to move down the value chain, some LED chip suppliers (for example San'an), large epi houses such as IQE, Epigan and other pure GaN epi houses. Hong comments: "The power GaN device business is only in early stages, the related GaN epiwafer open market is not yet well-established. Competition is very intense; Azzurro's 2014 bankruptcy has illustrated the risks faced by start-up GaN epi houses."

www.yole.fr

	2014	2015	2016	2017	2018	2019	2020
SiC wafer market size (M$)	35	48	56	68	80	93	110

EpiGaN and SunEdison Serve GaN-on-Si Globally

EpiGaN, a European supplier of commercial-grade 6- and 8-inch GaN-on-Silicon epi-wafers for 600-V HEMT (High Electron Mobility Transistor) power semiconductors, and SunEdison Semiconductor, a manufacturer of Silicon substrates for semiconductor manufacturing, have signed a global representation agreement for EpiGaN' epi wafers.

EpiGaN, located in Hasselt, Belgium, offers a portfolio covering power switching applications up to 650 V as well as RF power devices for millimeter-wave applications. EpiGaN is today developing and sampling GaN structures on 200 mm Si substrates for power switching devices. A key concept of EpiGaN's technology base is the in-situ SiN cap layer, which provides high passivation properties and device reliability. The use of in-situ SiN allows the use of pure AlN layers as barrier material with the resulting heterostructures having sheet resistance values below 300 Ohm/sq.

Combining EpiGaN's technology with SunEdison Semiconductor's market presence and expertise opens a new one-stop solution for IDMs active in next-generation GaN power technology on Si substrates. EpiGaN was formed in 2010 as a spin-off of Belgian micro and nano-tech research organization imec.

www.epigan.com, www.sunedisonsemi.com

Alex Lidow Receives 2015 SEMI Award on GaN

EPC's CEO Alex Lidow was selected as the recipient of the 2015 SEMI Award for North America for the innovation of power device technology, enabling the commercialization of GaN. Dr. Lidow was honored for his work in the area of Process and Technology Integration. Established in 1979, the SEMI Award was designed to recognize significant technological contributions to the semiconductor industry and to demonstrate the industry's high esteem for the individuals or teams responsible for those contributions.

Gallium Nitride (GaN) transistors and ICs offer faster and more power-efficient products compared with those made from Silicon. The use of GaN enables entirely new technologies and the advancement of existing technologies in a variety of areas, including 4G and 5G wireless communications, wireless charging, augmented reality glasses, autonomous vehicles and wireless medical technology, to name a few. "Semiconductors fuel innovation, creating the backbone of technology advancement and subsequently, the economy at large," commented Lidow. "It has been my driving passion to save energy by developing more efficient semiconductors. The team at EPC has delivered first off-the-shelf enhancement-mode GaN transistors and ICs and will continue to partner with our customers to use GaN to change the way we live."

www.epc-co.com ¶

Alex Lidow at PEE's GaN panel discussion PCIM 2015 showing GaN application PCBs

Cubic GaN LEDs

Plessey, Anvil Semiconductors and the University of Cambridge (UK) are working together to fabricate high efficiency LEDs in cubic GaN grown on Anvil's 3C-SiC / Si substrates.

Cubic GaN has the potential to overcome the problems cause in conventional LEDs by the strong internal electric fields which impair carrier recombination and contribute to efficiency droop. This is particularly true for green LEDs where the internal electric fields are stronger and are believed to cause a rapid reduction in efficiency at green wavelengths known as "the green gap". The availability of cubic GaN from a readily commercializable process on large diameter Silicon wafers is as a key enabler for increasing the efficiency of green LEDs and reducing the cost of LED lighting.

The collaboration, which is partly funded by Innovate UK under the £14 million Energy Catalyst Program, follows on from work by Anvil Semiconductors and the Cambridge Centre for GaN where they successfully grew cubic GaN on 3C-SiC on Silicon wafers by MOCVD. The underlying 3C-SiC layers were produced by Anvil using its patented stress relief IP that enables growth of device quality SiC on 100 mm diameter Silicon wafers. The process is readily migrated onto 150 mm wafers and potentially beyond without modification and is therefore suitable for large, industrial-scale applications. Plessey have started to commercialize LEDs produced in conventional (hexagonal) GaN grown 150 mm silicon wafers using IP originally developed at the University of Cambridge. Anvil's 3C-SiC on Silicon technology, which is being developed for SiC power devices, provides an effective substrate, to allow single phase cubic GaN epitaxy growth and provides a process which is compatible with Plessey's GaN on Si device technology. "The properties of Cubic GaN have been explored before, but the challenges of growing this thermodynamically unstable crystal structure have limited its development. The high quality of Anvil's cubic SiC on Si substrates and our experience of developing conventional GaN LED structures on large area wafers have enabled a breakthrough in material quality", Prof. Colin Humphreys, Director of the Cambridge Centre for GaN commented.

www.plesseysemiconductors.com, www.anvil-semi.co.uk,

StarPower Strengthens its Sales Team

StarPower Europe AG, the European subsidiary of the Chinese power semiconductor manufacturer StarPower Semiconductor Ltd., is strengthening its technical sales with the power semiconductor expert Rickmer Heubeck-Wex.

Heubeck-Wex has been working within the power semiconductor market for many years, he was previously employed as Product Manager, Key Account Manager and Head of National Sales at Semikron for 16 years in the division of semiconductor modules and systems. "The recruiting of additional personnel for the sales team with an experienced power electronics specialist is an important step on our path to expanding the company's market presence in Europe, in order to meet the increasing demand for quality semiconductors in the IGBT and bipolar module division," said Managing Director Peter Frey. In the past fiscal year, StarPower achieved a record turnover of $70 million with 350 employees. StarPower offers standard IGBT modules in 600, 1200 and 1700 V, as well as MOSFET and bipolar modules. All common circuits, such as half-bridges, 6 and 7 packs, IPMs, 3 and 5-level modules, are produced in various packages and performance classes.

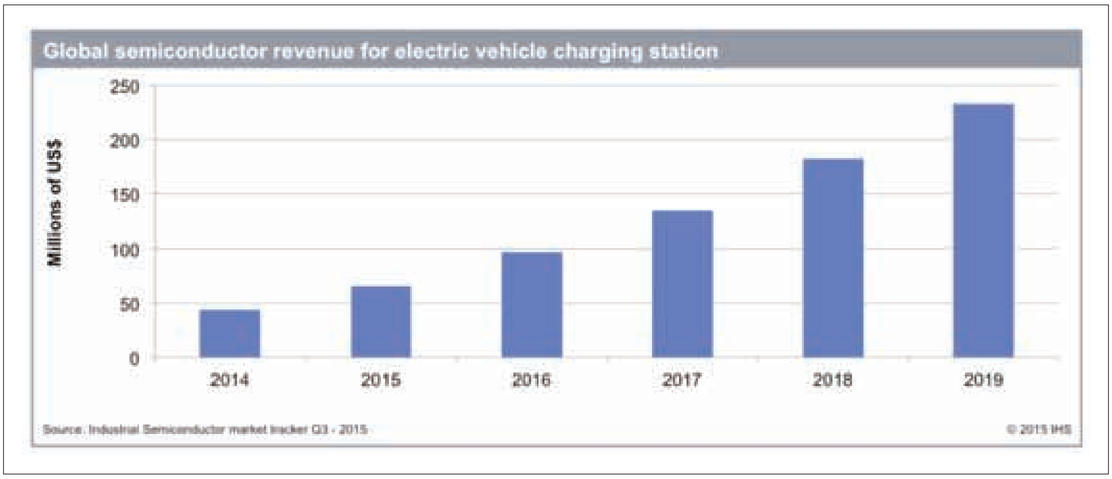
www.starpowereurope.com

Strong Semiconductor Growth Forecast for Electric Vehicle DC Fast-Charging Stations

The global market for semiconductors used in electric vehicle (EV) charging stations for plug-in hybrid (PH) and battery electric vehicles (BEV) will continue to expand in the coming years, providing significant growth opportunities to semiconductor manufacturers.

Revenue from semiconductors used in EV charging stations reached $44 million in 2014 and is expected to grow at a compound annual growth rate (CAGR) of 39 percent to reach $233 million in 2019, according to market researcher IHS. "Fast charging is a necessary step to the strong adoption of EVs and a higher power rating is required to support these shorter charging times," said analyst Noman Akhtar. "Electric vehicle charging stations with higher ratings require more power semiconductors, especially discrete semiconductor components, which will lead to increased semiconductor revenue growth."

In 2014, the average price for semiconductor components in a level-two charging station – which could charge a battery in about five hours – was $143. By comparison, semiconductor components used in the latest fast-charging direct-current (DC) chargers now cost more than $1,000; however, they are capable of charging a vehicle battery to 80 % of capacity in just 15 minutes. Average selling prices of semiconductors used in communication modules are expected to increase over time, as the industry moves toward single system-on-chip (SoC) solutions that not only provide faster control, but also include the memory required for secure communications and other applications. "Better communication between the utility and the charger improves the stability of the electric grid," Akhtar said. "The latest developments in communication interface ICs enable more secure and reliable information transfer."



www.ihs.com

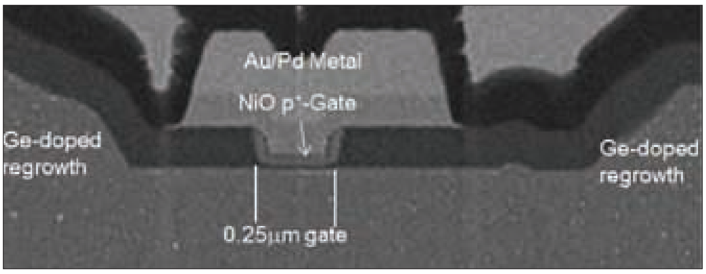
Power GaN in Research

The 61st annual IEEE International Electron Devices Meeting (IEDM) was held in December 2015 in Washington DC. Back by popular demand for the third year, the 2015 IEDM featured a slate of designated focus sessions on topics of special interest such as Beyond von Neumann Computing, Layered 2D Materials and Devices, Flexible Hybrid Electronics, Silicon-based Nano-devices for Detection of Biomolecules and Cell Function, and Advances in Wide Bandgap Power Devices – which are our main focus.

To make GaN power electronics a commercial reality, it has to be cost competitive with Si-based power electronics. For this, GaN grown on 6" and 8" Si wafers is a must, as these wafer diameters allow to use conventional Si fabrication infrastructure. The growth of high quality GaN on Si is however very challenging, especially when trying to optimize the trade-off between breakdown voltage, GaN thickness, and current collapse.

Long-term device reliability is critical for successful commercialization. A number of degradation mechanisms, such as inverse piezoelectric effect, peak electric field and hot electron damage, have been shown in the past to impact reliability. Among them, electrochemical oxidation plays a key role in inducing macroscopic defects and pits next to the gate electrode after long-term stress in the off-state. With proper passivation and field management, very stable devices have been achieved.

In spite of the excellent performance of lateral GaN devices, theoretical considerations indicate that vertical GaN transistors offer the ultimate power density management capability. This is due to a much more uniform heat generation, thanks to the vertical current path in these devices. Unfortunately,



SEM cross-section of 0.25 µm gate normally-off GaN FET fabricated with Ge-doped re-growth technique achieving $R_{on}W_g$ of 0.95 Ωmm

the bulk GaN substrates traditionally used for GaN vertical devices are expensive and their small diameter precludes the use of state-of-the-art Si fabs for device fabrication, which further increases the device cost.

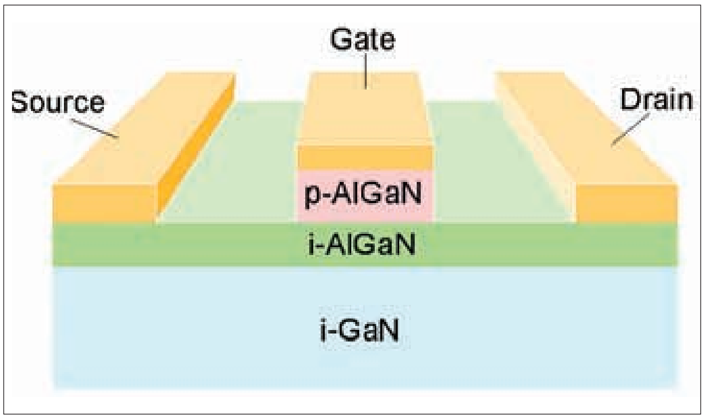
At US MIT a new generation of vertical GaN devices on Si substrates are under development to take advantage of the high power density of vertical devices, at the cost-point of Silicon. One of the main challenges for these devices is the high off-state leakage current. The leakage through the GaN sidewall was found to dominate our first generation of GaN vertical diodes. Once that this sidewall was passivated with a novel plasma-based surface treatment, vertical GaN power diodes on Silicon were fabricated with better off-state leakage current levels than lateral devices. This opens a path towards the use of these new vertical devices in commercial applications.

Renovation of Power Devices by GaN-based Materials

This was the title of the presentation by Daisuke Ueda from Kyoto Institute of Technology in Japan. Si trench MOSFETs have been widely used in the low-voltage applications since the structure enables to reduce on-resistance (R_{on}) by increasing the gate-width (W_g). R_{on} is the sum of channel-resistance (R_{ch}) and drift-region-resistance (R_d). Most effective to reduce R_{on} is scaling-down in the low-voltage range. For example, a 100 nm GaN FET is sufficient to be used in typical 12 V DC power-supplies, while Si MOSFET needs 500 nm spacing, thus we can drastically reduce the chip size in designing GaN power IC in the low-voltage range.

Scalability is significant advantage of wide bandgap device. One of the problems in miniaturizing GaN FET is the increase of contact resistance in source/drain regions. Recently, a new technology was developed to reduce the contact resistance by heavily Ge-doped re-growth. One order of magnitude higher carrier concentration was obtained in Ge-doped regrowth layer resulting in the significant reduction of contact-resistance.

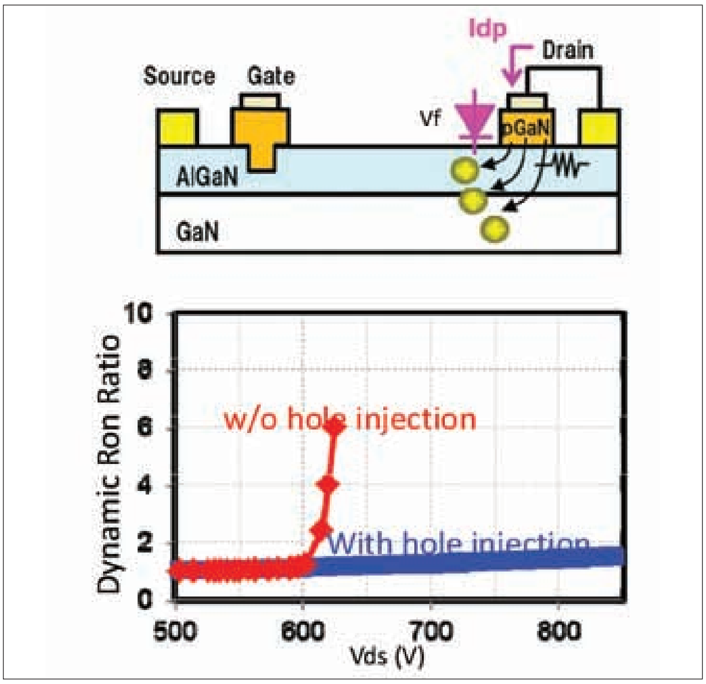
The normally-off GaN transistor named GIT (Gate Injection Transistor) from Panasonic, where holes are injected from the gate, enable high switching-



Normally-off GaN transistor named GIT (Gate Injection Transistor) where AlGaN gate is used to prevent reverse injection

speed with conductivity modulation. Though the life-time of the injected carrier is thought to be short because of direct recombination and defect-based recombination process inside the GaN material. Short life-time of minority carrier reduces the effect of conductivity modulation. Experimentally fabricated GIT shows strong dependency of switching time on the operation current. This phenomenon can be explained by the suppressed recombination owing to the spatially separated holes and electrons in the drift region due to inherent polarization.

One of the major problems for GaN power devices is current-collapse



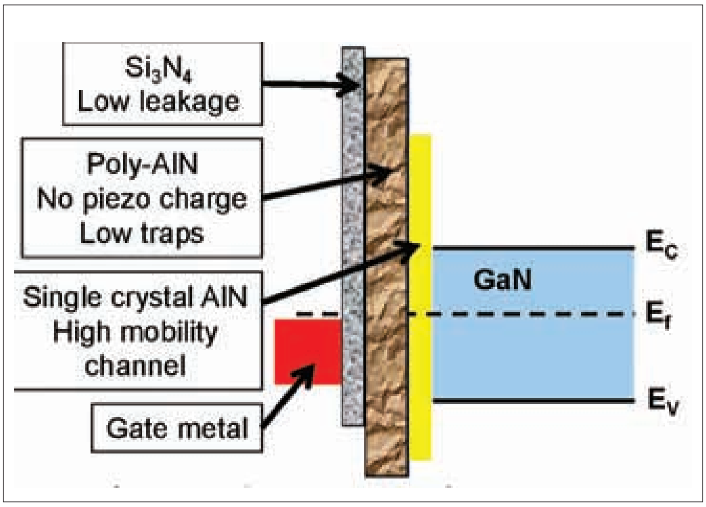
New GIT provided with hole-injector at the anode region like IGBT and measured current-collapse behavior with and without anode-injector

phenomena, where Ron is not recovered quickly after biasing the high-voltage stress. The phenomena become serious as increasing operation temperature and/or increasing breakdown voltage. This is caused by the deep-levels that decrease the carriers in the GaN material. A recently developed GIT with p+-anode with IGBT-like structure completely eliminates the current-collapse due to the trap-filling process by the injected carriers. This suggests introducing conductivity modulation is effective in future vertical GaN power device to widen the applications toward the application layer of infrastructure.

Increasing the Switching Frequency of GaN HFET Converters

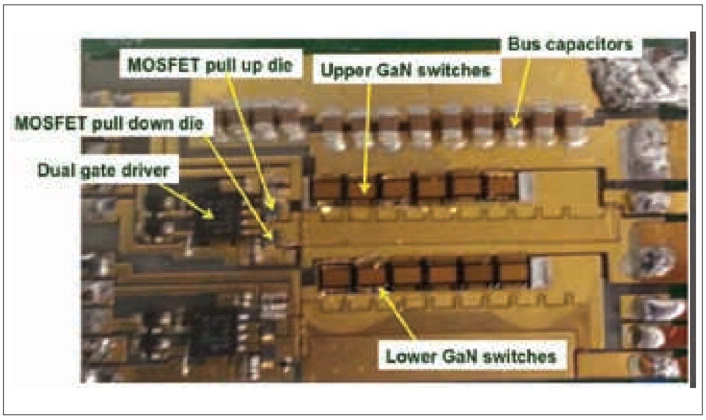
The GaN switches need short gate length to reduce channel resistance, low gate leakage for reliability, and e-mode for safe operation. D-mode GaN HFETs employ vertical ~ 30V Si MOSFETs in cascode for effective e-mode switches, but this approach is not suitable for GaN ICs. HRL's (**www.hrl.com**) approach for an e-mode GaN switch is a native insulator, similar to Si02 on Si. The AlN-based gate has low IV hysteresis and gate leakage current of 2 nA/mm at 600 V. The channel has a mobility of 1000 cm^2/V-s.

Faster switching reduces switching loss of converter. Increasing the frequency an efficient converter requires proportional decreases of parasitic



HRL's e-mode GaN HFET insulating gate structure illustrating key features

inductances in power loop and gate drive. To achieve efficient switching at 1MHz, HRL employed a hybrid GaN IC on 250μm AlN substrates. The loop size was reduced by employing bare die, and a vertical current loop to cancel most of the inductance. Integrated bare Si die gate driver reduces drive resistance to 50 mΩ and gate inductance to <1nH. During the high dV/dt of 325 V/ns switching the drain voltage overshoot was 200 V and the gate overshoot was more than 2 V, exceeding the device ratings. Critically damping the gate drive turn-on reduced drain overshoot to less than 20 V and gate



GaN HFET hybrid IC half bridge circuit, with vertical power loop to reduce inductance

overshoot to less than 1 V, however it slowed switching speed. The hard-switched 1MHz boost converter efficiency was 96 %.

A monolithic GaN power IC 400 V / 200 W ZVS converter is projected to be able to switch at 100 MHz, with 50 times lower parasitic inductances by shrinking length of power loop 2.5 times and reducing distance between inductance canceling currents by 50 x. The GaN-on-insulator power IC is directly attached to a heat sink. The GaN-on-insulator power IC will have lower parasitic CDS and no substrate biasing. Interleaving converters will reduce current ripple and allow scaling to higher power. The 100 MHz GaN power IC converter should weigh 10 x less and consequently cost less than today's 100 kHz converters.

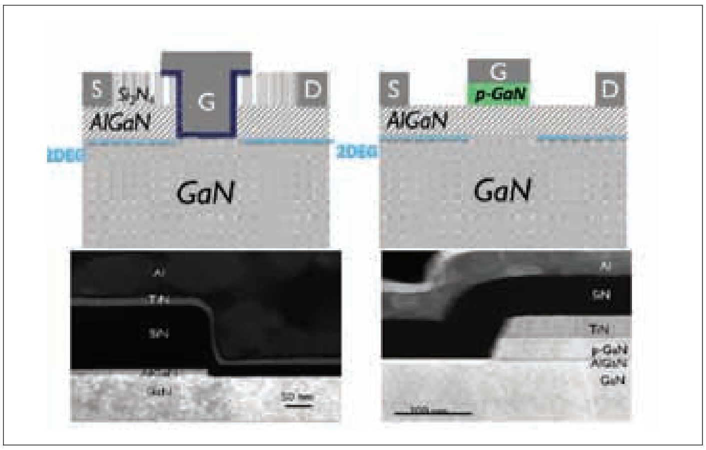
200 mm GaN-on-Si epitaxy

Development of GaN-on-Si e-mode technology for high power applications requires high voltage buffers and suitable device architectures to enable normally-off operation. Furthermore, the thermal and lattice mismatch between GaN and Si limit its scalability to larger areas (200mm and beyond). Wafer bow and morphological challenges needs to overcome, as explained by Denis Marcon from Belgium-based research lab imec (**www.imec.be**).

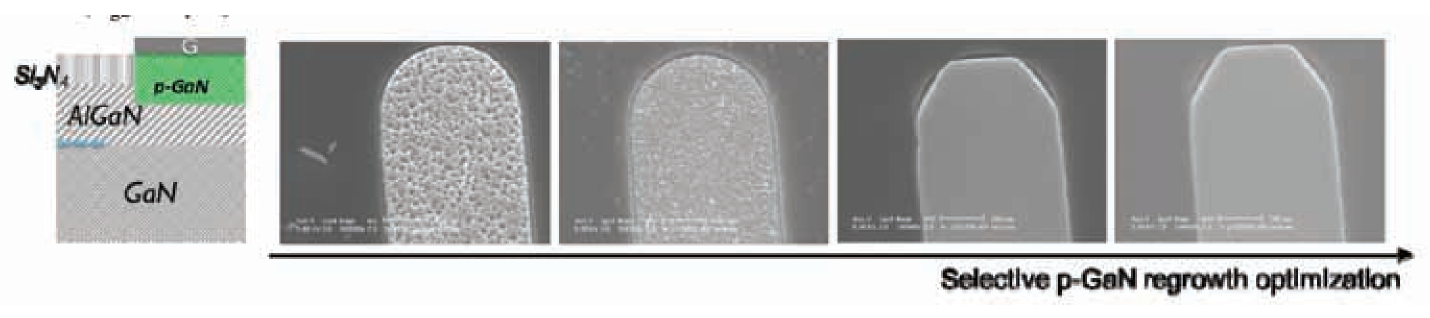
The continued research on GaN e-mode devices has converged gradually towards two competing device architectures for e-mode - recessed gate MISHEMT and p-GaN HEMT. Recessed gate MISHEMTs are obtained by fully recessing the AlGaN barrier to locally interrupt the 2DEG. Imec performed the full recess of the barrier as it minimizes non-uniformities over the 200 mm wafer. The challenges related to this architecture are the difficulties to obtain devices with a Vth above 1.5 V combined with on-resistance below 10 Ω·mm, and low PBTI (Positive Bias Thermal Instability). Different gate dielectrics have been tried, such as PEALD Si_3N_4 or ALD Al_2O_3. A higher V_{th} is obtained with an optimized PEALD Si_3N_4, however with too high hysteresis. A lower hysteresis and a 10 times improvement in terms of PBTI is obtained with an optimized ALD Al_2O_3 however, at the cost of a lower V_{th}. Further understanding of the role of bulk and interface charges in/at the gate dielectric are required.

Moreover, in high volume Au-free manufacturing, there are few options for further V_{th} increase by switching to electrode materials with higher work function (e.g. Ni/Au) and the tuning of threshold voltage through charges can result in Vth instabilities with temperature. Despite the use of an optimized gate dielectric, the electron mobility in the channel below the fully recessed gate is typically lower than for d-mode and p-GaN HEMTs, thus significantly contributing to R_{on}.

The p-GaN HEMT has better control over the gate region. The threshold voltage can be tuned by the thickness and doping of the p-GaN layer and by the barrier height of the electrode. P-GaN HEMT devices have very low hysteresis. The first challenge for the p-GaN HEMT device consists of controlling the Mg diffusion from the p-GaN layer into the access region and to avoid Mg deactivation during processing. With an optimization process Imec obtained e-mode devices with V_{th} larger than 2 V, R_{on} =7 Ω·mm and I_{dsat}

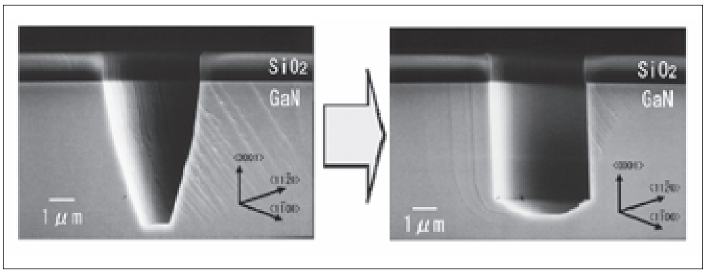


Schematic cross- section (upper part) and TEM of the gate region (lower part) of a recessed gate MISHEMT (left) and a p-GaN HEMT



Schematic cross-section (left) and first optimization tests of selective p-GaN re-growth

at 1 V > 0.4 A/mm. Forward gate leakage could represent a second challenge for this approach as it has been often reported to be quite high, thus representing a concern for reliability. However, it could be optimized to obtain less than 10 nA/mm at V_g =+12 V. The main processing challenge for this approach is the p-GaN etching, and surface restoration and passivation. This process impacts R_{on} scaling as a function of L_{gd} and can cause surface-related dispersion phenomena. In-situ MOCVD Si_3N_4 surface passivation for low dispersion could be combined with a p-GaN HEMT concept by performing a selective re-growth of the p-GaN layer in the gate area. First optimization experiments have shown that good quality p-GaN layer could be selectively re-grown, thus opening perspectives for this hybrid architecture that combines the best of two e-mode concepts.



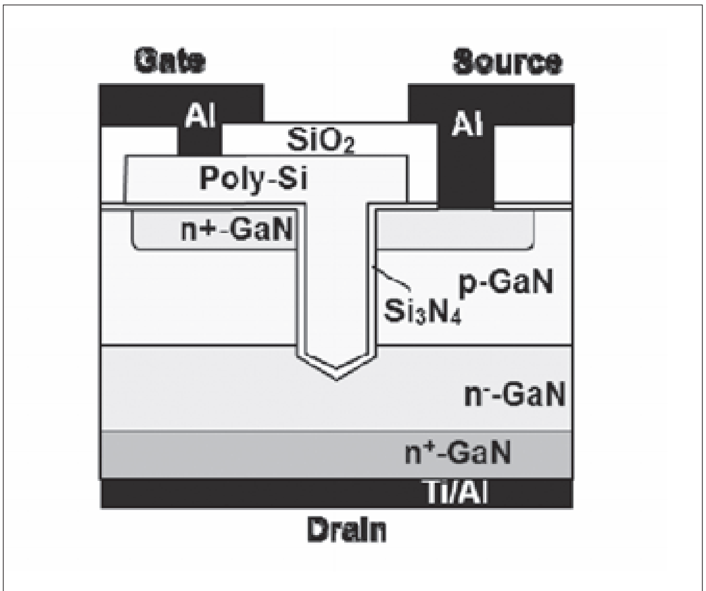
Fabrication process of the GaN trench - first step after ICP dry etching (left) and wet etching followed by the dry etching

State-of-the-Art GaN Vertical Power Devices

Tetsu Kachi from Toyota Central R&D Labs gave an outlook on the fabrication issues of bulk GaN power transistors.

Over the past decade, there are two types of GaN devices being developed, with either a lateral or a vertical structure. At present, mainstream GaN power devices have a lateral structure. On the other hand, progress in vertical devices was slower than that for lateral devices because GaN substrates lacked quality for high voltage applications. However, GaN substrate can become applied to high breakdown voltage above 1kV, and the vertical devices have recently attracted additional research attention.

The vertical structure has the advantages of current-collapse-free operation, small chip size, easy wiring and a high breakdown voltage. These characteristics are highly suited for high-power applications. The first developed device at Toyota was normally-on, with a threshold voltage -16 V, because the gate channel was an AlGaN/GaN heterostructure. This was the first demonstration of a vertical GaN transistor on a GaN substrate.



Cross-sectional structure of the GaN trench MOSFET. The trench was formed novel etching technology

Another device structure: a conventional trench MOSFET has also been examined. ICP dry etching was first used to form the trench. The trench shape after the dry etching was a V-shaped groove, and the sidewall of the trench was rough. Wet etching using tetramethylammonium hydride (TMAH) modified the dry-etched sidewall to be atomically flat. A GaN trench MOSFET was demonstrated using this novel trench fabrication technology.

The main issue is the quality of the GaN substrate. Toyota evaluated GaN substrates by forming Schottky barrier diodes on them in the early 2000's and observed high leakage currents under low reverse voltages. Recently, new approaches to high quality GaN substrates are being developed. These are liquid-phase growth technologies - the ammonothermal and the Na flux method. Both substrates contain few screw dislocations, these substrates have sufficient quality for high voltage applications. However, the entire GaN substrate area does not yet have a uniform quality. The remaining goals for GaN substrates are larger wafers of uniformly high quality and dislocation reduction.

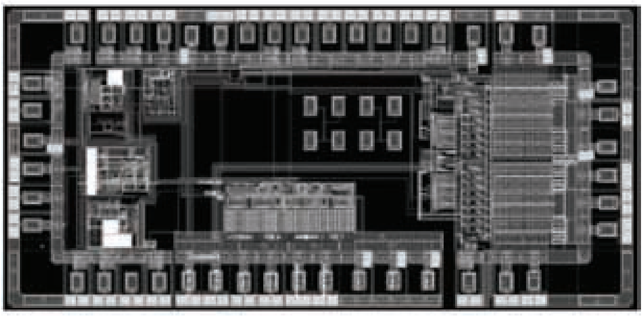
An other issue is low n-type doping control of the epitaxial layers. For example, a carrier concentration of less than 1×10^{16} cm^{-3} is required for breakdown voltages above 3 kV. However, epitaxial layers grown by MOCVD in general contain carbon atoms from Ga source, trimethylgallium at concentrations of approximately 1×10^{16} cm^{-3}. These carbon atoms will compensate Si donors and reduce electron mobility. The epitaxial conditions have been improved to reduce the carbon inclusion, and the residual carbon concentration was reduced to 3×10^{15} cm^{-3}.

To obtain the high breakdown voltage for a Schottky barrier diode (SBD), planarization of the GaN surface was effective. Toyota applied the catalyst-referred etching to planarize the epitaxial surface of GaN.

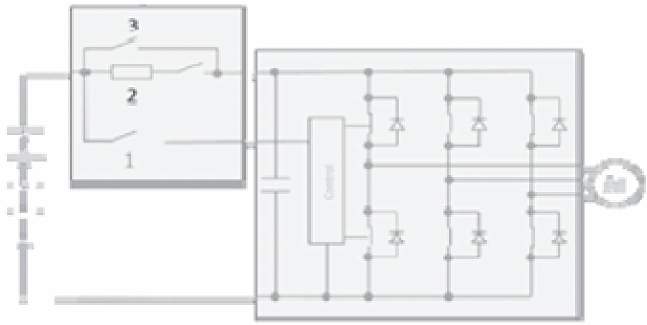
From Epitaxy to Converters Topologies

Developments of AlGaN/GaN based devices are driven by power switching applications, according to Lea Di Cioccio from CEA (**www.cea.fr**) in France. To compete in the market with SiC MOSFETs or Si IGBTs, performances of GaN HEMTs are of importance but cost is critical. This means high quality epitaxial layer growth with GaN on 200 mm Silicon substrates are the main challenges, while packaging and innovative topologies are also essential.

The design of Ga(Al)N epitaxial layers on Si (200 mm) has not yet



Wide Band Gap Gate Driver with Normally-On embedded management implemented with 0.35µm SOI technology



Normally-on device motor inverter cold-start up sequence (1-control added for n-on devices, 2-inverter input capacitor charge, 3-full power)

reached maturity and its impact on the final power device behavior is still significant. Buffer layers are needed to manage both the initial growth on Silicon and to adjust the stress in the layers to control the wafer bow. By improving the insulating behavior of these layers a leakage current of 50 nA/mm^2 at 600 V has been achieved for a total thickness less than 4 µm. Furthermore, the hole defect density has been drastically lowered thus increasing the blocking voltage limit. As a consequence devices up to 12 mm^2 can be produced with no impact on the leakage current.

The very fast switching characteristics of GaN introduce a problem caused by extreme variations in the drain voltage, commonly named dv/dt. High levels of dv/dt cause high current flow due to the Miller capacitance between the gate and the drain. It also induces a high common mode capacitive current in many converters architectures. In a half-bridge topology, a gate driver output stage with a relatively high on-resistance may cause the low side device to turn on accidentally. This phenomenon will increase the risk of power shoot- through and must be avoided. Techniques such as "the Miller clamp" are already used in industrial gate drivers to address this issue.

A demonstrator of a WBG Gate Driver with Normally-On embedded management, (0.35 µm SOI technology) has been implemented at CEA on a converter test board and tested up to 200°C.

Converter topologies should push the adoption of normally-on HEMTs with dedicated designs to handle the safety operation of the system. The channel conductivity of N-on is twice that of N-off HEMT, and the component technology will be easier, with no drastic gate recess, and no need for a high positive V_{th}. The cascode topology does not meet the high voltage requirement as the Si MOSFET is limited by its operating junction temperature. The cold start-up could be a solution. **AS**

Special Conference on Power Electronic Packaging and Integration

CIPS stands for a 3-day Conference on Power Electronics Packaging and Systems, Keynontes- and invited Papers, Dialog in Postersessions and Table Top Exhibition, and around 300 Delegates from March 8 to 10, 2016, in Nuremberg/Germany.

In the next decades, power electronic system development will be driven by energy saving systems, intelligent energy management, power quality, system miniaturization and higher reliability. Monolithic and hybrid system integration will include advanced device concepts (including wide bandgap devices), dedicated ideas for system integration, new ideas on packaging technologies and the overall integration of actuators/drives (mechatronic integration).

Thus CIPS is focussed on some main aspects such as: Integration with ultra high power density, of hybrid systems and mechatronic systems; systems and components operational behavior and reliability; basic technologies for integrated power electronics systems as well as upcoming new important applications which will be presented in interdisciplinary invited papers. Since 2010, CIPS is a IEEE sponsored conference. All accepted papers are avaible in IEEE Xplore.

The keynotes will cover: The Little Box Challenge (initiated by Google) by Prof. Kolar and Prof. Hoene; 100 MHz GaN power conversion by D. Maksimovic, Uni Boulder; Prospects of advances in power magnetics by C.R. Sullivan, Dartmouth College; and Review of Integration Trends in Power Electronics Systems and Devices by Gourab Majumdar, Mitsubishi Electric Corporation.

Invited papers will cover: SiC components by Peter Friedrichs, Infineon Technologies AG; GaN for industrial applications by Radoslava Mitova, Schneider-Electric; Design and Materials of Antiferroelectric Capacitors for High Density Power Electronic Applications by Günter Engel, CeraCap; Photovoltaic Inverters in µ-Scale by Regine Mallwitz, Technische Universität Braunschweig; Investigation of a power module with double sided cooling using a new concept for chip embedding by DI Hannes Stahr, AT&S AG; Challenges in low-voltage high-current applications - fathom the limits in system design by Ulf Schwalbe, Technische Universität Ilmenau; 1-MW Solar Power Conditioning System with Boost Converter using all-SiC Power Module by Yasuaki Furusho, Fuji Electric; Parasitic inductance hindering utilization of power devices by Reinhold Bayerer, Infineon Technologies AG; and New Gate Driver Solutions for Modern Power Devices and Topologies by Reinhard Herzer, SEMIKRON Elektronik.

The dialogue session has become over the years a very important part of the CIPS conference. It gives the participants and the authors a particular occasion to discuss and exchange their experiences. In order to promote papers presented at CIPS during the poster session - known as Dialogue Session - organizer VDE grant the Best Poster Award. The winner receives a high-value award (brass plate on wood), a certificate and monetary price of 1.000 Euro. A Young Engineer Award is sponsored by ECPE promoting young engineers with age below 35 presenting papers at the CIPS conference.

www.cips-conference.de

Time	Kaiser Karl IV	Kaiser Maximilian	Session
Tuesday, March 8			
10:30 AM-10:50 AM	Opening		
10:50 AM-12:50 PM	S01: System integration		
12:50 PM-02:00 PM			Lunch Break
02:00 PM-03:40 PM	S02: Converter	S03: Silver Sintering	
03:40 PM-04:10 PM			Coffee Break
04:10 PM-06:10 PM	S04: Control	S05: Die attach and wire bonds	
06:10 PM-06:30 PM			Break
06:30 PM-10:00 PM			DS: Dialog Session Little Box Challenge, DS: Dialog Session: Analytics, DS02: Dialog Session: Converter, DS03: Dialog Session: Silver Sintering, DS04: Dialog Session: Control, DS05: Dialog Session: Die attach, DS06: Dialog Session: Thermal Cycling, DS08: Dialog Session: Power Cycling, DS09: Dialog Session: Substrates, DS10: Dialog Session: Power Modules, DS11: Dialog Session: Temperature Measurements, DS12: Dialog Session: Lifetime, DS14: Dialog Session: Passives, DS15: Dialog Session: Parasitics, Clean Switching, EMC
Wednesday, March 9			
08:40 AM-10:20 AM	S06: Thermal Cycling	S07: Thermal Management	
10:20 AM-10:50 AM			Coffee Break
10:50 AM-12:30 PM	S08: Power Cycling	S09: Substrates	
12:30 PM-01:40 PM			Lunch Break
01:40 PM-03:00 PM	S10: Power Modules	S11: Temperature Measurements	
03:00 PM-03:30 PM			Coffee Break
03:30 PM-05:20 PM	S12: SiC Power Modules	S13: Lifetime	
07:00 PM-10:00 PM			Conference Dinner
Thursday, March 10			
08:30 AM-10:20 AM	S14: Passives		
10:20 AM-10:50 AM			Coffee Break
10:50 AM-12:00 PM	S15: Clean Switching, EMC		
12:00 PM-01:00 PM	S16: Integrated Power Electronics		
01:00 PM-02:00 PM			Lunch Break
02:00 PM-03:40 PM	S17: Wide-band-gap Applications		
03:40 PM-04:10 PM	Closing		

APEC 2016 — The Premier Global Event in Applied Power Electronics — March 20-24, 2016 — Long Beach California — Long Beach Convention & Entertainment Center

Conference for Practising Power Electronics Engineers

APEC's comprehensive program is according to the organizers remarkably attractive to the academic researchers, students, educators, industry, government agencies, and general public. The technical presentation papers are selected from a record high 1212 digests submitted from 45 countries. The exposition hits its record high participation with 263 exhibitors and 398 booths. The event will take place from March 20 – 24 in Long Beach, USA.

The Professional Educational Seminars, offered by internationally renowned experts, start on Sunday, March 20. Each of the 21 three-and-a-half hour educational seminars, selected from 52 submissions, provides an in-depth discussion of important and complex power electronics topics and combines practical application with theory.

The Plenary Session, on Monday afternoon, consists of distinguished world-class speakers from industry and academia covering the key power electronics technologies, components, and innovations affecting our industry and the society. Presentations include: The Challenges of VHF Power Conversion by Tony Sagneri, Finsix Corp.; The Future of Power Electronic Design by Michael Harrison, Enphase Energy; Breaking Speed Limits with GaN Power ICs by Dan Kinzer, Navitas Semiconductor; Residential Nanogrids With Battery Storage – Is This Our Future? by Antonio Ginart, University of Georgia; The Future of Magnetic Design for Power Electronics by Ray Ridley, Ridley Engineering; and Why Do Power Supplies Fail? – A Real-World Analysis by David Hill, Power Clinic.

The progressively popular industry sessions feature 119 presentations in 20 sessions from March 22 – 24.. Speakers are invited to make a presentation only, without submitting a formal manuscript for the APEC Proceedings. This allows to present information on current topics in power electronics from sources that would not otherwise be present at an industry conference. While many of these sessions are technical in nature, some also target business-oriented people such as purchasing agents, electronic system designers, regulatory engineers, and other people who support the power electronics industry.

www.apec-conf.org

DIALOGUE SESSIONS

THURSDAY, MARCH 24TH
11:30 A.M. - 1:30 P.M.

D01	AC-DC Converters
D02	DC-DC Converters I
D03	DC-DC Converters II
D04	Utility Interface
D05	Motor Drives and Inverters: Modeling and Control I
D06	Motor Drives and Inverters: Modeling and Control II
D07	Motor Drives and Inverters: Topologies
D08	Advanced Components and Devices
D09	System Design Considerations for Power Electronics
D10	Modeling and Simulation
D11	Control I
D12	Control II
D13	Renewable Energy Systems I
D14	Renewable Energy Systems II
D15	Transportation Power Electronics
D16	Power Topologies, Distribution, and Control
D17	Emerging and Renewable Power

TECHNICAL SESSIONS

TUESDAY, MARCH 22ND 8:30 A.M. - 12:00 P.M.

T01	Three-Phase AC-DC Converters
T02	High Frequency and Fast-Response DC-DC Converters
T03	Microgrids and Hybrid Systems
T04	Control Strategies for Inverters and Motor Drives
T05	Si Devices and Power Module Packaging
T06	DC-DC Converter Control
T07	Solar Energy Systems
T08	Advanced Converter for Power Systems used in Transportation
T09	Gate Drives, Failure Analysis, and Protection

WEDNESDAY, MARCH 23RD 8:30 A.M. - 10:10 A.M.

T10	Control of AC-DC Converters
T11	GaN-based DC-DC Converters
T12	Electric Machines
T13	Advances in Magnetics
T14	System Design and Layout for Improved Performance
T15	Modeling of AC Energy Converters and Systems
T16	Manufacturing, Test, and Reliability
T17	Soft-Switching Converters in Renewable Energy Systems
T18	Solid State Lighting

WEDNESDAY, MARCH 23RD 2:00 P.M. - 5:30 P.M.

T19	Resonant and Soft Switching DC-DC Converters
T20	Control Applications and Modulation Schemes
T21	Advances in Wide BandGap Devices
T22	Motor Drive Design and Inverter Topologies
T23	Modeling of Magnetic Circuits and Systems
T24	Inverter/Converter Control
T25	Topics in Renewable Energy Systems I
T26	Electric Vehicle Charging Systems
T27	Utility Interface & Inverter Applications

THURSDAY, MARCH 24TH 8:30 A.M. - 11:20 A.M.

T28	Isolated DC-DC Converters
T29	Multilevel Converters
T30	Multilevel and Matrix Converters for Motor Drives
T31	System Design Techniques for Reduced EMI
T32	Modeling of DC Energy Converters and Systems
T33	Gate Drive Techniques
T34	Energy Storage Systems
T35	Topics on Inductive and Capacitive Wireless Power Transfer
T36	Wireless Power Transfer

THURSDAY, MARCH 24TH 2:00 P.M. - 5:30 P.M.

T37	Single-Phase AC-DC Converters
T38	Non-Isolated DC-DC Converters
T39	Inverter Applications and Technologies
T40	Modeling, Modulation and Control of Motor Drive
T41	Gate Drivers and Integrated Packaging
T42	Component Modeling
T43	Grid and Utility Interface
T44	Topics in Renewable Energy Systems II
T45	Envelope Tracking and Resonant Conversion

pcim
EUROPE

International Exhibition and Conference
for Power Electronics, Intelligent Motion,
Renewable Energy and Energy Management
Nuremberg, 10 – 12 May 2016

Bigger Than Ever

Over 240 speakers from more than 25 countries presented the latest technological trends in power electronics components and systems at the PCIM Europe 2015 Conference. And this conference with more than 700 delegates was backed at the exhibition floor by 417 exhibitors and 88 represented companies and nearly 9000 visitors. According to the organizer Mesago, the number of exhibitors, as well as the booked exhibition area, are this year clearly exceeding from May 10 – 12 the previous year's level. This emphasizes the great importance of the event as the leading European knowledge platform within the power electronics community.

Keynotes on current issues

Welcome to the Post-Silicon World: Wide Band Gap Powers Ahead - that is the title of Dan Kinzer's PCIM keynote on the first day. He is co-founder of Navitas Semiconductor, a young company focused on advanced GaN power semiconductor devices and circuits, located in El Segundo, USA.

"In the early 1980's, industry pioneers transformed the Silicon bipolar transistor into the mass production MOSFET. The 1990's saw the adoption of IGBTs, and the 2000's brought superjunction MOSFET into volume. Now, an even more fundamental transition is underway as Silicon is overtaken by the introduction of SiC and GaN high performance, wide band-gap power products. The breakthrough performance of qualified products, with the subsequent application benefits of size and cost, is now fully appreciated by power system designers. As the 'eco-system' continues to mature, with new enabling topologies, control ICs and magnetic solutions, the transition will accelerate and transform the power industry". In his presentation examples will

Again it's time to prepare for PCIM Europe Nuremberg in May be taken from applications such as electric vehicles, renewable energy, power supplies, and battery chargers.

Smart Transformers – Concepts/Challenges/Applications – will be discussed on the second day keynote by Prof. Dr. Johann Walter Kolar, ETH Zurich Power Electronic Systems Laboratory.

And on the third day the keynote is entitled "Trends of solar system integration electricity networks" to be given by Jens Merten, Commissariat à l'énergie atomique et aux énergies alternatives, Le Bourget-du-Lac, France. "With their constant cost reduction, solar systems have become already today an economically viable alternative in many regions of the world. While the cost for solar modules has been drastically reduced in the last years, the cost reduction potential for the balance of system, like for example power conditioners, still needs to be exploited. On the other side, the massive penetration of variable solar energy systems challenges the management of the electricity networks". His speech outlines trends for solving these issues.

GaN on the system level

Since Gallium Nitride devices have been covered over the past in various PCIM Special Sessions i. e. organized by PEE this year's focus within the conference is more on the system level, expressed by a session called "GaN Converters" on the second day.

An "EMI Study in a GaN HEMT Power Module" will be presented by Xiaoshan Liu from SATIE Laboratory in France. The inherent RLC parasitics of an insulated metal substrate (IMS) power module have been modeled and their impacts on EMI have been studied by time domain simulation + FFT analysis. A PCB IMS has been proposed for a medium power GaN module by using a 650V 30A e-GaN HEMT. The mid-point parasitic capacitor has been minimized. IMS parasitic capacitances and discrete SMD capacitors are used as common mode (CM) and differential mode (DM) integrated filters. The DC bus impedances are balanced to avoid EMI noise transfer from DM to CM.

"Ultra-High Frequent Switching with GaN-Fets using the C_{oss}-Capacitances as non-dissipative Snubbers" is the subject of the second paper by Luis Alfonso Fernández-Serante from FH JOANNEUM in Austria. Due to the faster transients of wide bandgap transistors, the output capacitance can essentially influence the switching behavior and the losses. The switching cycle of a 650 V GaN-Fet half-bridge is analyzed. A linearized model serves for deriving the relations and explaining how the C_{oss} can be used for minimizing the losses, by using it as an non-dissipative snubber, providing soft switching. EMI-measurements are showing the reduction of radiated emissions when using soft-switching mode.

An "eGaN FET based 6.78 MHz Differential-Mode ZVS Class D A4WP Class 4 Wireless Power Amplifier" will be introduced by Michael de Rooij, Efficient Power Conversion (EPC) Corporation, USA. An eGaN FETs based 33 W capable A4WP class 4 power amplifier is presented. As the power levels and charge surface area increase, so do the design challenges. This paper delves into the challenges to realize a class 4 wireless power solution that include amplifier thermals, radiated EMI, coil re-tuning, and device side rectification.

A "High Frequency, High Temperature DC/DC Converter for GaN Gate Drivers" has been designed by Yohan Wanderoild at CEA Leti, Grenoble, France. It will be discussed in detail.

Finally, a "Fully-Monolithic GaN-on-Si Half-Bridge with Integrated Reverse-Diodes" will be discussed by Richard Reiner, Fraunhofer Institute for Applied Solid State Physics (IAF) in Freiburg, Germany. This work presents the design, realization, and the characterization of a monolithic GaN on Si half-bridge circuit with integrated Schottky-contacts as reverse-diodes. The extrinsic and intrinsic layouts are realized, explained and compared to other approaches. The high- and low-side switches feature an off-state voltage of 600 V, an on-state resistance of 120 mΩ, and a reverse resistance of below 150 mΩ at corresponding drain currents of 30 A.

More GaN demos will be presented within the poster sessions, at the exhibition floor and in our upcoming extensive PCIM preview, as well as other power electronic innovations. **AS**

New InnoSwitch-CP ICs Improve Charging Performance of Smart Mobile Devices

Power Integrations announced its InnoSwitch™-CP family of off-line CV/CC flyback switching ICs, a successor of the recently introduced Innoswitch-EP. Two devices are available: The INN2214K IC delivers 15 W constant output power between 5 and 9 V for universal voltage chargers and adapters, while the larger INN2215K part delivers up to 22 W for similar applications. Devices are priced at $0.90 in 10,000-piece quantities.

The new devices incorporate a constant power output profile which, when paired with an adaptive-voltage protocol such as Qualcomm® Quick Charge™ 3.0 or USB-PD, permits smart mobile device makers to optimize charging time across a range of products. Adaptive charging achieve faster charge times, improved charging efficiency and backward compatibility with the popular 5 V USB BC 1.2 specification, all while minimizing overall thermal management and battery charging system cost.

Operation principle

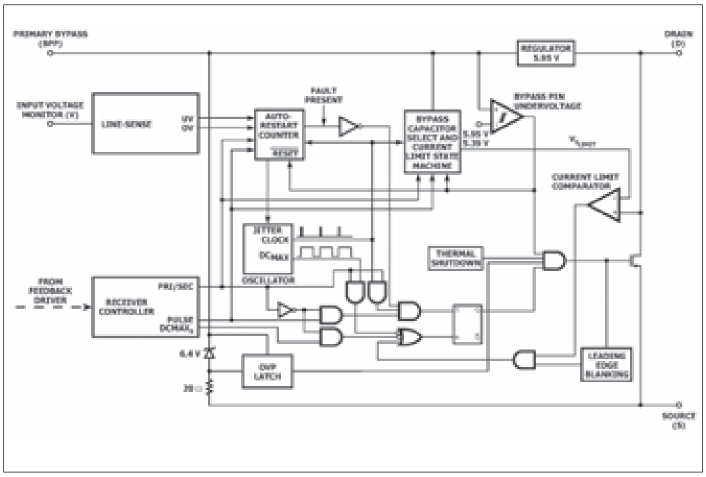
The InnoSwitch-CP combines a high-voltage power MOSFET switch, along with both primary- and secondary-side controllers in one device. It has a novel inductive coupling feedback scheme using the package leadframe and bond wires for accurate direct sensing of the output voltage and output current on the secondary to communicate information to the primary IC. This so-called FluxLink™ technology enables secondary-side control with the simplicity and low component count usually associated with primary-side regulation. FluxLink also optimizes the effectiveness of output synchronous rectification, resulting in high efficiency across the full load range. For example, no-load consumption at 230 VAC is less than 10 mW, while full-load efficiency exceeds 90 %.

The IC operate in the current limit mode. When enabled, the oscillator turns the 650 V synchronous power MOSFET on at the beginning of each cycle. The MOSFET is turned off when the current ramps up to the current limit or when the DC_{MAX} limit is reached. Since the highest current limit level and frequency are constant, the power delivered to the load is proportional to the primary inductance of the transformer and peak primary current squared. Hence, designing the supply involves calculating the primary inductance of the transformer for the maximum output power required. If the InnoSwitch-CP is appropriately chosen for the power level, the current in the calculated inductance will ramp up to current limit before the DC MAX limit is reached.

InnoSwitch-CP senses the output voltage on the FEEDBACK pin using a resistive voltage divider to determine whether or not to proceed with the next switching cycle. The sequence of cycles is used to determine the current limit. Once a cycle is started, it always completes the cycle. This operation results in a power supply in which the output voltage ripple is determined by the output capacitor, and the amount of energy per switch cycle.

Unlike conventional PWM (pulse width modulated) controllers, it uses a simple ON/OFF control to regulate the output voltage and current. The primary controller consists of an oscillator, a receiver circuit magnetically coupled to the secondary controller, current limit state machine, 5.95 V regulator, over-voltage

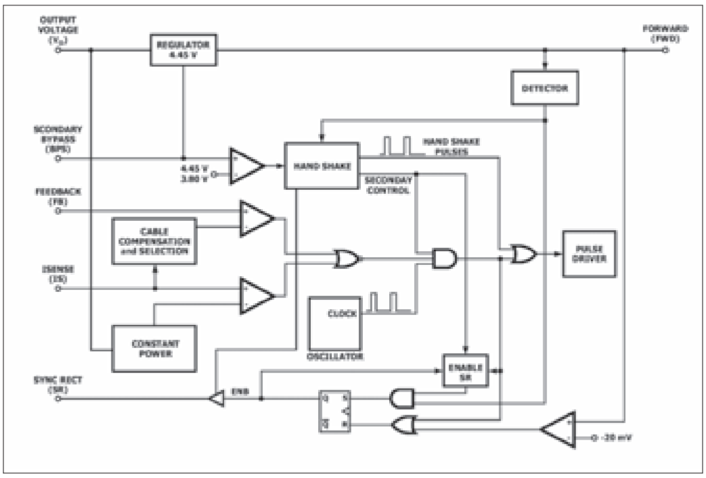
InnoSwitch™-CP off-line CV/CC flyback switching IC for output power up to 22 W



Innoswitch-CP primary side controller block diagram

circuit, current limit selection circuitry, over-temperature protection, leading edge blanking and a 650 V power MOSFET. The secondary controller consists of a transmitter circuit that is magnetically coupled to the primary receiver, constant voltage (CV) and constant current (CC) control circuitry, a 4.4 V regulator, synchronous rectifier MOSFET driver, frequency jitter oscillator and a host of integrated protection features.

The internal clock of the InnoSwitch-CP runs all the time. At the beginning of each clock cycle, the voltage comparator on the FEEDBACK pin decides whether or not to implement a switch cycle, and based on the sequence of samples over multiple cycles, it determines the appropriate current limit. At high loads, the state machine sets the current limit to its highest value. At lighter loads, the state machine sets the current limit to reduced values. At



Innoswitch-CP secondary side controller block diagram

near maximum load, InnoSwitch-CP will conduct during nearly all of its clock cycles. At slightly lower load, it will “skip” additional cycles in order to maintain voltage regulation at the power supply output. At medium loads, cycles will be skipped and the current limit will be reduced. At very light loads, the current limit will be reduced even further. Only a small percentage of cycles will occur to satisfy the power consumption of the power supply.

The response time of the ON/OFF control scheme is very fast compared to PWM control. This provides accurate regulation and excellent transient response.

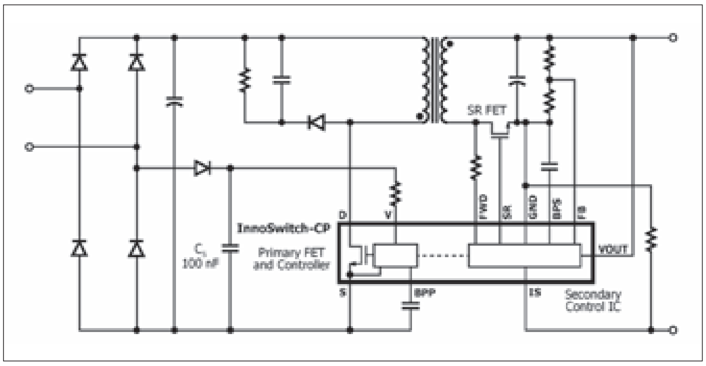
Power supply design considerations

InnoSwitch-CP features a primary sensed OV protection feature that can be used to latch off the power supply. Once the power supply is latched off, it can be reset if the V pin current is reduced to zero. Once the power supply is latched off, even after input supply is turned off, it can take considerable amount of time to reset the internal controller as the energy stored in the DC BUS will continue to provide bias supply to the controller.

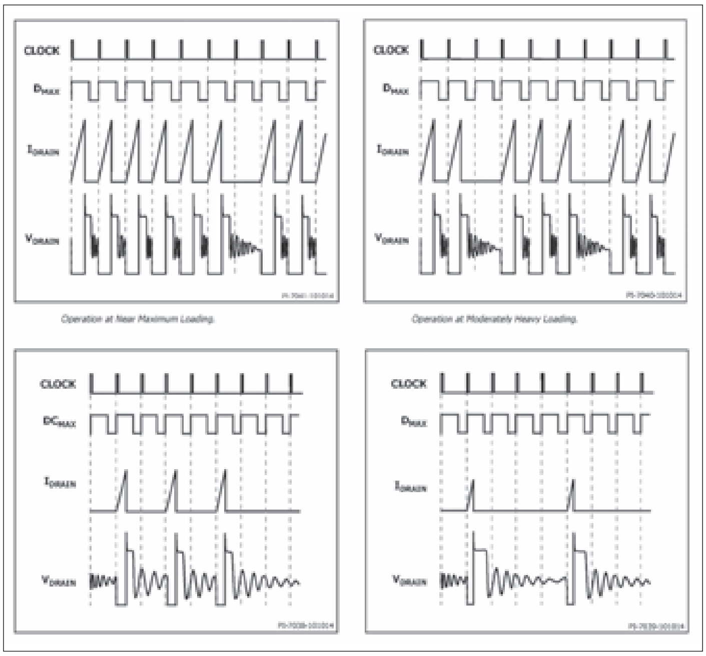
A fast AC reset can be achieved using a modified shown circuit configuration. The voltage across capacitor C_S reduces rapidly after input supply is disconnected which rapidly reduces current into the INPUT VOLTAGE MONITOR pin of the IC and resets the controller.

It is recommended that the highest voltage at the output of the bias winding should be measured for normal steady-state conditions at full rated load and lowest rated input voltage and also under transient load conditions. A Zener diode rated for 1.25 times this measured voltage will typically ensure that OVP protection will not operate under any normal operating conditions and will only operate in case of a fault condition. Use of the primary sensed OVP protection is highly recommended.

Although a simple diode rectifier and filter is adequate for the secondary-winding, use of a SR MOSFET enables significant improvement in operating efficiency often required to meet the European CoC and the U.S. DoE energy efficiency requirements.



Fast AC reset configuration



Innoswitch-CP operation at full load (upper left) to very light load (lower right)

The secondary-side controller turns on the SR MOSFET once the flyback cycle begins. The SR MOSFET gate should be tied directly to the SYNCHRONOUS RECTIFIER DRIVE pin of the InnoSwitch-CP IC. The SR MOSFET is turned off once the drain voltage of the SR MOSFET drops below -24 mV ($V_{SR(TH)}$). Therefore the use of MOSFETs with a very small on-resistance can be counterproductive as it reduces the MOSFET's on-time, commutating the current to the body diode of the MOSFET or an external parallel Schottky diode if used.

A MOSFET with 18 mΩ RDS(ON) is a good choice for designs rated for a 5 V, 2 A output. The SR MOSFET driver uses the secondary SECONDARY BYPASS pin for its supply rail and this voltage is typically 4.4 V. A MOSFET with too high a threshold voltage is therefore not suitable and MOSFETs with a low threshold voltage of 1.5 V to 2.5 V are ideal although MOSFETs with a threshold voltage (absolute maximum) as high as 4 V may be used.

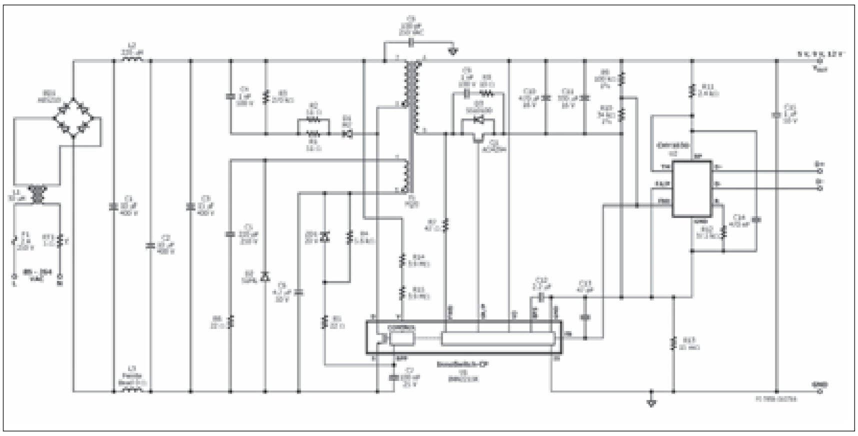
Regarding the output capacitor, low ESR aluminum electrolytic capacitors are suitable for use with most high frequency flyback switching power supplies though the use of aluminum-polymer solid capacitors have gained considerable popularity due to their compact size, stable temperature characteristics, extremely low ESR and simultaneously high RMS ripple current rating. These capacitors enable design of compact chargers and adapters.

Typically, 200 μF to 300 μF of aluminum-polymer capacitance is often adequate for every ampere of output current. The other factor that influences choice of the capacitance is the output ripple. Care should be taken to ensure that capacitors with a voltage rating higher than the highest output voltage with sufficient margin (>20 %) be used.

Typical adapter/charger application

The circuit shown in the application schematic is a low-cost high-efficiency quick charge adapter using the INN2215K. This design features DOE Level 6 and EC CoC 5 compliance. The integration offered by InnoSwitch-CP reduces component count from >60 to only 41. The charger provides 5 V at 3 A, 9 V at 2 A and 12 V at 1.5 A. The output is continuously adjustable in 200 mV increments per the QC 3.0 protocol to set the output voltage to other values.

Bridge rectifier BR1 rectifies the AC input supply. Capacitors C1, C2 and C3 provide filtering of the rectified AC input and together with inductor L2 form a pi-filter to attenuate differential mode EMI. Inductor L1 and capacitor C8 provide common mode noise filtering. Capacitor C15 connected at the power



QC 3.0 compliant charger/adapter featuring 5 V, 3 A; 9 V, 2 A; 12 V, 1.5 A output

supply output helps to reduce high frequency radiated EMI. Thermistor RT1 limits the inrush current when the power supply is connected to the input AC supply. Input fuse F1 provides protection against excess input current resulting from catastrophic failure of any of the components in the power supply.

One end of the transformer primary is connected to the rectified DC bus; the other is connected to the drain terminal of the MOSFET inside the InnoSwitch-CP IC (U1). A low-cost RCD clamp formed by diode D1, resistors R1, R2 and R3, and capacitor C4 limits the peak drain voltage of U1 at the instant of turn-off of the MOSFET inside U1. The clamp helps to dissipate the energy stored in the leakage reactance of transformer T1.

The InnoSwitch-CP IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor (C7) when AC is first applied. During normal operation the primary-side block is powered from an auxiliary winding on the transformer T1. Output of the auxiliary (or bias) winding is rectified using diode D2 and filtered using capacitor C6. Resistor R4 limits current being supplied to the BPP pin of the InnoSwitch-CP IC (U1).

Output regulation is achieved using On/Off control and the number enabled switching cycles are adjusted based on the output load, as outlined above. There are four operating states (current limits) arranged such that the frequency content of the primary current switching pattern remains out of the audible range until at light load where the transformer flux density and therefore audible noise generation is at a very low level. The secondary-side of the InnoSwitch-CP IC provides output voltage, output current sensing and drive to the MOSFET providing synchronous rectification.

The secondary of the transformer is rectified by diode D3 and filtered by capacitors C10 and C11. High frequency ringing during switching transients that would otherwise create radiated EMI is reduced via a snubber (resistor R8 and capacitor C9). To reduce dissipation in the diode D3, synchronous rectification (SR) is provided by MOSFET Q1. The gate of Q1 is turned on by secondary-side controller inside the IC based on the winding voltage sensed via resistor R7 and fed into the FWD pin of the IC. In continuous conduction mode of operation, the MOSFET is turned off just prior to the secondary-side commanding a new switching cycle from the primary. In discontinuous mode of operation, the power MOSFET is turned off when the voltage drop across the MOSFET falls below a threshold of approximately -24 mV. Secondary side control of the primary-side power MOSFET avoids possibility of cross conduction of the two MOSFETs and provides extremely reliable synchronous rectification. As the SR MOSFET is not on for the full switching cycle, a small low current diode is still required (D3) to increase efficiency.

www.power.com/innoswitch-cp/

High-Voltage SiC Power Modules for 10 – 25 kV Applications

The development of power electronic devices with higher operating voltages (6.5 kV+) has enabled more power to be transmitted for a given current and reduced the number of switches required to reach those voltage levels in multi-level converters. Silicon Carbide (SiC) power devices – with their significantly higher blocking voltages (into the tens of kilovolts), higher switching frequencies, and higher operating temperatures (200°C) – have had a major impact on the ability of power electronics engineers to develop power modules that are more compact, operate at higher voltages, and require less thermal management than power modules designed with conventional Silicon devices. **Brandon Passmore, Development Engineering Manager, Chad O'Neal, Development Engineer, Electronics Packaging, Wolfspeed, Research Triangle Park, USA**

Designing and manufacturing these new compact, SiC-based high voltage power modules requires important consideration regarding insulation materials, creepage/clearance design, an optimized parasitic design, external bussing connection scheme, and high temperature and environmental testing. The two SiC power modules described in this article clearly demonstrate the potential for SiC devices in high-voltage applications, including energy storage, grid-connected power electronics, electric rail, and shipboard power systems.

SiC power module for 15 kV applications

A low profile power module has been designed around the latest generation of high-voltage SiC device technology, enabling increased operating voltage while minimizing both the module's size and the need for extensive thermal management. Compared to 6.5 kV Si-based solutions, this SiC-based power module is one-third the volume and half the weight, and has 10X higher switching speeds and 2X the breakdown voltage with reduced cooling requirements. At the system level, this translates into more than 10 % increased efficiency with a 50 % reduction in energy losses, which increases the power density of the system. As such, this novel SiC power module represents a powerful new building block for power electronics systems that require simplified design and increased operating efficiency.

Shown in Figure 1, this power module is a half-bridge configuration with eight SiC power devices per switch position: four SiC switching power devices and four SiC Schottky diodes. This module design can employ a wide range of different high-voltage devices, including SiC MOSFETs rated for 10 kV / 40 A or SiC IGBTs rated for 15 kV / 80 A. The module design also includes an integrated temperature sensor that monitors the die junction temperature during operation.

Internal bonding variations within the module include a standard wire-bond die interconnect, as well as an option for flip-chip mounting. The substrates, baseplates, and housing are standard for both module configurations to standardize manufacturability. After the baseplate and substrate are joined with high-temperature solder, the four separate half-bridge subassemblies are tested before incorporating them into the module. This enables separate testing and quality control for the subassemblies, providing design engineers with a critical opportunity to rework the device prior to final assembly.

Subdividing the module's switch positions also improves the thermal-mechanical characteristics, reducing the effects of bowing due to thermal expansion mismatches in the materials used. The subassembly baseplates are made from a low coefficient of thermal expansion (CTE) metal-matrix composite material with a low

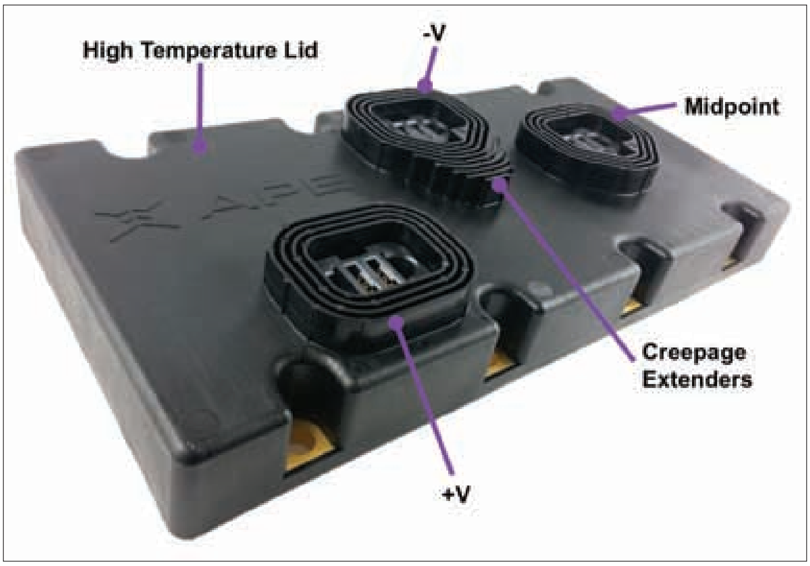


Figure 1: 15 kV SiC power module rated at 200°C operation - key characteristics include reworkability, modularity, and small form factor

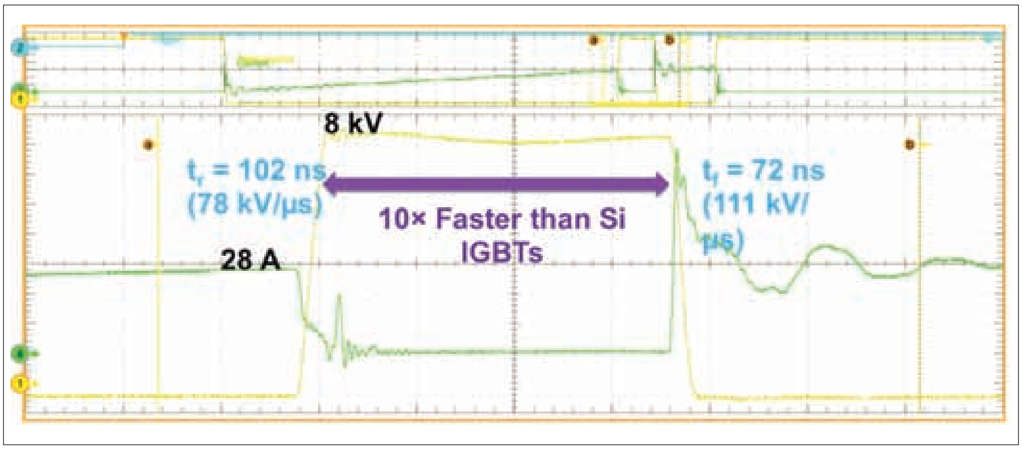


Figure 2: **Clamped inductive load switching waveform (V_{bus} = 8 kV, I_{switch} = 28 A, Rg = 2.5Ω) for a submodule of the 15 kV power module**

density, which contributes to the 80 % weight reduction, as the baseplate is often the heaviest component of the module. Moreover, since there are typically multiple modules per system, this module weight reduction can contribute to a significant reduction of the total system weight.

The module housing is molded from a high temperature plastic, which provides protection from higher temperature environments and allows for high-temperature operation. In addition, the high temperature plastic housing was designed to meet UL and IEC creepage (Pollution Degree 2) requirements based on 15 kV operation. Internal clearances are maintained with a high temperature Silicone gel.

To demonstrate the high performance packaging design coupled with the superior dynamic characteristics of 10 kV SiC MOSFETs, the improvement in dynamic characteristics for a submodule can be seen in Figure 2, which illustrates the clamped inductive load test results for the module at 8 kV /28 A. Using a gate resistor of 2.5 Ω, the submodule exhibits switching speeds up to 111 kV/µs, which equates to a 10X improvement in switching speed over conventional Si IGBTs. The switching energy plots, shown in Figure 3, demonstrate the turn-on, turn-off, and total energy data for the submodule.

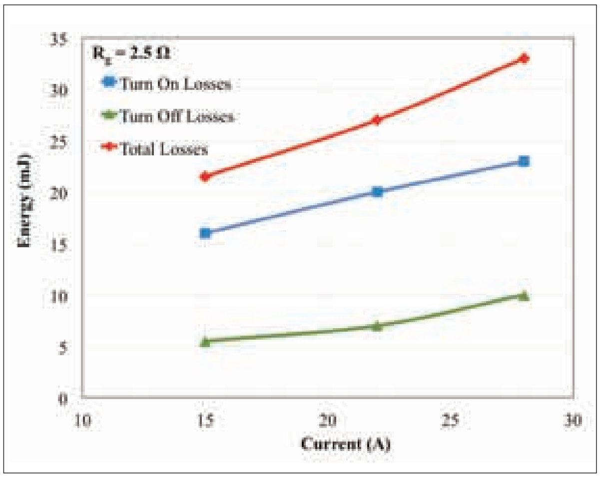


Figure 3: **Switching energy as a function of current at 8 kV for a submodule - total switching losses are 70X lower than a Si-based 6.5 kV / 250 A IGBT power module**

Power Module at 24 kV / 30 A using SiC IGBTs

An evaluation module using high-voltage (24 kV) SiC IGBTs was recently developed under a contract with the U.S. Army Research Lab (Cooperative Agreement Number W911NF-13-2-0023) to meet a specific requirement for an ultra-high voltage module with a compact footprint. The internals of the module were designed to withstand 24 kV operation and are shown in Figure 4. As designed, the terminal spacings do not meet clearance spacings to withstand breakdown in open air. Thus, the module was designed to operate in a dielectric fluid.

The module can be internally configured for several different basic topologies, including an IGBT diode co-pack, boost chopper, or half-bridge configuration, providing design engineers with several building block topology choices for implementing this type of module into a broad range of high-voltage applications.

The module is specifically designed for high temperature (200°C) operation, employing dielectric potting material in the interior of the module and high temperature plastic for the external housing. The power module was carefully designed using finite element modeling and advanced CAD tools to determine mechanical stresses, thermal gradients, electric field strengths, and overall module parasitics. Additionally, the baseplate material was selected to have a closely matched coefficient of thermal expansion with the thick ceramic substrate used to electrically isolate the high voltage SiC IGBTs from the baseplate.

In previous work performed by Wolfspeed [1], the electrical performance of the module for reverse blocking and switching performance over temperature is presented in Figure 5. The clamped inductive load testing was performed at 14 kV / 22 A, demonstrating a switching speed of 46 kV/µs, with some degradation noted as the temperature rises to 125°C. However, it is worth noting that this device

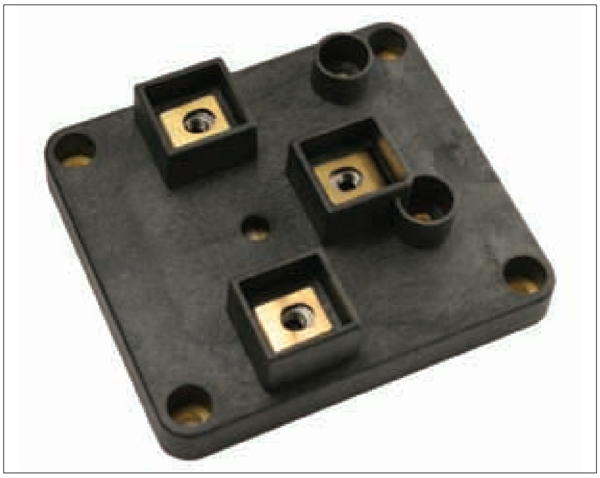


Figure 4: **24 kV / 30 A SiC IGBT power module**

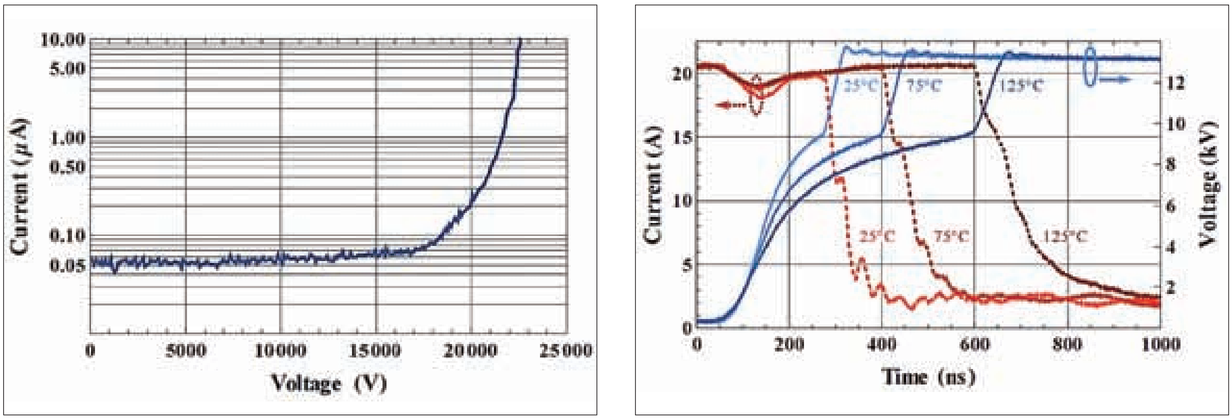


Figure 5: Reverse leakage for 24kV SiC IGBTs (left) and dynamic characteristics for 24 kV / 30 A SiC IGBTs over temperature

and its performance will improve substantially as development progresses. Overall, the 24 kV SiC IGBTs exhibit extremely fast switching speeds.

Conclusions

The two high voltage, high temperature SiC power modules demonstrate the extremely fast switching characteristics of high voltage SiC-based transistors. Module packaging designed especially for these and other wide bandgap power devices enables reduced physical size and complexity in multi-level systems, the elimination of external cooling systems, and a significant increase in both efficiency and power density at the system level. Specifically, the high voltage and thermal characteristics of SiC power devices will enable power electronics design engineers to significantly reduce the number of topology levels compared to conventional silicon power modules. Although the cost of the SiC devices is often seen as a barrier to adoption, their cost is continually being reduced as production volume increases. Furthermore, since the integration of SiC devices enables a reduction of overall system cost and significantly increases performance, it will not be necessary for SiC devices to reach true cost parity with Silicon in order to make the overall value proposition for system integrators successful.

Literature

[1] E. V. Brunt, L. Cheng, M. O'Loughlin, C. Capell, C. Jonas, K. Lam, et al., "22 kV, 1 cm2, 4H-SiC n-IGBTs with Improved Conductivity Modulation," in 26th International Symposium on Power Semiconductor Devices & IC's, Waikoloa, Hawaii, 2014, pp. 358-361.

Maximizing Cell Monitoring Accuracy and Data Integrity

Grid-connected battery arrays are viable backup and carry-through power sources; application-specific measurement ICs which meet their unique and sophisticated requirements ensure reliable system performance. **Mike Kultgen, Greg Zimmer, Linear Technology, and Stefan Janhunen, BMS Products, Nuvation Engineering, USA**

The use of large-scale battery arrays for backup and carry-through energy storage is getting increasing attention, as evidenced by Tesla Motors' recent announcement of their Powerwall system for homes and offices. The batteries in these systems are continually charged from the power-line grid or other source, and then deliver AC-line power back to the user via a DC/AC inverter.

Using batteries for power backup is not new, with many systems spanning basic 120/240V AC and several hundred watts for short-term desktop-PC backup, to thousands of watts for specialty vehicles, such as ships, hybrid cars, or all-electric vehicles, up to hundreds of kilowatts for grid-scale telecom and data-center backup. Yet while advances in battery chemistry and technology get much of the attention, an equally critical part of a viable battery-based installation is its battery management system (BMS).

There are many challenges when implementing battery management systems for energy storage, and their solutions do not simply "scale up" from small-scale, lower-capacity battery packs. Instead, new and more sophisticated strategies and critical support components are needed.

The challenge begins with the need for high accuracy and confidence in the many measurements of key battery cell parameters. Further, the design must be modular in its subsystems to enable tailoring the configuration to the specific needs of the application, along with possible expansion, overall management issues, and necessary maintenance.

The operating environment of larger-scale storage arrays brings other significant challenges, as well. The BMS must provide precise, consistent data within an extremely noisy electrical and often hot environment despite the high voltage/current inverters and resultant current spikes. In addition, it must provide extensive "fine-grain" data on internal module and system temperature measurements, which are critical for charging, monitoring, and discharging, rather than just a few broad-brush aggregate values.

Due to the basic role of these power systems, their operating reliability is inherently critical. To translate that easily stated objective into reality, the BMS must ensure data accuracy and integrity, along with continuous health assessments so it can take the needed actions on an ongoing basis. Achieving a robust design and safety is a multi-level process, and the BMS must anticipate problems, perform self-test, and provide failure detection on all subsystems, then implement appropriate actions while in standby and operational modes. As a final mandate, due to the high voltage, current, and power levels, there are many stringent regulatory standards that the BMS must meet.

System design translates concepts to the real-world results

Although monitoring rechargeable batteries is simple in concept – just place the voltage- and current-measurement circuits at the cell terminals – the reality of a BMS is quite different and much more complicated.

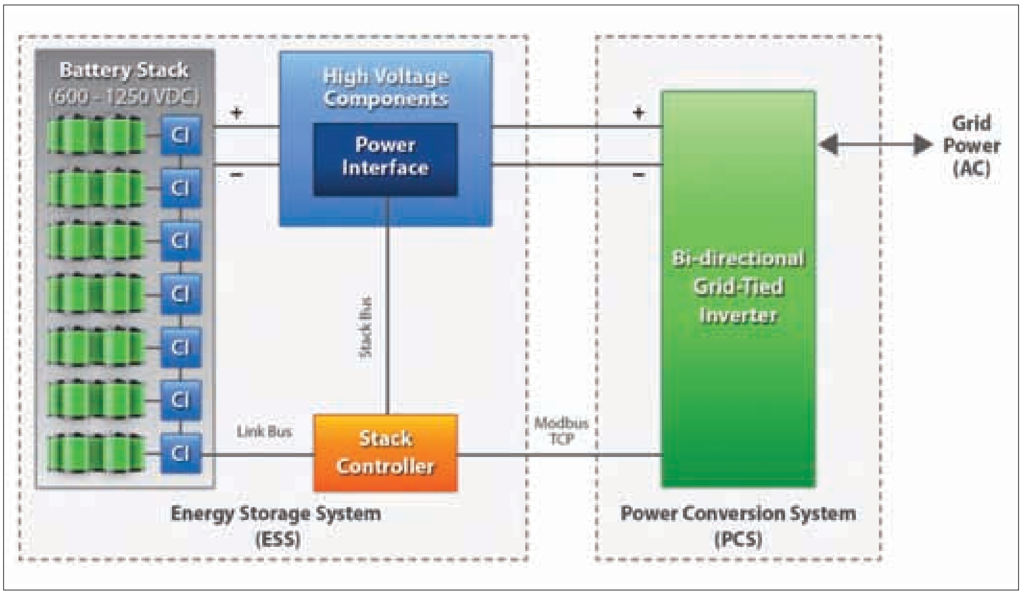
Robust design begins with comprehensive monitoring of individual battery cells, which places significant demands on analog functions. The cell readings need millivolt and milliamp accuracy, and voltage and current measurements must be time-synchronized to calculate power. The BMS must also assess validity of each measurement, as it needs to maximize data integrity, while it must also identify errors or questionable readings. It cannot ignore unusual readings which may indicate a potential problem, but at the same time, it should not take action based on data which has errors.

A modular BMS architecture enhances robustness, scalability, and reliability. Modularity also facilitates use of isolation where needed in the data links between subsections to minimize impact of electrical noise and to enhance safety. In addition, advanced data-encoding formats including CRC (cyclic redundancy check) error detection and link-acknowledgement protocols assure data integrity, so the system management function has confidence that the data it receives is what was sent.

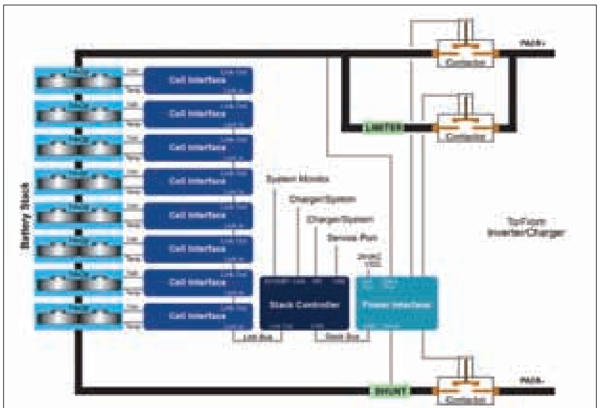
An example of a BMS that incorporates these principles is the scalable and customizable battery management system developed by Nuvation Engineering. This BMS design is proving itself with design wins in grid energy-storage systems and power-backup equipment, where reliability and ruggedness are critical. The key advantage for this off-the-shelf BMS is its tiered, hierarchical topology (Figure 1) with three subsystems, each with unique functions, as shown in Figure 2.

The cell interface provides tight management and monitoring of each battery cell in a stack; the system uses as many cell interfaces as needed, depending on the number of stacks. These interfaces can be daisy-chained as the number of cells and thus the stack voltage increases. The cell interface is connected to a single stack controller which monitors and manages multiple cell-interface units. Multiple stack controllers can be connected together, if needed, to support large packs with many stacks in parallel. The power interface connects the stack controllers to high voltage/current lines and is the interface to the inverter/charger. It isolates high-voltage and high-current components of the stack physically and electrically from the other modules. It also powers the BMS directly from the battery stack, thus eliminating the need for any external power supplies for the BMS operation.

The modular and hierarchical architecture of the Nuvation BMS supports battery-pack voltages ranging up to 1250 VDC, using cell-interface modules each containing up to 16 cells, stacks with up to 48 cell-interface modules, and battery packs that contain multiple stacks in



LEFT Figure 1: The Nuvation Engineering battery management system is the interface between the AC power grid and an array of battery cells; it provides both sophisticated battery charging/discharge oversight as well as the DC/AC inverter function



Grid Storage 112s2p Single Stack with Inverter/Charger, Precharge & Contactors

Figure 2: The three major subsystems of the Nuvation BMS - cell interface, stack controller, power interface - comprise a modular, hierarchical design which results in scalability, robustness, and reliability across a wide range of power levels as shown in the block diagram (above) and physical realization (right)

parallel. The entire array assembly is managed as a single unit from the user's perspective.

Solid design also builds from the bottom up

Factors such as modular architecture, hierarchical topology, and error-aware design are essential to the integrity and expandability of the Nuvation BMS, but not enough. A successful implementation requires high-performance functional blocks to serve as the physical foundation.

That's why the LTC6804 Multicell Battery Monitor IC (Figure 3) plays a critical role in the Nuvation BMS implementation. It is expressly tailored for the needs of BMS systems and multicell designs, beginning with providing precise measurements on up to 12 battery cells stacked in series. Its measurement inputs are not ground-referenced, which greatly simplifies measurement of those cells, and the LTC6804 itself is stackable for use with higher-voltage arrays (and it also supports a variety of cell chemistries). It offers maximum 0.033 % error with 16-bit resolution, and needs just 290 ?s to measure all 12 cells in the stack. Such synchronized voltage and current measurements are critical to yield meaningful analysis of power parameters.

Of course, performance in the benign environment of a prototype at the bench is not the same as actual achievable performance in an electrically and environmentally hostile real-world BMS setting. The LTC6804's analog/digital converter (ADC) architecture is designed to resist and minimize those detrimental effects, using filters specifically designed for the noise of power inverters.

The data interface uses a single twisted-pair, isolated SPI interface which supports rates up to 1 Mb and distances of up to 100 m. To further enhance system integrity, the IC Includes an array of ongoing subsystem tests. As further indication of its reliability and ruggedness, the LTC6804 meets the stringent AEC-Q100 standard for automotive quality. This IC achieves its results due to an application-specific design which focuses closely on BMS issues and environments, including the unique system-level objectives of the application and its many challenges.

Three major issues resolved

The LTC6804 addresses three major areas which affect system performance, conversion accuracy, cell balancing, and connectivity/data-integrity considerations:

1) Conversion accuracy: Due to the short- and long-term accuracy demands of the BMS application, it uses a buried-Zener conversion reference rather than a bandgap reference. This provides a stable,

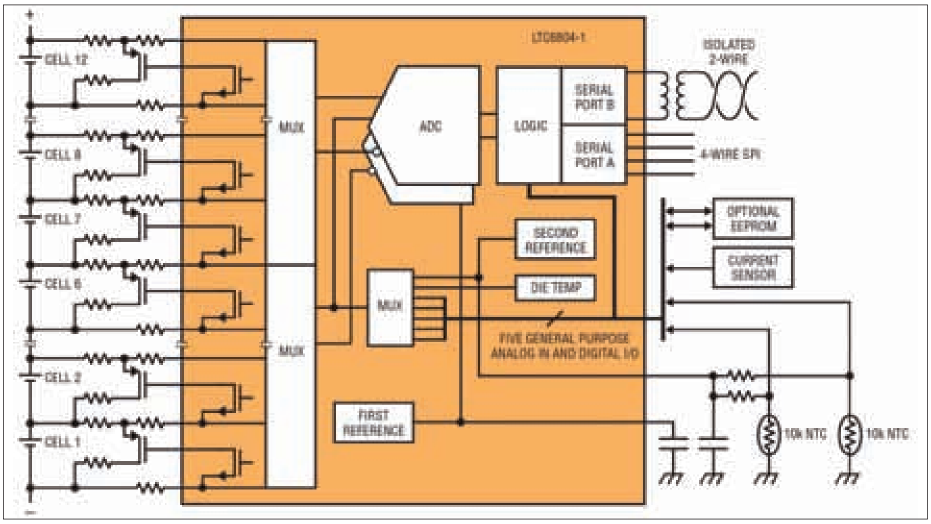


Figure 3: The LTC6804 Multicell Battery Monitor IC provides accurate, precise measurements on stacked battery cells, which are the starting point for a successful BMS implementation

low-drift (20 ppm/√kHr), low-temperature coefficient (3 ppm/K), low-hysteresis (20 ppm) primary voltage reference along with excellent long-term stability. This accuracy and stability is critical since it is the basis for all subsequent battery-cell measurements and these errors have a cumulative impact on acquired-data credibility, algorithm consistency, and system performance.

Although a high-accuracy reference is a necessary feature to ensure superior performance, that alone is not enough. The A/D converter architecture and its operation must meet specifications in an electrically noisy environment, which is the result of the pulse-width modulated (PWM) transients of the system's high current/voltage inverter. Accurate assessment of the state of charge (SOC) and health of the batteries also requires correlated voltage, current, and temperature measurements.

To mitigate the system noise before it can affect the BMS performance, the LTC6804 converter uses a delta-sigma topology, aided by six user-selectable filter options to address noisy environments. The delta-sigma approach reduces the effect of electromagnetic interference (EMI) and other transient noise, by its very nature of using many samples per conversion, with an averaging, filtering function.

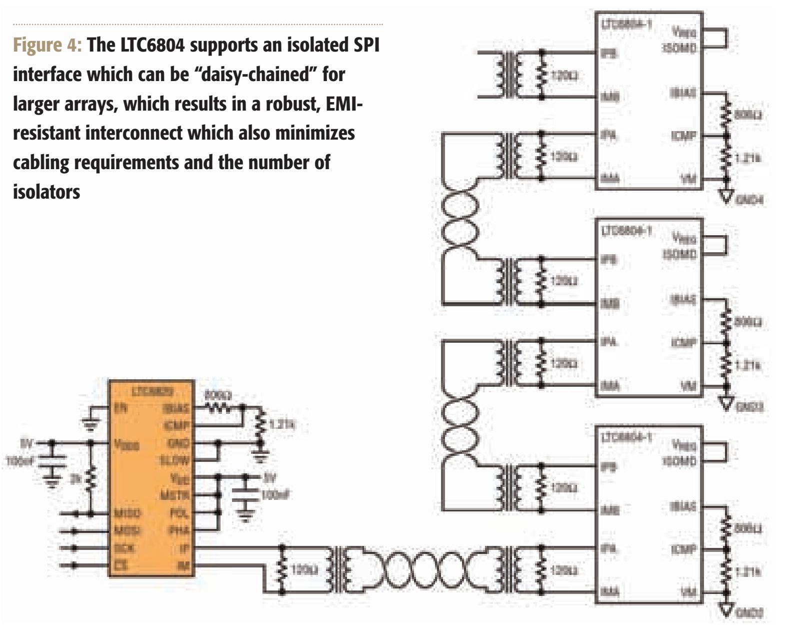
2) Cell balancing: The need for cell balancing is an unavoidable consequence in any system that uses large battery packs arranged as groups of cells or modules. Although most lithium cells are well matched when first acquired, they lose capacity as they age. The aging process can differ from cell to cell due to a number of factors, such as gradients in pack temperature. Exacerbating the whole process, a cell that is allowed to operate beyond its SOC limits will prematurely age and lose additional capacity. These differences in capacity, combined with small differences in self-discharge and load currents, lead to cell imbalance.

To remedy the cell imbalance issue, the LTC6804 directly supports passive balancing (with a user-settable timer). Passive balancing is a low cost, simple method to normalize the SOC for all cells during the battery charge cycle. By removing charge from the lower capacity cells, passive balancing ensures these lower capacity cells are not overcharged. The LTC6804 can also be used to control active balancing, a more-complicated balancing technique which transfers charge between cells through the charge or discharge cycle.

Whether done using active or passive approaches, cell balancing relies on high measurement accuracy. As measurement error increases, the operating guardband which the system establishes must also be increased, and therefore the effectiveness of the balancing performance will be limited. Further, as the SOC range is further restricted, the sensitivity to these errors also increases. The LTC6804's total measurement error of less than 1.2 mV is well within system-level requirements.

3) Connectivity/data integrity considerations: Modularity in the battery-

Figure 4: The LTC6804 supports an isolated SPI interface which can be "daisy-chained" for larger arrays, which results in a robust, EMI-resistant interconnect which also minimizes cabling requirements and the number of isolators



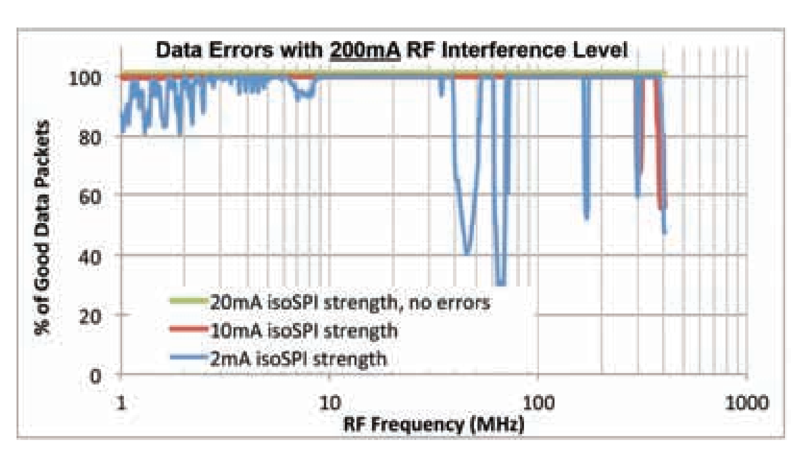


Figure 5: Test results on the LTC6804 and isoSPI interface showed no data errors despite 200 mA of injected RF with the isoSPI operating at 20 mA signal strength

pack design adds to scalability, serviceability, and form-factor flexibility. However, this modularity requires that the data bus between packs has galvanic isolation (no ohmic path), so failures in any one pack do not affect the rest of the system or put high voltages on the bus. Further, the wiring between packs must tolerate high levels of EMI.

A two-wire isolated data bus is a viable solution to achieve these goals in a compact and cost-effective way. Therefore, the LTC6804 offers an isolated SPI interconnect called isoSPI, which encodes the signals for clock, data in, data out, and chip select into differential pulses, which are then coupled through a transformer a rugged, reliable, and long-established isolation component (Figure 4).

Devices on the bus can be connected in a "daisy chain" configuration, which reduces harness size and enables modular designs for large, high-voltage battery packs, while maintaining high data rates and low EMI susceptibility (Figure 5).

To demonstrate the noise immunity, Linear Technology performed BCI testing on the LTC6804. This involved coupling 100 mA of RF energy into the battery-wiring harness, with the RF carrier swept from 1 MHz to 400 MHz and with 1 kHz AM modulation on the carrier. The LTC6804 digital filter was programmed for a 1.7 kHz cutoff frequency, and an external RC filter and ferrite choke were added as well. The result: the error in voltage reading was below 2 mV over the entire RF sweep range.

An array of self-assessment and self-test features adds to the suitability of the LTC6804 for BMS applications. These checks include open-wire detection; a second internal reference for ADC clock; multiplexer self-test, and even measurement of its internal power-supply voltages. The device is engineered for systems that are intended to be compliant with ISO 26262 and IEC 61508 standards.

Conclusion

There's a lot of "glamour" associated with backup and carry-through supplies for grid-level systems. It seems so straightforward: just keep an array of batteries charged (whether from the grid-AC line, or solar, wind, or other renewable sources), then use the batteries with a DC/AC inverter when you need to provide line-equivalent AC power. The reality is that batteries are not "simple" in any of their behavior or performance characteristics, and they need carefully controlled charging, monitoring of their voltage, current, and temperature, and discharging. As power levels increase, a practical, efficient, and safe system is not a trivial design, and so a grid-connected multicell BMS is a complex system. Many unique problems need to be understood and addressed, with safety a major concern as well. A successful and viable system design needs a modular, structured, top-down architecture that is supported from bottom up by optimized components such as the LTC6804. When combined with sophisticated, secure data-acquisition and control software, the result is a high-performance, reliable BMS that requires minimal operator involvement, and will function autonomously for years of reliable service.

Improved Battery Stack Monitor

Linear Technology announced end of 2015 the LTC6811 high voltage (75 V) battery stack monitor, a drop-in replacement for the former introduced LTC6804 with higher performance and 25 % lower price. The LTC6811 is a complete battery measuring IC for hybrid/electric vehicles that incorporates a deep buried Zener voltage reference, high voltage multiplexers, 16-bit delta-sigma ADCs and a 1 Mbps isolated serial interface. An LTC6811 can measure up to 12 series-connected battery cell voltages with better than 0.04 % accuracy. With 8 programmable 3rd order low pass filter settings, the LTC6811 provides outstanding noise reduction. In the fastest ADC mode, all cells can be measured within 290 µs.

For large battery packs, multiple LTC6811s can be interconnected and operated simultaneously, using a proprietary 2-wire isoSPI™ interface. This built-in interface provides electrically isolated, high RF noise immune communication for data rates up to 1 Mbps. Using twisted pair, many LTC6811s can be connected in a daisy chain to one host processor, enabling the measurement of hundreds of cells in high voltage battery stacks. The LTC6811 is specified for operation from −40°C to 125°C. It has been engineered for ISO 26262 (ASIL) compliant systems with extensive fault coverage via its redundant voltage reference, logic test circuitry, cross-channel testing, open wire detection capability, a watchdog timer and packet error checking on the serial interface.

For existing designs using LTC6804 battery stack monitor, the LTC6811 is a drop-in replacement with additional filter cutoff frequencies, added passive and active balancing control features, new ADC commands and enhanced fault coverage for functional safety. The LTC6811 is supported by Linear's Linduino™ technology, an Arduino-based microcontroller board and software library. The microcontroller board includes an electrically isolated USB port and directly connects to the LTC6811 demonstration board, providing a simple platform for evaluating and developing the application. The LTC6811 is offered in a 8 mm x 12 mm surface mount SSOP package. Priced at $8.19 each in 1,000-piece quantities, samples and demonstration boards are available at www.linear.com/product/LTC6811.

Testing Power Electronic Systems Efficiently

With today's increased incorporation of power electronics and switching devices in overall system design, there is a growing need for accurate measurement of both the power behavior of the applied power electronics and other inter-related electrical and physical parameters. **Clive Davis, Marketing Manager, Test and Measurement, Yokogawa Europe & Africa**

It may be surprising to learn that there is no accredited traceability for power measurement calibration anywhere in the world above 200 kHz. Indeed there are only five calibration laboratories which can perform ISO 17025 accredited power calibrations at 100 kHz. This naturally affects the validity of power measurements, particularly in switching applications where higher frequencies are present. There are a variety of products available to measure power, the selection of which will depend on a number of factors, including the stage of the development of the power electronics product and the desired accuracy of the measurement.

Architecture and design

At the architecture and design stage, we are considering the development of individual parts, and measurements include characteristics such as fast inverter switching, high-frequency dynamic behavior, overshoot on pulses, and the need to trigger on individual waveforms. A mixed-signal oscilloscope with up to eight input channels to view input and output signals in three-phase systems can be used to make these measurements (Figure 1). With a waveform-displaying product, such as an oscilloscope, it can seem easier to understand power measurement as even standard measuring features can be used to derive the value of active power. However, consideration must be given to both the accuracy and the stability of the measurement. Accuracy specifications of oscilloscopes do not include those for power measurement and generally do not even include any for AC voltage measurements.

So, although IGBT and SiC MOSFET switching losses, for example, can be measured using dedicated oscilloscope features, the absolute accuracy is not specified, and it is difficult to estimate the errors. Possible sources of error include the inaccuracy of the scope, the inaccuracies of the probes and the phase differences between them. In power measurement, phase differences can be a major source of error. The error from phase differences can be reduced, however, by using the automatic probe anti-skew feature if available. Thus, by paying attention to the measurement and perhaps using a reference circuit, an oscilloscope can indeed be used to judge if a circuit modification has increased or reduced the losses.

Verification and prototyping

The next stage is verification and prototyping, at which the individual parts

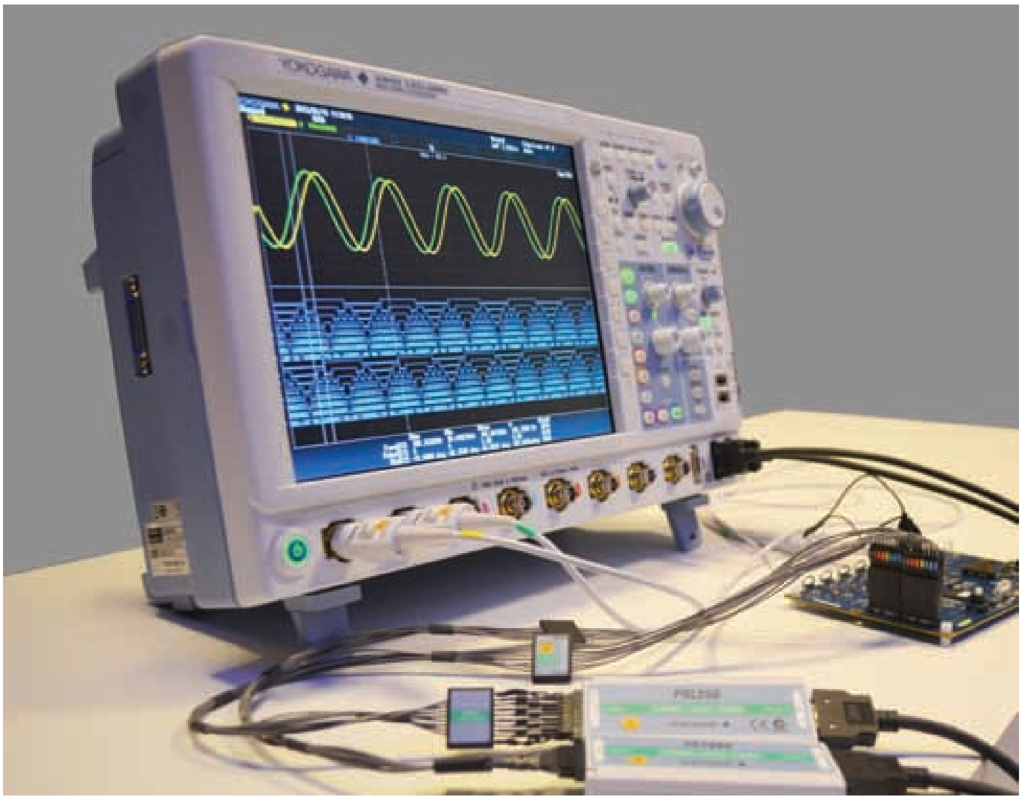


Figure 1: The DLM4000 mixed-signal oscilloscope offers up to eight input channels to view input and output signals in three-phase systems

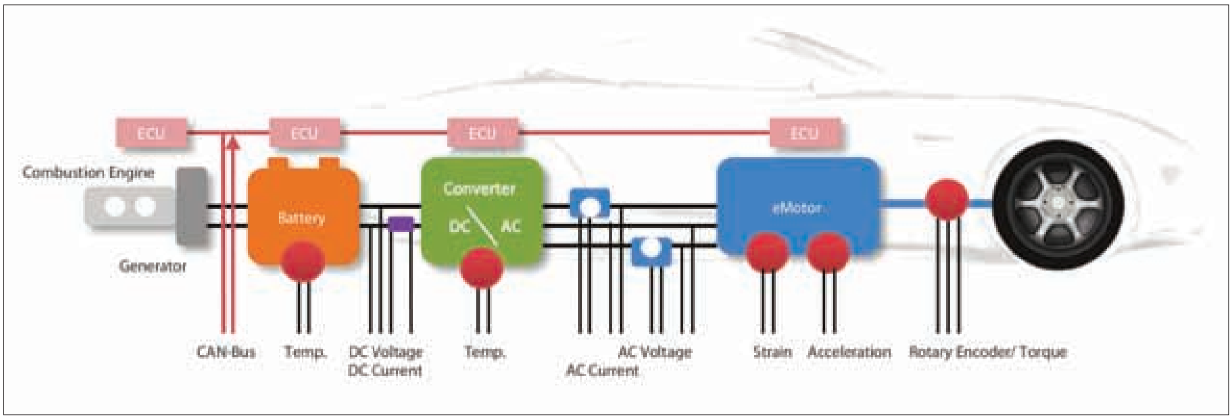


Figure 2: **Schematic of an electric car drive train, illustrating the various signals that need to be measured at the verification and prototyping stage**

are combined and form the system under test. To understand the dynamics of the application requires the measurement and analysis of a combination of electrical, mechanical and physical signals and, in automotive applications, signals from buses such as CAN and LIN (Figure 2). For this type of measurement, ScopeCorders are used. As a portable data acquisition recorder, a ScopeCorder can capture and analyze both transient events and trends for long periods. Using flexible modular inputs, it can combine measurements of electrical signals, physical parameters from sensors and CAN and LIN serial buses, and can trigger on electrical power related and other calculations in real time.

Efficiency validation

In the efficiency validation stage, the key factors that need to be tested are power analysis, conversion efficiency, harmonics and, for instance, the battery charge and discharge process. For tests of this type, the instrument of choice is the power analyzer, offering high precision, high accuracy, high stability, and the ability to carry out calibrated measurements. A key difference therefore between an oscilloscope type product and a power analyzer is that a power analyzer is fully specified for power measurement and voltages and currents are connected directly.

At this point, in order to select an appropriate instrument, the user also needs to consider what absolute accuracy is required for the power measurements, the frequencies in the signal and how this accuracy is proven. Where small improvements in input/output efficiency are being sought, for example for PV inverters, where efficiencies are typically 95 to 98 %, small improvements can only be recognized if the accuracy of the measuring instrument is at the highest level. With an ISO 17025 accredited calibration at frequencies up to 100 kHz, it is possible to not only prove the specified accuracy but also achieve much better performance than the specification (Figure 3).

Hybrid instruments

In addition to the dedicated instruments described above, engineers and R&D professionals are also looking for hybrid instruments that can be used at all stages of the development cycle. When the power consumed by the load varies – for example during the start-up of a motor – it may be necessary to measure power at much shorter intervals. A specific requirement is to provide the time-based measurement functionality of an oscilloscope combined with the accuracy of a power analyzer (Figure 4). Instruments such as precision power scopes provide users with flexibility, accuracy and wide bandwidth, allowing them to draw together the range of power readings needed to optimize the efficiency of boost circuits and inverters – two key elements in overall electric vehicle

Figure 3: **The WT3000 precision power analyzer**

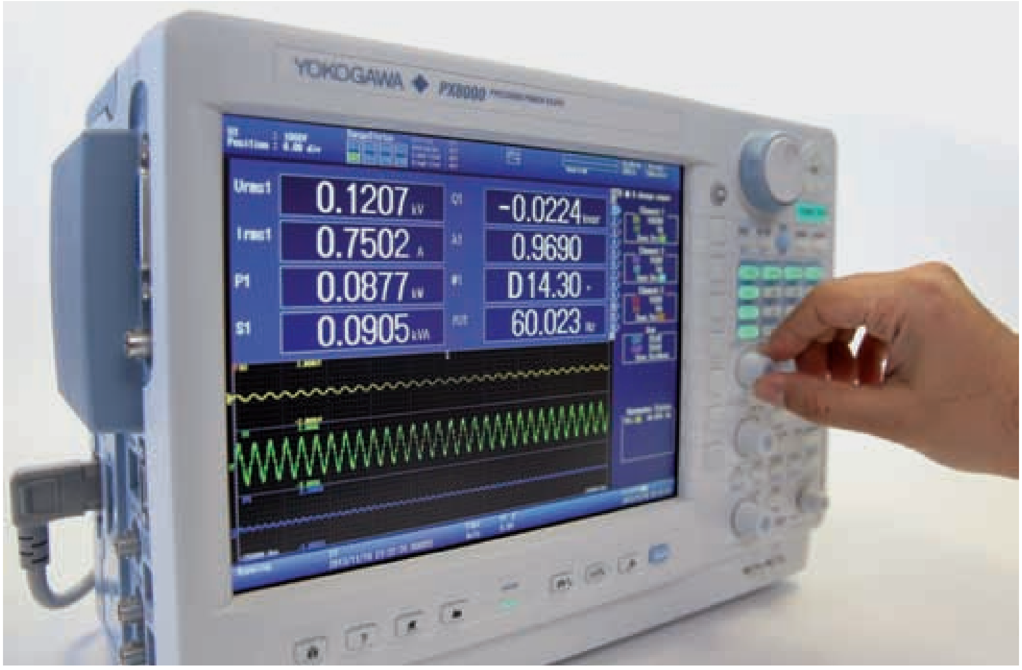


Figure 4: **The PX8000 Precision Power Scope**

performance.

Like a power analyzer, a precision power scope is capable of accurately measuring steady-state power and related variables, since they share the same input techniques and measurement principles. However, as it also shares characteristics of oscilloscopes and ScopeCorders, it is capable of capturing and measuring the power arbitrarily over any part of the power waveform using start and stop cursors. This is particularly useful for examining transient phenomena and in the design of periodically controlled equipment. The trigger functionality helps to set various trigger conditions based on the analysis of the transient phenomena to understand the behavior of the system under test. During the start-up phase of an inverter and motor in an electric or hybrid car, for example, current increases can be analyzed in each cycle (Figure 5). And, when the load changes rapidly, the engineers can gain insights that will enable them to improve the control of the inverter.

The need for calibration

As more and more innovation focuses on energy efficiency and the use of renewable energy resources, engineers are increasingly demanding accuracy and precision from their power measurements. At the same time, new standards such as IEC62301 Ed2.0 and EN50564:2011, covering standby power consumption, and the SPEC guidelines, covering power consumption in data centers, demand more precise and accurate testing to ensure compliance.

To meet these challenges, R&D teams are coming to terms with the need for new levels of precision in power measurement, but these levels of precision can only be achieved if the measuring instruments are properly calibrated with reference to national and international standards.

Regular calibration by a laboratory, which can provide very low measurement uncertainties at the specific measurement points applicable to individual users, should enable instrument makers and their customers to have confidence in their test results.

Laboratories that are accredited to ISO 17025 (General requirements for the competence of testing and calibration laboratories), however, have demonstrated that they are technically competent and able to produce precise and accurate calibration measurements. Yokogawa's European Calibration Laboratory is the only industrial (i.e. non-government or national) organization to offer traceability up to 100 kHz, and makes it the only power meter manufacturer which can directly prove the performance of its own instruments.

Literature

Clive Davis, Erik Kroon, "The Need for High-Frequency High-Accuracy Power Measurement", Power Electronics Europe 6/2015, pages 29 - 31

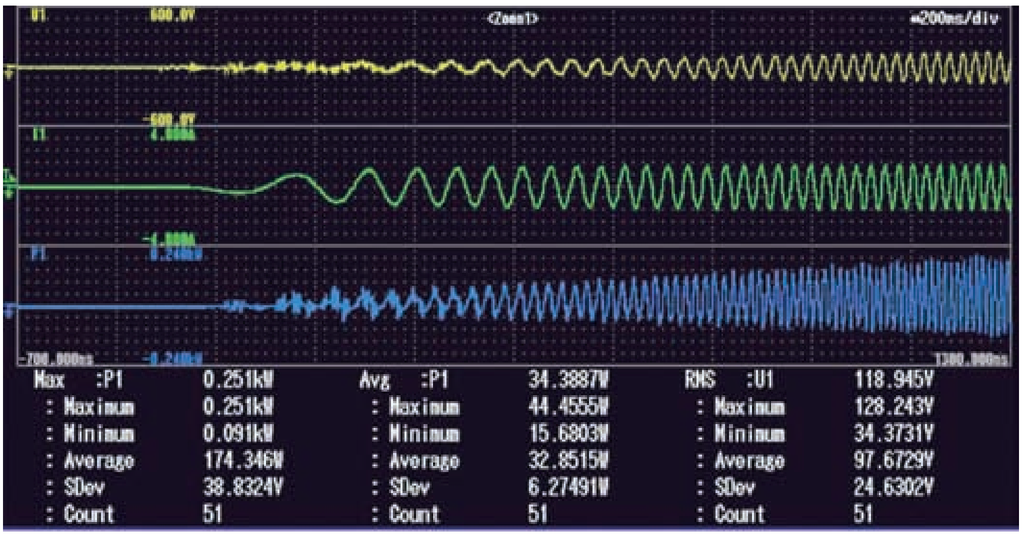


Figure 5: **During the start-up phase of an inverter and motor in an electric or hybrid car, for example, the Precision Power Scope allows current increases to be analysed in each cycle**

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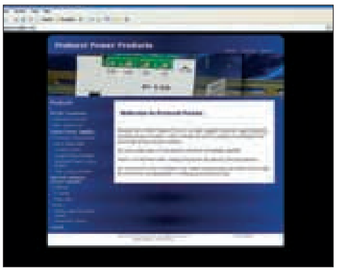

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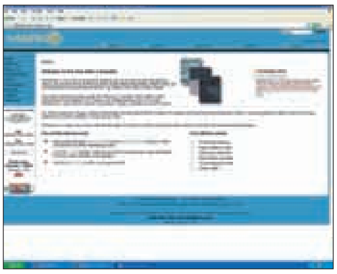

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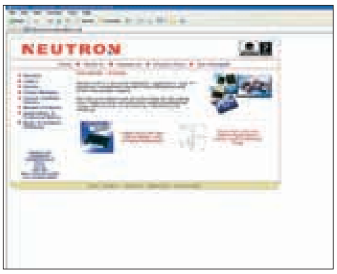

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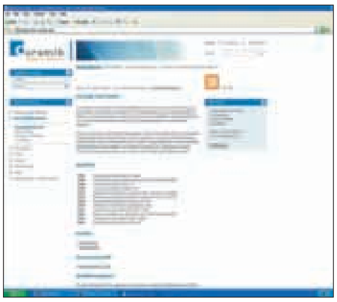

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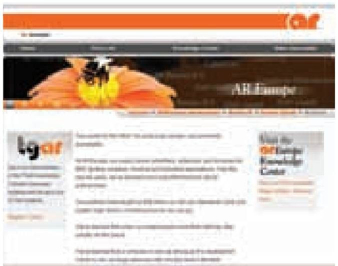

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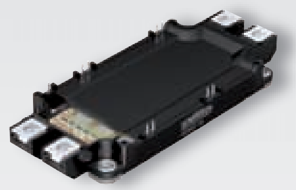
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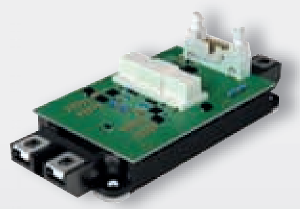
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