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POWER SEMICONDUCTORS

Low Temperature Silver Sintering Improves Reliability of Power Semiconductors

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Also inside this issue

Opinion | Market News | Industry News
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Power Modules | Automotive Power | Products | Website Locator

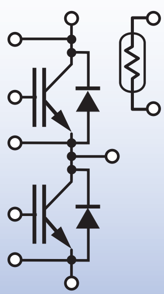
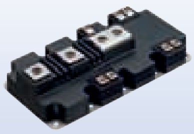
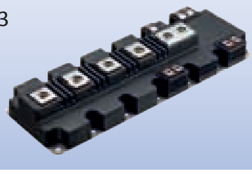
PrimePACK™ 7G IGBT MODULES

Upgrading to 1200A in PP2 and 1800A in PP3

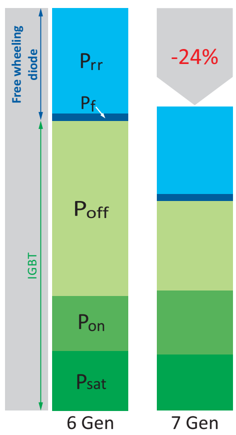
Main features of enhanced package design

- Low internal stray inductance
- CTI > 600
- Higher power cycling capability
- New silicone gel for high temperature operation
- Optimized thermal management
- Lower power losses by new X-Series chips
- Higher continuous operating temperature up to 175°C

Line-up

		1200V	1700V
	PP2 	900A	1200A
		1200A	
	PP3 	1400A	1400A
		1800A	1800A

Power Dissipation at 6kHz
6 Gen vs 7 Gen
Module rating: 1700V/1400A



PrimePACK™ is registered trademark of Infineon Technology AG, Germany.

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COVER STORY

Low Temperature Silver Sintering Improves Reliability of Power Semiconductors

Reliability and lifetime of power semiconductors can be improved by using low temperature sintering on silver-containing layers. It is worth mentioning this technology has many applications - from IGBTs, where this technology allows to ensure a reliable connection chip-DBC, DBC-substrate, DBC–power terminals, to SCR thyristors and their subtypes (PCT, BCT, GTO, etc) where it is required to ensure a reliable connection between the power chip and molybdenum thermal compensator. Sintering of high-powered single-chip thyristors and diodes experience is representing such advantages as improved cycling capacity, reduced thermal resistance, as well as increased surge current values. Moreover, the technology possesses significant benefit of the emitted layer surface injection index values. However, to achieve all the above listed advantages one must pay attention to several specific aspects. The sintering technology is based on principles of diffusion welding and plastic deformation of silver particles. The driving force of sintering is to store energy on the surface of silver particles. More details on page 25.

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Capacitors for Power Electronics

IGBT Snubbers
RF Mica Capacitors
DC Link Capacitors
-High Current, High Voltage Film
-High Capacitance Aluminum Electrolytic
AC Output Harmonic Filter Capacitors

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Events Promote Power Electronics

The recent event APEC 2017 and the upcoming PCIM Europe showed respective will show the growing role of power electronics and in particular power semiconductors in our daily life due to the rising penetration not only in industrial applications, but also in automotive, commercial and entertainment.

In 2016, 25 million electrified vehicles were sold. Power MOSFET sales in automotive applications have surpassed computing and data storage, now representing more than 20 % of the total market. As vehicle numbers increase worldwide and people adopt electrified vehicles, this sector's rapid growth will continue at 5.1 % copound annual growth rate (CAGR) between 2016 and 2022.

Today's trend is to increase the battery and the fix charger power. However, this trend limits the mass market for BEVs (battery electrical vehicle). The first PCIM keynote by Renault/Nissan will show some of these limits on the car point of view (battery cost/packaging/weight, uncertainty on specific material availability and environmental consideration). Game changer as charging during driving could solve these mass market car roadblocks. Charging during driving transfers an important investment part from BEV to infrastructure by reducing battery size or in other words transfers investment from the BEVs owners to the public. If we consider that 5000 Euros could be saved by reducing the needed battery size and if we consider 30 percent EVs to be sold each year, it would represent 3 billion Euros investment each year for road infrastructure only for a country like France. In any case, hundreds of billions will be needed though the world to equip the road in coherence with the high number of BEV expected from now to 2030.

Power MOSFETs are widely used in various automotive applications involving braking systems, engine management, power steering and other small motor control circuits, in which a low conduction loss and high commutation speed device is very much appreciated. Silicon power MOSFETs are also becoming increasingly popular in EV/HEV converters, depending on their electrification level. For battery chargers MOSFETs can handle roughly 3-6 kW, which is perfect for small size plug-in EVs or full EVs. They are also used for 48 V DC/DC converters and other micro inverters in the start/stop function module. With the trend of EV/HEV adoption led by Tesla, Analysts believe this market segment will become increasingly important in the next 5-10 years. Computing and storage market segment which includes desktops, laptops, as well as different kinds of servers in the datacenters comes to the second largest market. With the declining sales number of personal PCs this market segment is slowing down and has been surpassed by automotive part in 2016. However with the increasing demand for servers and datacenters, the whole segment is still having a steady increase, posting a 2.8 % CAGR for the 2016-2022 period. That's why not only the established manufacturers invest into new technologies, but also new market entries. At APEC 2017 a new start-up named D3 Semiconductor announced its entry into the power semiconductor market with the launch of 650 V (superjunction MOSFETs). The fabless Texas-based company claims to offer devices with lowest on-resistance and gate charge and will add mixed-signal functions into high-voltage switching devices.

According to a keynote given by Ahmad Bahai, Chief Technologist at Texas Instruments, the multi-directional flow of data is now also flowing in power. But power scaling is much less than in microprocessors, it is 20 percent in low-power LDOs and less than 10 percent in high power applications. Silicon Carbide and Gallium Nitride will improve this situation, in particular GaN is coming to the point that is it affordable for most applications. Nevertheless, technology development is much slower than Moore's law, it takes more or less ten years to implement new materials. At system level 5 percent price reduction and 50 percent performance increase can be gained. In data centers, GaN totem pole power factor correction and LLC can reduce volume by 30 percent, and direct conversion from 48 V to 1 V with GaN devices can improve efficiency by a factor 4. And GaN has the potential of using larger wafer sizes and thus cost reduction, what is not the case with SiC.

Market researchers estimate that WBG technologies represent only less than 2 percent of the overall power semiconductor market today but are showing a real growth potential in a near future. Ever more new companies are promoting SiC and GaN solutions and new designs. Analysts believe this will be the next technology evolution stage. GaN devices being implemented for high frequency switch applications in the low-to-mid voltage 100-200 V range, but remaining a small portion. Both SiC and GaN devices will penetrate the high frequency market around 600 V, but will probably only be popular in particular markets, like EV on-board chargers and data center power supply units.

Besides that we have provided more subjects in this issue – enjoy reading the following pages!

Achim Scharf
PEE Editor

Power MOSFET Market Still Growing By New Applications

In 2016, the MOSFET market recovered, after a minor downturn in 2015, according to market researcher Yole Développement. With stable growth, mainly in automotive and industrial sales in 2016 the overall Silicon power MOSFET market size surpassed 2014's performance. Overall market revenue neared $6.2 billion. From 2016 to 2022 Yole estimates a 3.4 % annual growth rate.

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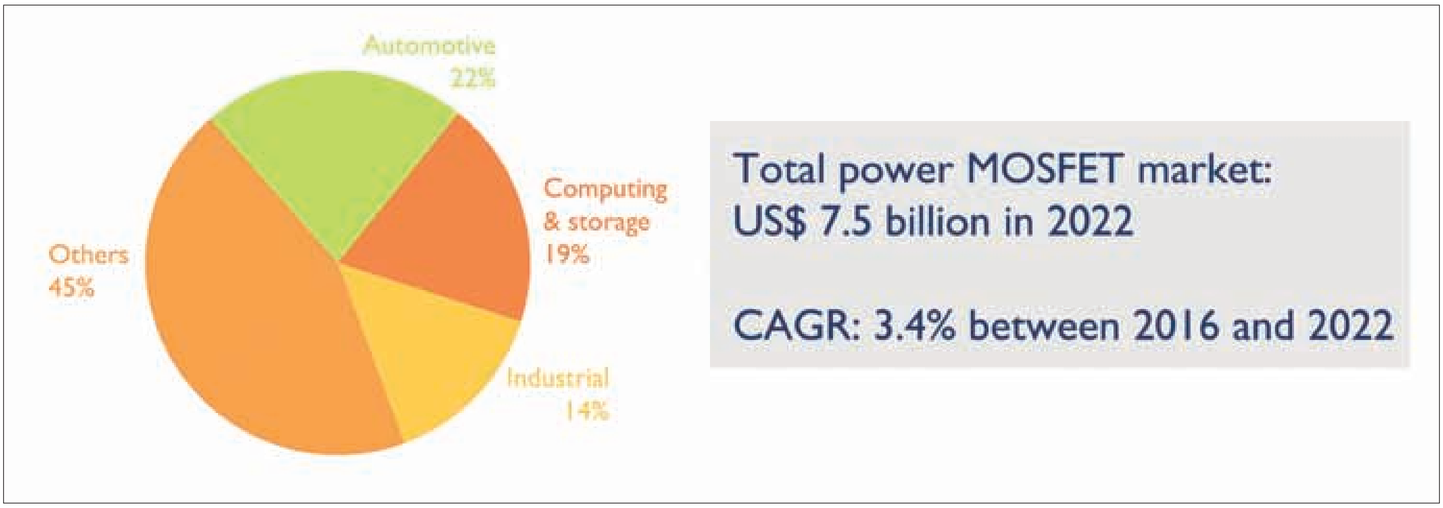
Computing and storage market segment which includes desktops, laptops, as well as different kinds of servers in the datacenters comes to the second largest market. With the declining sales number of personal PCs this market segment is slowing down and has been surpassed by automotive part in 2016. However with the increasing demand for servers and datacenters, the whole segment is still having a steady increase, posting a 2.8 % CAGR for the 2016-2022 period.

Power electronics market future may depend on governmental decisions concerning electrified vehicles as well as renewable energies applications. It includes carbon dioxide reduction targets, increased energy efficiency, etc. Both markets could be the most important in 2030, announces Yole in its MOSFET report. On the other hand, other large volume applications may come, such as 5G, drones or robots. All these applications, demanding power supply, will clearly push the MOSFET market. Today it is not possible to get a comprehensive understanding of the MOSFETs market without taking into account the impact of the innovative WBG technologies including SiC and GaN.

Silicon power MOSFETs have been developing for 20 years. Ceaseless improvement and technology innovations from planar to trench structure and today's superjunction, have reduced device sizes and costs dramatically - but today, device performance has reached Silicon's theoretical limit.

Chasing better performance and even smaller devices size, today the power electronics industry is at the beginning of SiC and GaN's adoption. Ever more new companies are promoting SiC and GaN solutions and new designs. At Yole, analysts believe this will be the next technology evolution stage. However, this does not necessarily mean doom for Silicon power MOSFETs. "Looking back at the development of bipolar transistors and power MOSFETs in the past 20 years in different applications, we expect that there will still be a very solid market share reserved for Silicon power MOSFETs", analyzes Zhen Zong from Yole. "With increasing need in the end applications, the overall market size for MOSFETs will not necessarily decline. Both SiC and GaN devices will penetrate the high frequency market around 600V, but will probably only be popular in particular markets, like EV on-board chargers and data center power supply units. The majority of the market will still use Silicon power MOSFETs, thanks to their proven reliability and good cost performance ratio."

www.yole.fr



Power MOSFET market in 2022 by application **Source: Yole Développement 4/2017**

ROHM and SEMIKRON Collaborate in Japan

ROHM and SEMIKRON will collaborateon sales of SiC power devices and modules, to contribute jointly to the evolution of the Japanese power electronics market.

ROHM (**www.rohm.com**) has been a leading developer of Silicon Carbide (SiC) products and SiC power devices in particular. It was the first company to manufacture the SiC MOSFET in 2010 and offers SiC Schottky diodes as well. The wide range of SiC chips is suitable for an easy module integration. SEMIKRON (**www.semikron.com**) is one of the market leaders in power modules, covering a wide range of packages for all applications. It is well known for its packaging technology that has set standards in power electronics. SEMIKRON offers SiC modules in six different packages covering 20 A to 600 A, which are widely used in the world-wide power electronics market, enabling energy savings in various applications. Both companies together will synergize their joint knowledge (about device, control and module technology) to widen the SiC power module line-up and contribute to energy saving and miniaturization. “We are convinced that SEMIKRON is offering a good fit to our SiC technology and can implement our SiC chips into the right package, suiting the application requirements. We see SEMIKRON as one of our enabling partners for market development of SiC thanks to their system and application understanding”, commented Kazuhide Ino, General Manager Power Device Division at ROHM. “By utilizing ROHM’s highly efficient SiC components we can offer designed-to-fit application specific SiC power modules, matching the customer’s requirements in terms of performance and cost. Our line-up of SiC power modules spans a wide spectrum of packages suitable for all power conversion applications such like renewable energy and energy storage, chargers for electric vehicles and more traditional markets, e.g. auxiliary power supply for transportation and UPS”, stated Erwin Ysewijn, Managing Directror SEMIKRON Japan.

SEMIKRON’s Managing Director Japan Erwin Ysewijn (left) and Kazuhide Ino, General Manager Power Device Division, ROHM Co., announcing their collaboration in Japan

Power Integrations Still On Track

“We believe the 2016 big-picture themes such as energy efficiency, faster charging for mobile devices, smarter homes and appliances, and more – will remain operative not just for 2017 but also for the foreseeable future”, said Power Integrations CEO Balu Balakrishnan

Net revenues for the fourth quarter were $101 million, an increase of 16 percent from the fourth quarter of 2015. Power supply applications and IGBT drivers contributed to this growth.

“For the full year 2016, our revenues grew by 13 percent up to $387.4 million – more than twice the growth rate of the analog semiconductor industry. We also introduced new products broadening our portfolio of ICs for the power-supply, LED-lighting and IGBT-driver markets and increasing our served addressable market (SAM) to more than $3 billion. With a robust pipeline of new products still to come in 2017 and beyond, we believe our SAM will soon exceed $4 billion, giving us ample opportunity to grow for the foreseeable future. Moreover, we believe the big-picture themes that underpinned our growth in 2016 – energy efficiency, faster charging for mobile devices, smarter homes and appliances, and more – will remain operative not just for 2017 but for years to come”, commented CEO Balu Balakrishnan.

While the drivers of last year’s growth are continuing into 2017 and beyond, Balakrishnan also expects to layer on new revenue streams in the very near future. InnoSwitch products have already made a mark on the mobile-phone industry, but are now being designed into a wide range of other power-supply applications such as appliances, networking gear, and numerous industrial applications, at higher average selling prices. The next-generation ICs will address higher power levels than the first generation, bringing the benefits to an even wider range of applications, including TVs, computer monitors, power adapters for notebook computers and many more.

"Our new IGBT SCALE-iDriver family, introduced last May, is the first product arising from the combination of our low-power technology and our IGBT-driver technologies. This new product family, which incorporates the Fluxlink technology that lies at the heart of our InnoSwitch products, addresses IGBT-driver applications up to 100 kilowatts, including industrial motor drives, medical equipment and commercial solar installations. Longer term, this product family will also enable us to compete in the automotive market, where the growth of the electric vehicle market is creating a need for highly reliable, energy-efficient power electronics for drive trains and charging stations."

The SCALE-2 IGBT gate drivers are suitable for driving power MOSFETs and devices based on new materials such as silicon carbide (SiC) operating at switching frequencies up to 500 kHz. IGBT drivers as a result of the CT Concept acquisition in 2012 already accounts for ten percent of the company's revenues. **AS**

www.power.com

SCALE-2 IGBT Gate Drivers Now at Mouser

Mouser Electronics is now stocking the SCALE-2 IGBT gate drivers from Power Integrations. These extremely flexible IGBT gate driver cores integrate commonly required driver functions – including galvanic isolation, protection, and DC/DC conversion – in a single module.

The gate drivers are based on an ASIC chipset that integrates the full functionality of a dual-channel gate driver core in a primary-side chip logic-to-driver interface (LDI) and a secondary-side chip intelligent gate driver (IGD). The highly integrated level of the ASIC chipset enables the number of discrete components to be drastically reduced, resulting in cost and reliability advantages for designers. The modules are available with blocking voltage capabilities from 600 V to 6500 V and from 1 W to 20 W per channel. To ensure optimum performance for direct driving of external N-type DMOS elements, the pre-driver stages of each of the modules incorporate separate gate resistors for independent control of on/off functionality.

www.mouser.com/new/Power-Integrations/power-integrations-scale-2-igbt/

98 Percent Efficient PFC Designs Up to 550 W

The new HiperPFS-4 ICs from Power Integrations incorporate a 600 V MOSFET suitable for 305 V AC input and a high efficiency, variable frequency, CCM PFC controller in a single, compact, electrically isolated, heatsinkable package. The IC family delivers high power factor, low THD and uniformly high efficiency across a wide output load range, allowing OEMs to meet the demanding 80 PLUS® Platinum and Titanium power supply standards.

HiperPFS-4 ICs achieve a high power factor above 0.95 and low THD even at 20 % of rated load. The devices also meet the stringent surge requirements such as the 1 second 410 V AC input test, which ensures field reliability and robustness against voltage swells and surges. The ICs suit enclosed designs up to 300 W, open frame power supplies of up to 400 W and highline applications up to 550 W. Protection features include UVLO, UV, OV, OTP, brown-in/out, cycle-by-cycle current limit and power limit. The ICs consume less than 60 mW at 230 VAC while regulating output at no-load and less than 20 mW in sleep mode and are available in thermally-efficient eeSIP packaging, which simplifies heatsink mounting. Devices cost $1.46 in 10,000-piece quantities.

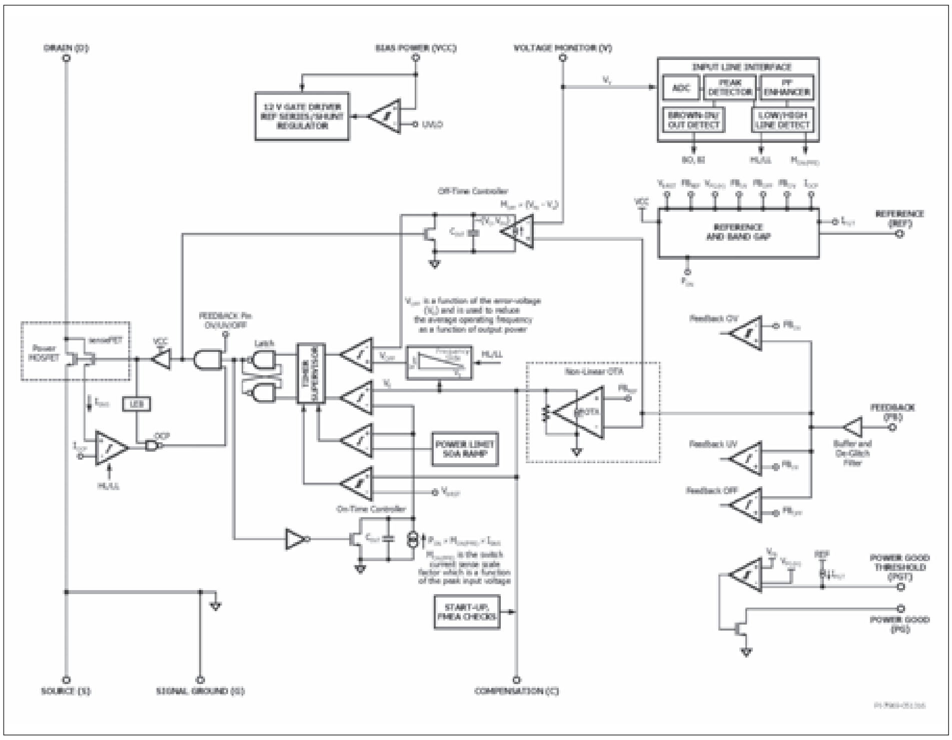
New PFC IC for high-voltage power supplies

Functional description

The devices incorporate a continuous conduction mode (CCM) boost PFC controller, gate driver and 600 V power MOSFET. External current sense resistors with their associated power loss are not required. An innovative control technique adjusts the switching frequency over output load, input line voltage, and input line cycle. This control technique maximizes efficiency over the entire load range, particularly at light loads. Additionally, it minimizes the EMI filtering requirements due to its wide bandwidth spread spectrum effect. Digital techniques are used for line monitoring, line feed-forward scaling, and power factor enhancement; while analog techniques are used for the core controller in order to maintain extremely low no-load power consumption. The HiperPFS-4 also features an integrated non-linear error amplifier for enhanced load transient response, a user programmable Power Good (PG) signal as well as user selectable power limit functionality.

HiperPFS-4's variable frequency continuous conduction mode operation (VF-CCM) minimizes switching losses by maintaining a low average switching frequency, while modulating the switching frequency in order to suppress EMI, the traditional challenge with continuous conduction mode solutions. HiperPFS-4 typically reduce the total X and Y capacitance requirements of the converter, the inductance of both the boost choke and EMI noise suppression chokes.

Many regions mandate high power factor for many electronic products with high power requirements. These rules are combined with numerous application-specific standards that require high power supply efficiency across the entire load range, from full load to as low as 10 % load. High efficiency at light load is a challenge for traditional PFC solutions where fixed MOSFET switching frequencies cause fixed switching losses on each cycle, even at light loads. In addition to featuring flat efficiency across the load range, HiperPFS-4 also enables a high power factor of >0.95 at 20 % load. Compliance with new and emerging energy-efficiency standards over a broad market space in applications such as PCs, LCD TVs, notebooks, appliances, pumps, motors, fans, printers and



Functional block diagram of HiperPFS-4

KNOWLEDGE IS POWER

Massive power density in the smallest packages

Microchip Technology now offers an integrated switching power module designed specifically for height-constrained telecom, industrial and solid-state drive (SSD) applications. These products come in an impressive thermally-enhanced package that incorporates inductors and passive components into a single, molded power converter. The slim packages simplifies board design, saves space and eliminates concern over passive components that may introduce unexpected electromagnetic interference (EMI).

Highlights

- Variety of module package offerings (small to large, fit to application)
- High power density with integrated magnetic and passive components
- Performance (efficiency, thermal, transient response)
- Reliable (power and thermal stress tested)
- Low EMI (CISPR 22 Class B ratings on modules)

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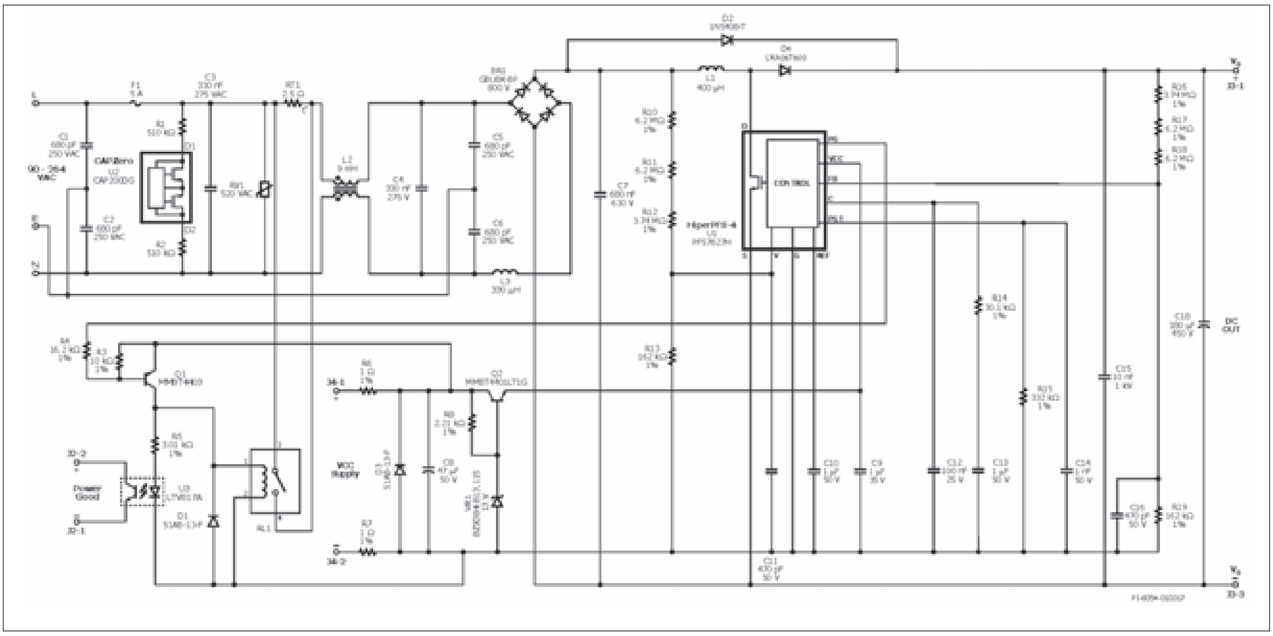

275 W PFC reference design

LED lighting is simplified.

The power packaging technology and high efficiency simplify the complexity of mounting the IC and thermal management, while providing very high power capabilities in a single compact package; these devices are suitable for PFC applications with maximum continuous power from 75 W to 405 W universal (550 W high-line only).

Design for high bus voltage

A reference design is rated for a continuous output power of 275 W and provides a regulated output voltage of 385 VDC nominal, maintaining a high input power factor and overall efficiency from light load to full load. Fuse F1 provides protection to the circuit and isolates it from the AC supply in the event of a fault. Diode bridge BR1 rectifies the AC input voltage. Capacitors C1-C7 together with inductors L2 and L3 form the EMI filter which reduces the common mode and differential mode noise. Resistors R1, R2 and CAPZero-2, IC U2 are required to discharge the EMI filter capacitors once the circuit is disconnected.

CAPZero-2 eliminates static losses in R1 and R2 by only connecting these components across the input when AC is removed. Metal oxide varistor (MOV) RV1 protects the circuit during line surge events by effectively clamping the input voltage seen by the power supply.

Inductor L1 and boost diode D4 in conjunction with HiperPFS-4 IC U1, form the boost converter stage, controlling the input current of the power supply while simultaneously regulating the output DC voltage. Diode D2 prevents a resonant buildup of output voltage at start-up by bypassing inductor L1 while simultaneously charging output capacitor C18.

Thermistor RT1 limits the inrush input current of the circuit at start-up and prevents saturation of L1. However in the highest efficiency designs, an electro-mechanical relay RL1 will be used to bypass the thermistor once the output voltage is in regulation as indicated by a power good signal (asserted low). Resistors R3 and R4, and transistor Q1, drive relay RL1 and optocoupler U3. Diode D1 clamps the relay coil reverse voltage during de-assertion transitions. Resistor R5 limits the current to the diode in the optocoupler. IC U3 provides optocoupler isolation through connector J2 for a power-good output signal if required.

Capacitor C15 is used for reducing the loop length and area of the output circuit to reduce EMI and overshoot of voltage across the drain and source of the MOSFET inside U1 at each switching edge.

The PFS7627H IC requires a regulated supply of 12 V for operation (15 V max). Resistors R6, R7, R8, Zener diode VR1, and transistor Q2 form a series pass regulator that prevents the supply voltage to IC U1 from exceeding 15 V. Capacitors C8, and C9 filter the supply voltage and provide bypassing and decoupling to ensure reliable operation of IC U1. Diode D3 provides reverse polarity protection. Resistor R15 programs the output voltage level [via the POWER GOOD THRESHOLD (PGT) pin] below which the POWER GOOD [PG] pin will go into a high-impedance state. Capacitor C14 provides noise immunity on the POWER GOOD THRESHOLD pin. IC U1 is configured in full power mode by capacitor C10 which is connected to the REFERENCE pin.

The rectified AC input voltage of the power supply is sensed by IC U1 using resistors R10-R13. These resistors values are large to minimize power consumption. Capacitor C11 connected in parallel with the bottom resistor R13 filters noise coupled into the VOLTAGE MONITOR pin.

Output voltage divider network comprising resistors R16 – R19 are used to scale the output voltage and provide feedback to the IC. Capacitor C16 in parallel with resistor R19 attenuates high frequency noise. Components R14, C12 and C13 are required for shaping the loop response of the feedback network.

275 W PFC reference design board

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Digitally Enhanced Power Analog Solution for DC/DC Power Conversion

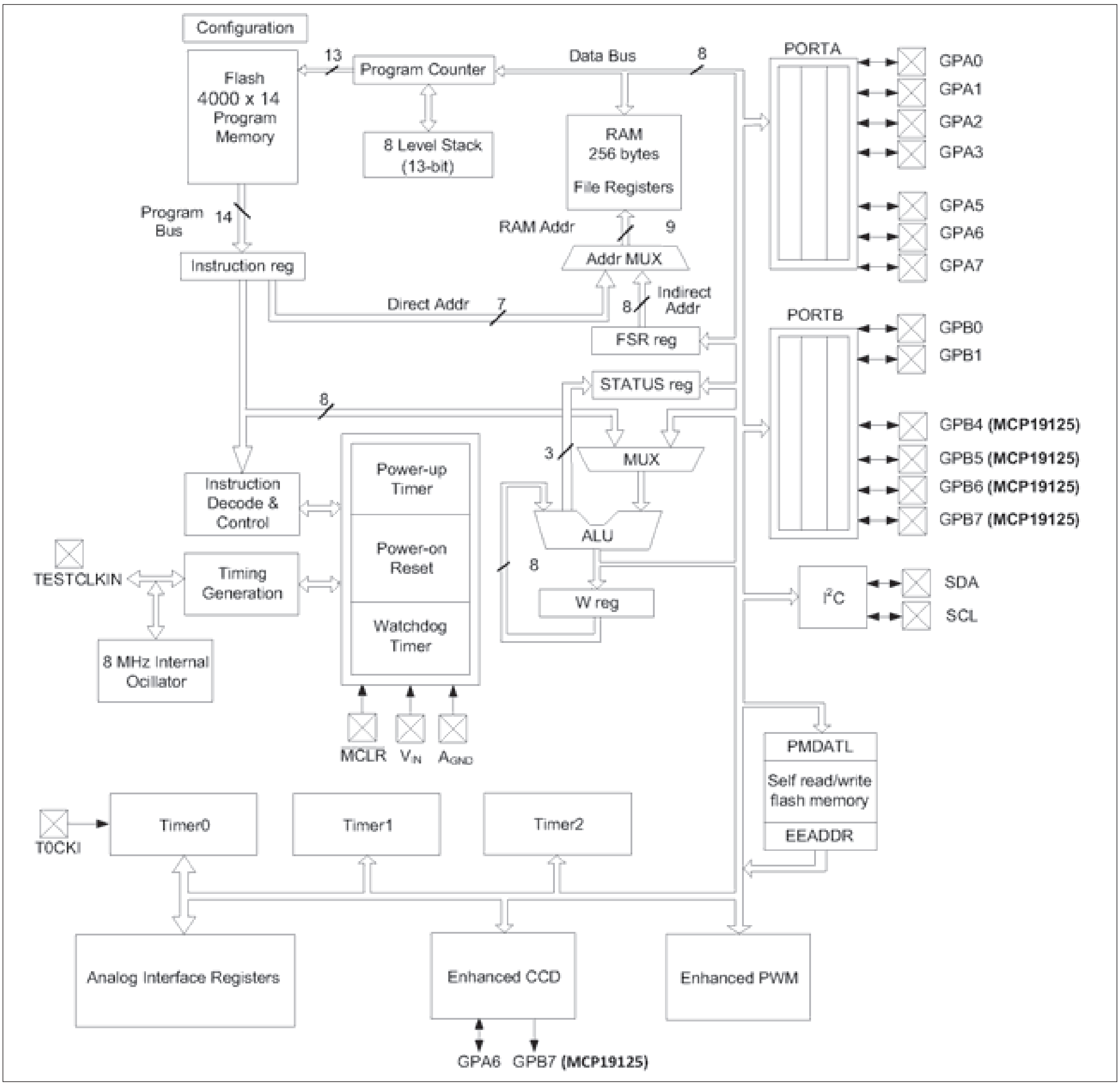
A new Digitally Enhanced Power Analog controller (MCP19215) from Microchip for DC/DC power conversion is capable of high voltage input while simultaneously regulating a wide output voltage range from 300 mV to several hundred volts, depending on topology. The device also features low quiescent current sleep modes and the ability to survive load dump transient conditions, making it ideal for automotive applications. The device can be programmed to shut down other loads and enter sleep mode, allowing direct connection to the battery with minimal power consumption when the engine is not running.

The MCP19124/5 are highly integrated, mixed-signal low-side synchronous controllers that operate from 4.5V to 42V. The family features individual analog PWM control loops for both current regulation or voltage regulation. These features along with an integrated microcontroller core make this a device used for battery charging applications, LED lighting systems and any other low-side switch PWM applications.

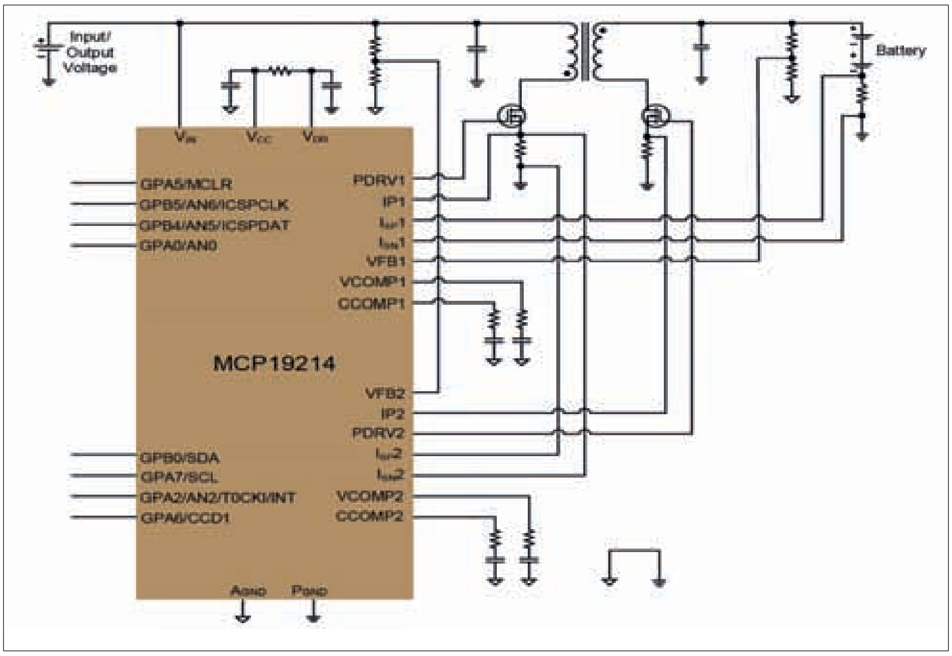
Supporting many topologies

The MCP19124/5 devices are derived from the MCP19114/5 Enhanced PWM Controllers with the exception of some additional features along with an additional analog control loop designed for voltage regulation. Complete customization of device operating parameters, start-up or shutdown profiles, protection levels and fault handling procedures are accomplished by setting digital registers using MPLAB¬Æ X software and one of in-circuit debugger and device programmers.

The MCP19124/5 mixed-signal low-side synchronous controllers feature integrated programmable input UVLO/OVLO, programmable output overvoltage (OV), two low-side gate drive outputs with independent programmable dead time, programmable leading edge blanking (four steps), programmable 6-bit slope compensation and an integrated internal programmable oscillator for fixed-frequency applications. If users decide to regulate voltage via EA2 voltage error amplifier and control loop, the output OV is disabled. An integrated 8-bit reference voltage (V_{REF}) is used for setting output current. A separate integrated 8-bit reference voltage (OV_{REF}) is used to set the voltage regulation set point or the over-voltage protection set point. An internal comparator supports quasi-resonant applications. Additional Capture and



Microcontroller core block diagram



Schematic of a bidirectional converter

Compare modules are integrated for additional control, including enhanced dimming capability.

The MCP19124/5 devices contain two internal LDOs. A 5V LDO (V_{DD}) is used to power the internal processor and provide 5 V externally. A 4 V LDO (AV_{DD}) is used to power the internal analog circuitry. Either V_{DD} or AV_{DD} can be connected internally to the 10 bit Analog-to-Digital Converter reference input. The 5 V external output can be used to supply the gate drive. An analog filter between the V_{DD} output and the V_{DR} input is recommended when implementing a 5 V gate drive supplied from V_{DD}. Two 4.7 µºF capacitors are recommended with one placed as close as possible to V_{DD} and one as close as possible to V_{DR}, separated by a 10 Ω isolation resistor. An external supply is required to implement higher gate drive voltages.

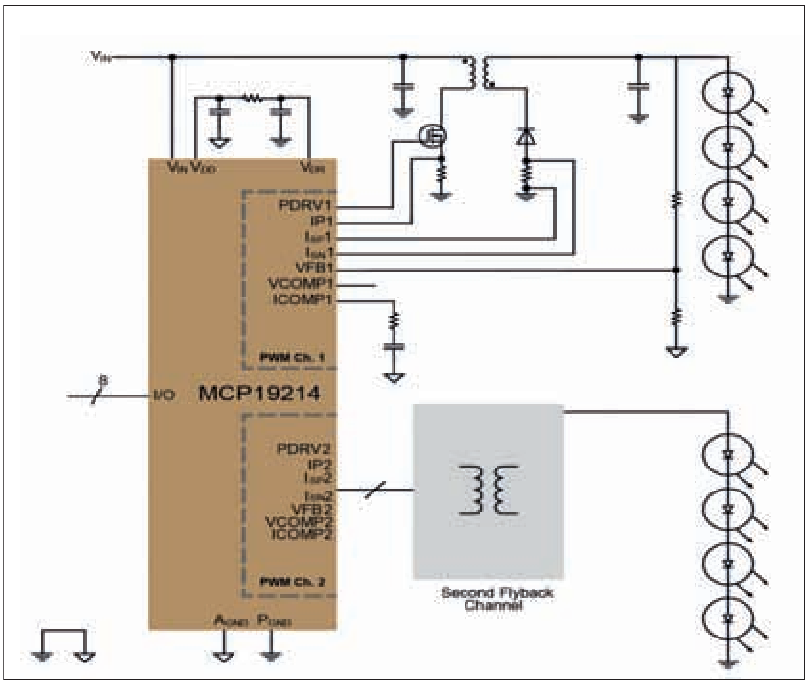
By utilizing a TC1240A voltage doubler supplied from V_{DD} to provide V_{DR}, a 10 V gate drive can be achieved. The 4 V LDO is used to power the internal analog circuitry. The two low-side drivers can be used to operate the power converter in bidirectional mode, enabling the 'shaping' of LED dimming current in LED applications or developing bidirectional power converters for battery-powered applications.

The ability to configure application-specific features allows users to save costly board real estate and additional component costs. The General Purpose Input/Output (GPIO) of the MCP19124/5 can be configured to offer a status output such as a device enable, to control an external switch; a switching frequency synchronization output or input and even a device status or "heartbeat" indicator.

Power trains supported by this architecture include but are not limited to boost, flyback, quasi-resonant flyback, SEPIC, Cuk, etc.

Two low-side gate drivers are capable of sinking and sourcing 1 A at 10 V V_{DR}. With a 5 V gate drive, the driver is capable of 0.5 A sink and source. The user has the option to allow the V_{IN} UVLO to shut down the drivers by setting the UVLOEN bit. When this bit is not set, the device drivers will ride through the UVLO condition and continue to operate until V_{DR} reaches the gate drive UVLO value. This value is selectable at 2.7 V or 5.4 V and is always enabled. An internal reset for the microcontroller core is set to 2.0 V. An internal comparator module is used to sense the desaturation of the flyback transformer to synchronize switching for quasi-resonant applications.

The operating input voltage for normal device operation ranges from 4.5 V to 42 V with an absolute maximum of 44 V. The maximum transient voltage is 48 V for 500 ms. An I²C serial bus is used for device communications from the PWM controller to the system.



Schematic of a dual LED driver

Start-up

To control the output current during start-up, the MCP19124/5 have the capability to monotonically increase system current, at the user's discretion. This is accomplished through the control of the reference voltage DAC (V_{REF}). Users also have firmware control over the switching frequency through Timer2 and the PR2 register. Maximum duty cycle control is established through the PWMRL register.

Fixed PWM frequency

The switching frequency of the MCP19124/5, while not controlled by the DESAT comparator output, is generated by using a single edge of the 8 MHz internal clock. The user sets the switching frequency by configuring the PR2 register. The maximum allowable PDRV duty cycle is adjustable and is controlled by the PWMRL register. The programmable range of the switching frequency will be 31.25 kHz to 2 MHz. The available switching frequency below 2 MHz is defined as F_{SW} = 8 MHz/N, where N is a whole number between 4 and 256.

Thermal shutdown

To protect the MCP19124/5 from over-temperature conditions, a 150ºC junction temperature thermal shutdown has been implemented. When the junction temperature reaches this limit, the device disables the output drivers. In Shutdown mode, both PDRV and SDRV outputs are disabled and the over-temperature flag (OTIF) is set in the PIR2 register. When the junction temperature is reduced by 20ºC to 130ºC, the MCP19124/5 can resume normal output drive switching.

The MCP19124 is packaged in a 24-lead 4 mm x 4 mm QFN and offers an alternate-bonded 28-lead 5 mm x 5 mm QFN. The MCP19125 is packaged in a 28-lead 5 mm x 5 mm QFN. Pricing starts at $3.17 in 10,000 unit quantities

www.microchip.com/mcp19215

More Power Supplied

APEC 2017 in Tampa/Florida from March 26 to 30 again marked a milestone in power electronics with record 5,000+ conference attendees. The focus were not so much on new power devices, but more on new circuit topologies and applications.

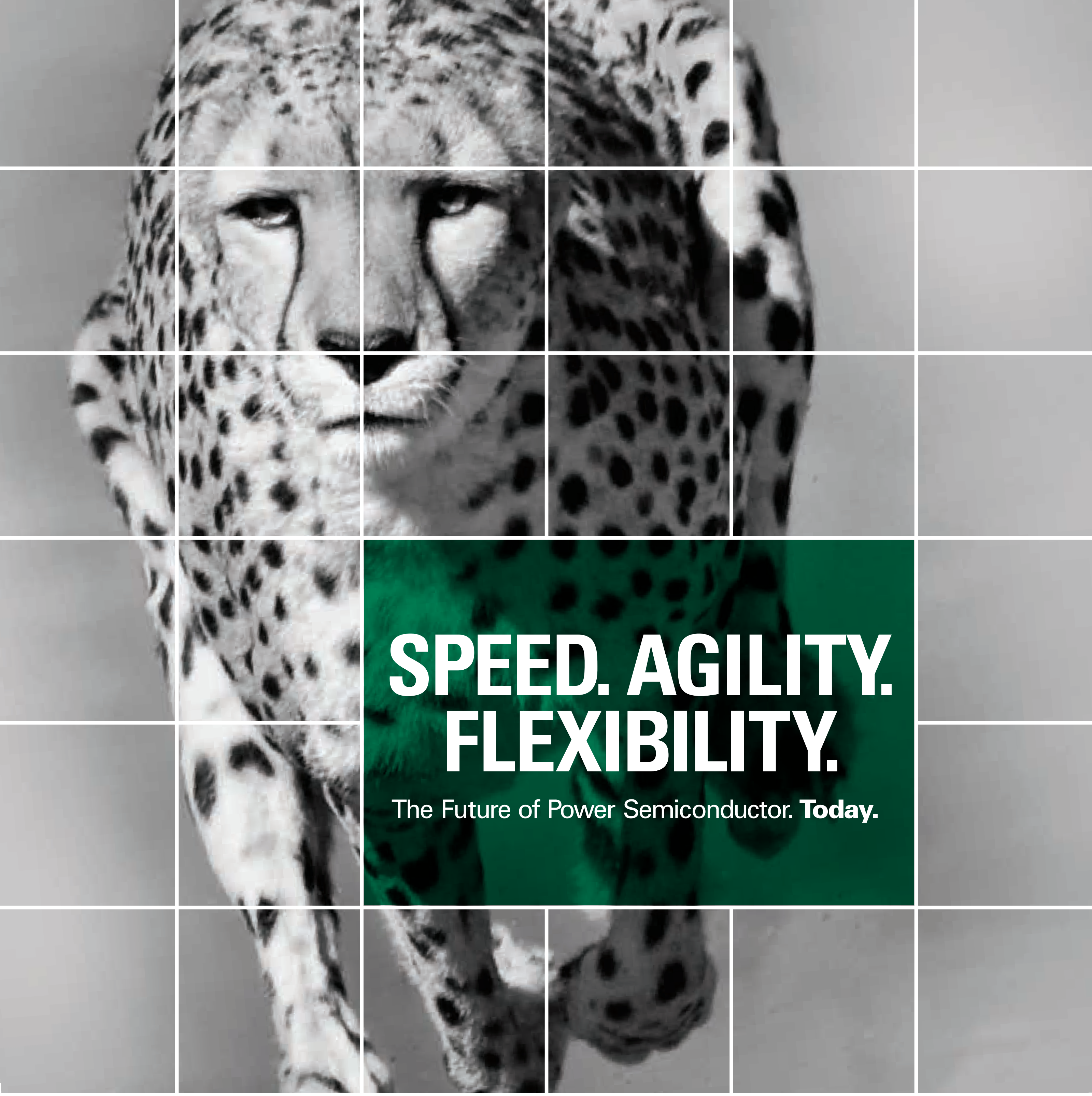
One of APEC's specialities are the keynotes within the plenary session on the first day, giving an overview of the latest developments and an outlook on future applications.

Ahmad Bahai, Chief Technologist at Texas Instruments, presented under the title 'USB Power Delivery – Opportunity for Today and Tomorrow' a more general outlook. According to Bahai in the year 2005 around 30 percent of electricity were flowing through power management systems, in 2030 it can be 80 percent. The multi-directional flow of data is now also flowing in power. But power scaling is much less than in microprocessors, it is 20 percent in low-power LDOs and less than 10 percent in high power applications. Silicon Carbide and Gallium Nitride will improve this situation, in particular GaN is coming to the point that is it affordable for most applications. Nevertheless, technology development is much slower than Moore's law, it takes more or less ten years to implement new materials. A leading European car manufacturer for instance is using GaN devices for on-board charger because of saving space and weight. At system level 5 percent price reduction and 50 percent performance increase can be gained. In data centers, GaN totem pole power factor correction and LLC can reduce volume by 30 percent, and direct conversion from 48 V to 1 V with GaN devices can improve efficiency by a factor 4. And GaN has the potential of using larger wafer sizes and thus cost reduction, what is not the case with SiC. Though his talk was focused on WBG, he mentioned USB 3.1 as the future power delivery solution capable of carrying 20 A or 100 W.

WBG applications

At the exhibition floor TI (**www.ti.com**) demonstrated how an end-to-end solution improves datacenter AC-to-processor power density by over 3x. GaN solutions are enabling a new generation of power-conversion designs not previously possible with Silicon MOSFETs. GaN-based solutions can be incorporated into power supplies throughout data centers, from the AC mains to the individual points of load (POLs). GaN also enables new architectures such as high-voltage DC distribution systems. Electric utilities require a power-

Tampa's Convention Center hosted APEC 2017


SPEED. AGILITY.
FLEXIBILITY.
The Future of Power Semiconductor. Today.

factor-correction (PFC) stage in order to optimize power-grid efficiency. PFC operates as a boost converter, and typically provides a DC output voltage of 380 V. This voltage needs to be further stepped down to provide a DC bus supply for the system. Various topologies are used for this stage, but inductor-inductor-capacitor (LLC) and phase-shifted full bridge are commonly used to generate a bus voltage of 12 V or 48 V. GaN-based solutions can change both the architecture and density of the entire power system, from the AC to the processors.

By a totem-pole PFC topology, GaN devices such as the integrated LMG3410 reduce the number of active power switches and filter inductors by 50 %, according to TI. A four- to tenfold increase in switching frequency (continuous conduction mode (CCM) or critical conduction mode (CRM) significantly reduces the size of magnetics while improving overall efficiency to over 99 %, versus 96% for today's titanium-grade power supplies. Interleaved solutions further scale the power stage to meet system demands. The DC/DC stage takes advantage of GaN's superior switching characteristics to push the LLC resonant converter to over 1 MHz, compared to some 300 kHz in previous solutions. The high frequency reduces the magnetics while improving power density and efficiency. The smaller form factor further enables the emerging high-voltage distribution systems in data centers for 380 V/48 V converters. GaN has a major impact on POL DC/DC converters. First, it enables a single step conversion from 48V in order to power processors, memories and other loads directly, reducing PCB real estate by as much as 50 % while reducing footprints by 75 %. Second, the half-bridge current double topologies using the LMG5200 enable to stack the power stages for different load demands. "The days of GaN being viewed as a future technology are over. GaN is here now and is enabling designers to do what was once unreachable - design new power systems that are substantially smaller, switch faster and are cooler than before", said TI's GaN expert Steve Tom.

Efficient Power Conversion Corporation (**www.EPC-Co.com**), demonstrated at the exhibition floor the scalability of their enhancement-mode gallium nitride on silicon (eGaN) power FETs and ICs with the introduction of the EPC2045 (7 mΩ, 100 V) and the EPC2047 (10 mΩ, 200 V) generation 5 devices. This fifth-generation technology cuts the die size in half for the same on-resistance and voltage rating. At 200 V the eGaN FET die size is more than 16 times smaller than an equivalently-rated silicon MOSFET. Applications for the EPC2045 include single stage 48 V to load Open Rack server architectures, point-of-load converters, USB-C, and LiDAR. Wireless charging, multi-level AC/DC power supplies, robotics, and solar micro inverters are example applications for the 200 V EPC2047. "These new products demonstrate how our gallium nitride transistor technology is increasing the performance and reducing the cost of eGaN devices for applications currently being served by MOSFETs. Further, advancements of our GaN technology will continue to enable new end-use applications that go beyond the capability of silicon devices. These products are evidence that the performance and cost gap with MOSFET technology continues to widen", said CEO Alex Lidow. EGaN devices have found already many applications, such as LiDAR, headlights or wireless charging in automotive, the latest interest comes from a German company for automotive laser headlights.

GaN Systems (**www.gansystems.com**) demonstrated commercial systems that use GaN transistors in wireless power transfer and power module applications. Showcased were also customer-built systems that use GaN transistors to power a diverse range of applications, including DC/DC converters, energy storage systems, or EV traction inverters. A 150 W transmitter wirelessly powering an airborne drone in real-time, operating at 13.56 MHz gained a lot of interest. The drone demonstrator designed at the Imperial College in London incorporated long range transfer (efficient operation up to around 1 to 2 coil diameters). It can cope, efficiently and robustly, with continuously variable air gap geometries as the drone moves around over the charging pad, without needing a dedicated tuning mechanism. Due to ultra-light weight systems that allows the small drone to fly with our system installed. Closed loop control between receiver to transmitter is not required – the system is globally open loop and the only closed loop control is on the receiver side. "High frequency operation is what allows us to achieve long range due to the high Q factors of the coils, and light weight due to the compact nature of the passive components. In this system we are using

a GS66504B and the inverter, whilst operating at only 35 W in this demo, can run to over 150 W", Paul Mitcheson, Imperial College, underlined. Another high-power example was a 5 to 10 kW half-bridge power block consisting of eight paralleled GaN transistors and a matching driver card.

Regarding SiC also the focus was on applications – and politics. Last year Infineon (**www.infineon.com**) announced plans to acquire Wolfspeed (**www.wolfspeed.com**) – the former power & RF division of Cree (**www.cree.com**), for around $850 million. Recently the Committee on Foreign Investment in the US (CFIUS) informed Infineon and Cree that the transaction poses a risk to the national security. Furthermore, CFIUS had not identified any mitigation measures that it believed would adequately mitigate the particular national security risks posed by the transaction. Against this background, Infineon is of the opinion, that there is that the transaction, as agreed, is not going to close. "We remain committed to work closely together with both CFIUS and Cree to find solutions that would mitigate the concerns, though we are very disappointed on this situation", said Peter Friedrichs, Senior Director SiC at Infineon Technologies. This transaction consists not only on Wolfspeed's device technology, but also the related substrate business from Cree, a major ingredient in the SiC value chain. Also Wolfspeed was not happy with this US decision – Wolfspeed's marketing director Paul Kierstedt was upset not to join Infineon's SiC activities. "We are disappointed that the Wolfspeed sale to Infineon could not be completed. In light of this development, we are going to shift our focus back to growing our business, perhaps with SiC MOSFETs in the voltage range below 900 V".

A new SiC player entered the APEC stage at Littelfuse's (**www.littelfuse.com**) booth. The company recenty announced it has made an incremental $15 million investment in Monolith Semiconductor Inc. (**www.monolithsemi.com**), a Texas-based SiC start-up company. "We are a fabless company designing planar 1200 V SiC MOSFETs with our partner X-Fab on 6-inch wafers. Planar technology does not have the problems of gate oxide degradation observed with trench technology", CEO sujit Banerjee stated. X-Fab, a high-volume 150 mm Silicon foundry develops all of the processes required to manufacture SiC wafers in a CMOS line. Specific challenges for SiC devices involve creating designs that are compatible with standard Si processing steps as much as possible, while optimizing the performance of the SiC power devices. An initial processing challenge was the optically transparent SiC wafers, which were difficult to handle on many of the existing Si fabrication processes and tools that rely on different methods for positioning and moving Si wafers. Monolith and X-Fab developed processing and tool updates to allow processing of transparent SiC wafers on the Si production line. Monolith Semiconductor is an active member of the DOE-supported National Network for Manufacturing Innovation PowerAmerica institute, which is led by NC State University, set up to advance the deployment of WBG semiconductor based power electronics particularly in the US. The company will also attend PCIM in May.

Silicon still in play

Besides the ongoing development of WBG technology Silicon improves even further. Infineon extended its portfolio of power MOSFETs with the 600 V CoolMOS™ P7 (**www.infineon.com/600v-p7**) and 600 V CoolMOS™ C7 Gold (G7) series. The P7 is targeting applications such as chargers, adapters, lighting, TV, PC power, solar, server, telecom and EV charging in power classes from 100 W to 15 kW. The wide on-resistance range from 37 mΩ to 600 mΩ for both surface mount (SMD) and through hole packages makes the 600 V CoolMOS P7 suitable for a broad variety of applications and power ranges. The G7 features a lower on-resistance, minimized gate charge, reduced energy stored in the output capacitance, and a 4 pin Kelvin source capability of the TO leadless package. This minimizes losses in PFC and LLC circuits and offers a performance gain of 0.6 percent as well as higher full load efficiency in PFC circuits. The low parasitic source inductance of 1 nH also contributes to the increased efficiency levels. The improved thermal properties in a TO leadless package enable the usage in higher current designs while SMD technology allows for a less costly mounting process. The C7 Gold features a very low on-resistance, ranging from 28 mΩ to 150 mΩ. Compared to traditional D2PAK, it offers 30 percent footprint, 50 percent height and 60 percent space reduction.

Obviously the power MOSFET market (see our Market News) is not saturated, thus a new start-up named D3 Semiconductor (**www.d3semi.com**) announced its entry into the power semiconductor market with the launch of 650 V+FET™ line (superjunction MOSFETs). The fabless Texas-based company claims to offer devices with lowest on-resistance and gate charge – a look in the preliminary datasheet for the D3S080N65 (650 V/38.3 A) gives a total gate charge of 77 nC and on-resistance of 80 mΩ. Reverse recovery charge is 9.5 µC. Packages include thru-hole (TO-220/TO-220FP), surface-mount (DPAK/D2PAK) and advanced surface-mount (5x6/8x8) devices. The initial product lineup of +FET devices offer socket-for-socket alternatives to competitive parts. "Our roadmap is changing the landscape of power devices by adding mixed-signal functions into high-voltage switching devices," said CTO Tom Harrington. Whether this means integrated digital functions for configuration or start-up has not been answered so far.

Power Integrations (**www.power.com**) launched the HiperPFSTM-4 family of PFC ICs incorporating a 600 V MOSFET suitable for 305 VAC input in a electrically isolated, heatsinkable eeSIP package. The new ICs suit enclosed designs up to 300 W, open frame power supplies of up to 400 W and highline applications up to 550 W. Protection features include UVLO, UV, OV, OTP, brown-in/out, cycle-by-cycle current limit and power limit. HiperPFS-4 ICs consume less than 60 mW at 230 VAC while regulating output at no-load and less than 20 mW in sleep mode (see more details in our Industry News).

Peregrine Semiconductor, a Murata company, announced Arctic Sand's (**www.arcticsand.com**) acquisition and its ARC3C family of LED driver ICs, targeting the fast growing, ultra-high-definition (UHD) LCD backlight applications. The ARC3C LED drivers, manufactured at TSMC, has up to eight integrated programmable current sinks, integrates all MOSFETs, control and driver circuitry, and features dimming options within a 4 mm x 4 mm QFN package. The drivers are designed specifically for 2-cell or 3-cell input voltages, with product variants suited up to 8-string LED arrays sinking current up to more than 40 mA per string. The ICs feature fault protection including over-current, output over-voltage and under-voltage protection, LED open and uniquely short circuit protection. An I^2C 6.0-compatible serial interface operating at up to 1 MHz allows programming, with settings stored in non-volatile memory. "Rated at up to 10 W output power, the ARC3C can save up to 1 W of power in the LED boost switched capacitor circuit, improving battery runtime for a notebook computer by typically one hour by delivering LED efficiency levels of greater than 94 percent peak at up to 45 V output and with an input voltage range up to 15 V", Peregrine's marketing director Stephen Allen commented. His goal is to integrate all boost circuity including Silicon capacitors into the IC. **AS**

pcim
EUROPE

International Exhibition and Conference
for Power Electronics, Intelligent Motion,
Renewable Energy and Energy Management
Nuremberg, 16 – 18 May 2017

Ever Increasing Interest in Power Electronics

The increase of around five percent of exhibitors particularly in passive components is a tribute to the positive development of PCIM Europe. Overall, more than 450 exhibitors from 28 nations will be present in Nuremberg from 16 – 18 May 2017. Seminars and Tutorials will be held on May 14 and 15.

The exhibition offers a varied program in two different forums. At the industry forum, associations, experts from specialized media as well as from renowned companies discuss issues which are moving the sector at present. For instance, Pierric Gueguen, Business Unit Manager Power Electronics and Compound Semiconductors at Yole Développement in Lyon, talks about "Status and Perspectives in Power Semiconductor Business" and Richard Reiner, scientist from the Fraunhofer Institute for Applied Solid State Physics IAF in Freiburg, will address the subject "Monolithically-Integrated GaN Circuits". During all three exhibition days, the exhibitor forum informs visitors about product highlights in the power electronics sector in twenty-minute presentations.

E-mobility is increasingly emerging as a new business segment with immense growth potential. Thus the new E-Mobility Area in hall 6, a central platform for products and solutions on the topic of automotive, has been established. On the first and second exhibition day, presentations on current industry trends will be offered. The distinctive focus is set on new developments and challenges in power electronics with regard to diverse applications such as electrical, hybrid and fuel cell vehicles as well as charging

Again it's time to visit PCIM Europe from May 16 – 18 in Nuremberg infrastructure. To name only a few examples, Dr. Bernd Eckardt, Fraunhofer Institute for Integrated Systems and Device Technology IISB focuses on "Power Electronics for next Generation Electric Vehicles". Laurent Beaurenaut, Infineon Technologies AG, on the other hand, poses the question "Silicon Carbide Inverters: The Future of Electromobility?". On the third and final day of the event, exhibiting companies introduce product innovations specifically for the automotive sector in 20-minute presentations.

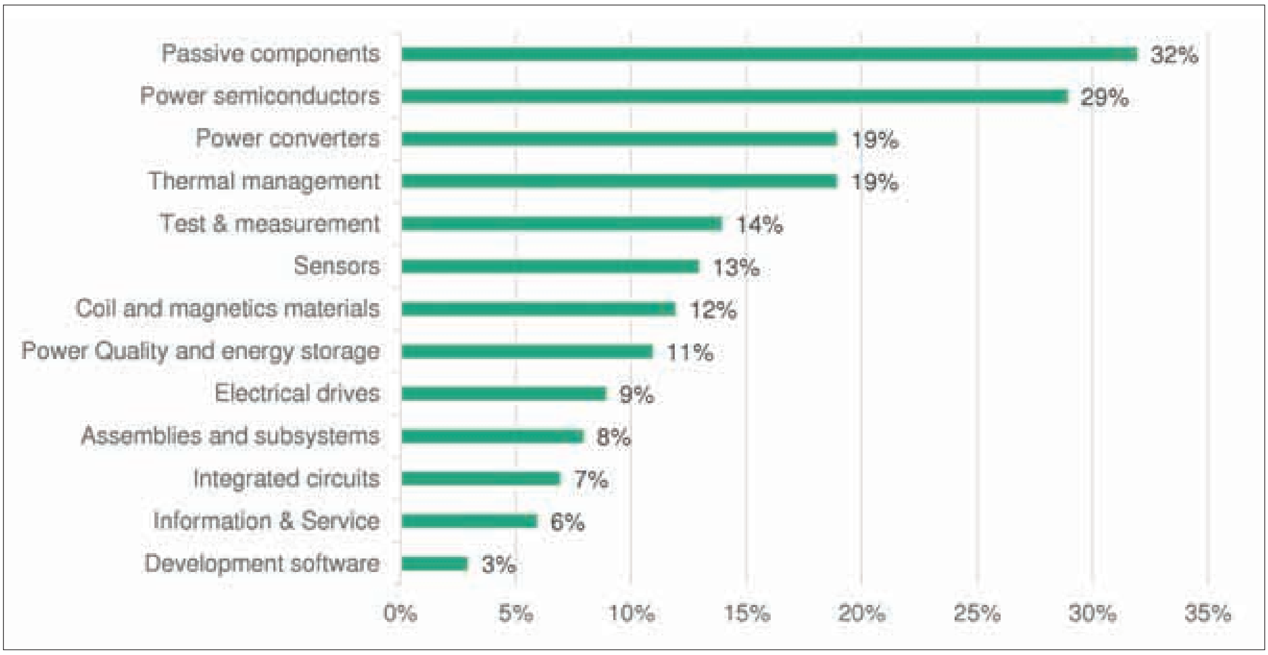
The exhibition is one highlight of PCIM Europe, the other is the conference. Experts from industry and science report on new developments and future-oriented topics in more than 100 presentations and more than 200 poster sessions, each one an initial publication. On each day keynotes in the morning present insights into the future of power electronics. Other conference highlights are three special sessions on "Passive Components", "Capacitors" and "Measurement Technologies with Focus on High/Low Power".

Keynotes on current topics

Long Distance Charging Solutions for BEVs: from now to 2030, that is the title of the first keynote after the opening and award ceremony, given by Robert Lassartesses from Renault SAS in France. The today trend is to increase the battery and the fix charger power. However, this trend limits the mass market for BEVs (battery electrical vehicle). The keynote will show some of these limits on the car point of view (battery cost/packaging/weight, uncertainty on specific material availability and environmental consideration). Game changer as charging during driving could solve these mass market car roadblocks. Charging during driving transfers an important investment part from BEV to infrastructure by reducing battery size or in other words transfers investment from the BEVs owners to the public. If we consider that 5000 euros could be saved by reducing the needed battery size and if we consider 30 % EVs to be sold each year, it would represent 3 billion euros investment each year for road infrastructure only for a country like France. In any case, hundreds of billions will be needed though the world to equip the road in coherence with the high number of BEV expected from now to 2030.

The Smart Future of Power Electronics and its Applications will be discussed by Hans Krattenmacher from SEW-Eurodrive in Germany. Power electronic components have been used for decades in devices in the field of electric drives. One of the most important devices is the conventional frequency inverter which is employed in countless applications of the conveyor technology, materials handling technology as well as the field of machine automation. The technology and therefore the power electronics have been adjusted, improved, optimized and perfected to fit the applications throughout the years. However the application itself hardly changed as the main focus lied on making it faster, more efficient and more robust. The traditional stationary materials handling technology, in which many gearmotors and electronic components are built into, will be replaced by mobile materials handling systems. Based on this knowledge it can be concluded that the product in its current form will no longer be needed in the solutions of tomorrow. The production philosophy for the future SMART Factory will be organized and operated in a completely new way. Power Electronics will remain an enabling technology however the converter technology will become "SMART".

The third keynote on the Thursday is entitled Evolution in Topologies as a Result of New Devices and Enabling Technologies and will be presented by Ionel Dan Jitaru, Rompower USA. The topic that new topologies may be needed as the progress in semiconductor industry and other enabling technologies are emerging, has been raised with different occasions. Though in the last thirty years no more topologies were introduced, we noticed a clear shift in the preferred topologies used by engineers in power conversion. That shift did occur mostly due to the progress in semiconductor devices. Another key role was played by the type of applications in power electronics which changed some of the specifications and favored some topologies over others. Recently the availability of digital control has opened the door to intelligent power processing, and allowed us to take a conventional topology and convert it in soft switching topology without any changes in the hardware. his presentation will look at the progress of some topologies over the years such as flyback topology, forward derived topologies including the two transistors forward, half and full bridge topologies and the changes made in order to further improve the performances. The latest two transistor forward topology



Featured product groups at PCIM Europe exhibition

achieves soft switching both in primary and secondary, with minor hardware changes and through intelligent control. The same evolution is achieved also in the traditional boost converter, which evolved in the latest applications in PFC wherein the efficiency went above 99 percent mostly due to the GaNs and intelligent control.

High-voltage SiC

On the first day the morning session HV SiC MOSFETs will highlight the latest advances in semiconductor and module technology.

A 3.3 kV/450 A Full-SiC nHPD2 (next High Power Density Dual) module will be introduced by Dr. Takashi Ishigaki, Hitachi Power Semiconductor Device,Ltd., Japan. The extremely low internal inductance of the package can make the best use of full-SiC. Fast and smooth switching of the module will be explained, as well as the output characteristics of the full-SiC module in traction inverter simulation with considering the reverse conduction of the module accurately.

Characterization of 3.3 kV and 6.5 kV SiC MOSFETs is the subject of the paper presented by M. Eng. Takui Sakaguchi, ROHM, Kyoto, Japan. Over 3.3kV SiC MOSFET is the promising technology for further contribution to the low energy consumption society. ROHM fabricated 3.3 kV and 6.5 kV SiC MOSFET and demonstrated static and dynamic characteristics and avalanche capability.

Dynamic Characterization of Next Generation Medium Voltage (3.3 kV, 10 kV) SiC Power Modules is the name of the paper by Ty McNutt, Wolfspeed, USA. It paper focuses on dynamic analysis of the new 3.3 kV & 10 kV all-SiC power modules, based on the third generation SiC MOSFET technology. A clamped inductive load test is utilized to analyze switching events across multiple system variables including: bus voltage, switched current, and gate resistance.

A 3.3kV All-SiC Power Module for Traction System Use will be introduced by M. Eng. Tetsu Negishi, Mitsubishi Electric Corporation, Japan. Mitsubishi developed 3.3kV all-SiC power module composed of SiC-MOSFET and SiC-SBD. The total power loss is significantly reduced by 59 % compared to conventional Si power module. In addition, the inverter operation reliability is confirmed by durability performance test with H-bridge circuit as actual railcar traction system.

SiC MOSFETs

In the afternoon the session SiC MOSFET will dive more in the device technology.

Infineon's CoolSiC Trench MOSFET Technology for Low Gate Oxide Stress and High Performance will be examined by Dr. Dethard Peters, Infineon Technologies, Germany. A novel SiC trench MOSFET concept is described which balances low conduction losses with IGBT like reliability by designing the gate oxide stress low enough to fulfill requirements of industrial applications. Long term gate oxide tests reveal that the extrinsic failure rate can be confidently predicted to <1 ppm. Basic features of the performance of the 45 m Ω/1200V CoolSiC MOSFET are presented. The favorable temperature behavior of the on-state makes the device easy to operate in parallel.

The paper Short-Circuit Robustness of Discrete SiC MOSFETs in Half-Bridge Configuration by Nicolas Degrenne, Mitsubishi Electric, France, studies the short-circuit robustness of SiC power MOSFETs in half-bridge configuration. The energy repartition during short-circuit is inherently unstable and unequal, leading to the failure of one device before the other. The short circuit event before destruction typically lasts 50 % longer in half-bridge configuration, compared to single-device short circuits. Different series of tests are realized to identify failure scenarios and mechanisms.

The paper Design Rules To Adapt The Desaturation Detection For SiC MOSFET Modules by Teresa Bertelshofer, University of Bayreuth, Germany, presents an over-current and short-circuit detection method for high current SiC MOSFET-modules adapting the existing desaturation detection, which is state-of-the-art for IGBTs. These adjustments include separate detection paths for hard switching faults and fault under load as well as preventive gate clamping and soft shut down. Test results show reliable detection and shut down of over-current, HSF and FUL while not influencing normal switching behavior.

Device Simulation Modeling of 1200 V SiC MOSFETs will be examined by Dr. Benedetto Buono, ON Semiconductor/Fairchild, Sweden. SiC MOSFETs for 1200 V rating were fabricated and used for comparing electrical measurements with device simulations. The MOSFET subthreshold characteristics were used for tuning the simulation model parameters for acceptor interface traps at the SiC/SiO2 interface. Good agreement between measurements and simulations was obtained for ID-VGS, ID-VDS, breakdown voltage and qualitative agreement was obtained for the reverse transfer capacitance.

GaN and SiC

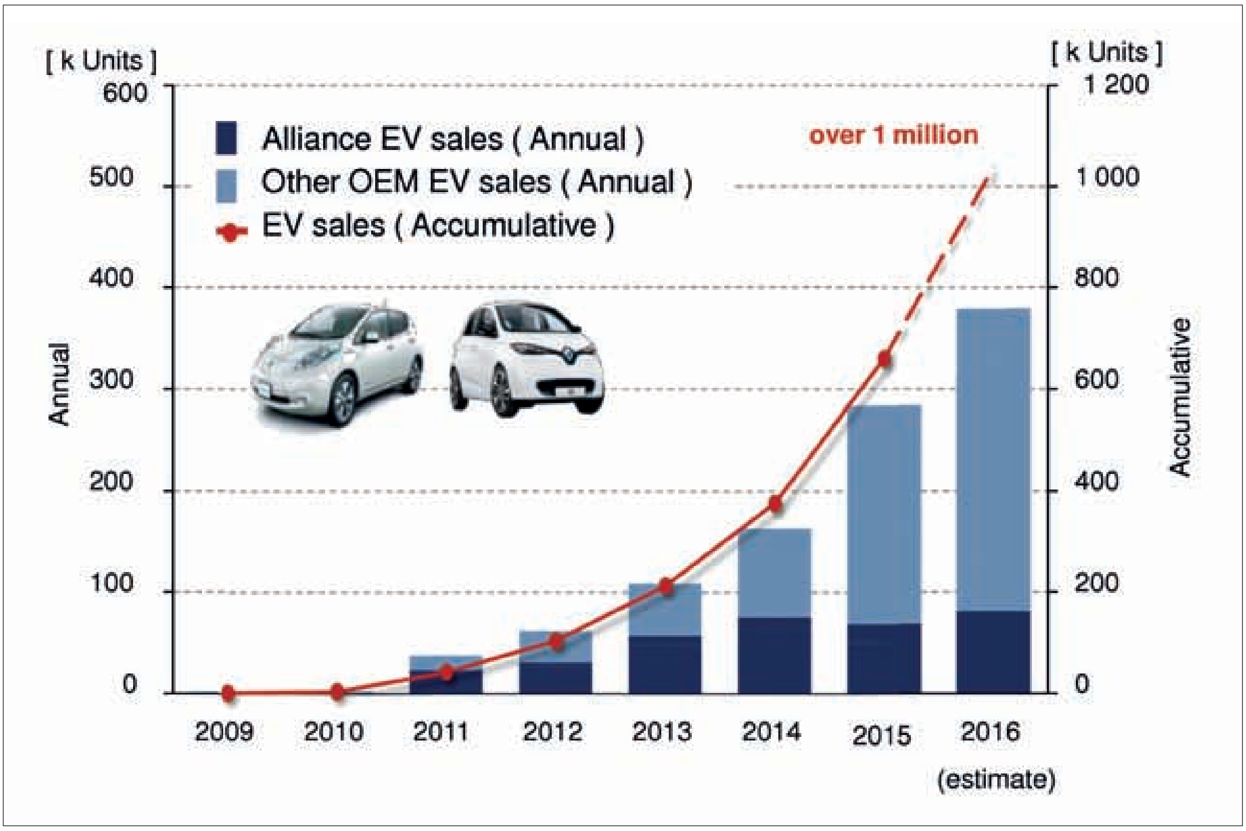
On the Thursday (May 18) morning the session Advanced Wide Bandgap will cover GaN and SiC.

The work Investigation of GaN-HEMTs in Reverse Conduction by Richard Reiner, Fraunhofer Institute for Applied Solid State Physics (IAF), Germany, investigates the reverse conduction characteristic of 600 V-class GaN-HEMTs. The behavior of a conventional HEMT is analyzed and compared to the reverse conduction of an improved HEMT structure with integrated free-wheeling diodes. The characteristics of both structures are measured on exemplarily fabricated devices. Furthermore, the behaviors are explained with regards to the intrinsic layouts.

The paper Dispersion of Electrical Characteristics and Short-Circuit Robustness of 600V E-mode GaN Transistors by Matthieu Landel, ENS/SATIE, France, presents experimental work on the short-circuit capability of 650 V GaN transitors.

A Mechatronic Design of 2 kW SiC DC/AC Converter will be introduced by Dipl.-Ing. Thomas Menrath, Fraunhofer Institut für Integrierte Systeme und Bauelementetechnologie IISB, Germany. Goggle's Little Box Challenge has shown that with a SiC based solution highest power densities can be reached in the 400 V voltage range. The Fraunhofer IISB approach has a power density of 201 W/inch (86.5 mm x 75.5 mm x 25 mm = 0.163 dm^3 @ 2kW) and is based on a 6-switch power topology with latest 900 V SiC MOSFETs. The key to high power densities is a well-designed mechatronic assembly.

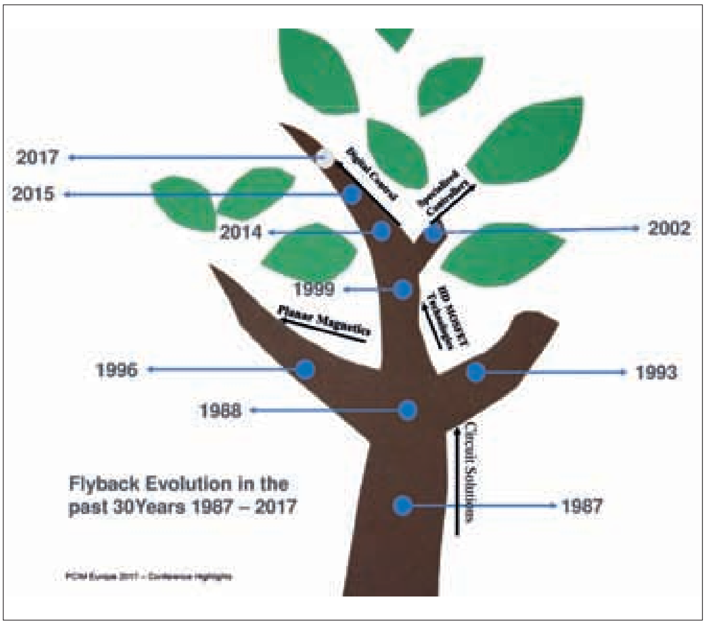
A Full SiC Module Operational at 200°C Junction Realized by a New Fatigue-Free Structure will be introduced by Hiroshi Notsu, National Institute of Advanced Industrial Science and Technology (AIST), Japan. A full-SiC module for 200°C operation was developed. To get a highly reliable attachment structure, the designers focused on keeping the sintered copper joint layer in the elastic region. There are two essential factors. One is a thin copper layer



Subject of the first keynote is charging of BEVs (battery electrical vehicles) by Renault/Nissan France

sandwiched by a roughly one order thicker SiC and substrate. The other is to get an active metal brazed substrate's coefficient of thermal expansion close to SiC. The module was operated over 35,000 power cycles at 200°C junction temperature.

A Novel SiC Power Module with 3D Integration will be examined by Dr. Jinchang Zhou, ON Semiconductor, USA. A 3D stacked power module with interposer is introduced. Unlike conventional structural or other double-sided cooling modules, the power devices are stacked over and connected with interposer with via. In this way, power density is greatly increased with smaller module size. The module featured with ultra-low parasitic, high operation temperature (> 200°C), and low thermal resistance with double sided cooling, is a great fit for SiC power module requirement. The process to manufacture



The third keynote deals with the Evolution in Topologies as a Result of New Devices and Enabling Technologies by Rompower USA

such a module with high robustness, reliability as well as of process simplicity is also addressed.

Passive components and new materials

This session on the Wednesday afternoon deals with the trend towards higher switching frequencies and working temperatures of upcoming power electronic systems.

The Evolution of Magnetics in Power Electronics Applications and Facing the Challenges of Future Electronics Industry will be covered by B. Eng. Kapila Warnakulasuriya, Murata Power Solutitons, UK. It is a widely accepted fact that magnetic components have not gone through its evolution at a competitive or even at a sufficient speed compared to the evolution of electronics. In this paper a compressive coverage is given on the evolution of magnetics from conventional wire wound components to planar magnetics to PCB integrated and on chip magnetics. The suitability of each generation of magnetics for different areas of applications is discussed with practical examples. The development of ultra-high power high frequency magnetics also discussed based on developments done by the author.

High Performance Common-Differential Mode Chokes for High Efficient EMI Filters will be examined by Dr.-Ing. Thiemo Kleeb, University of Kassel, Germany. Converter operation of several 100 kHz in the lower kW power range requires very high filter attenuation, because of EMI standard limitations. Combined common-differential mode chokes can take advantage of attenuating both common and differential mode noise effectively. Therefore, these components can reduce the effort and the power loss of EMI filters significantly.

The paper Dimensioning and Testing Planar Inductors for High Frequency Operation by Dipl.-Ing. Gérard Delette, CEA-Léti, France, deals with the the operation of passive components (inductors) in high frequency power converters. A prototype of planar inductor made of NiZn spinel ferrite has been designed in order to minimize the thermal heating due to power losses. Experimental results obtained after implementation in a boost converter are discussed.

This is a selection only based on the released program. More details on the numerous oral and poster sessions are available on PCIM's wewbsite. AS

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Low Temperature Silver Sintering Improves Reliability of Power Semiconductors

Reliability and lifetime of power semiconductors can be improved by using low temperature sintering on silver-containing layers. It is worth mentioning this technology has many applications - from IGBTs, where this technology allows to ensure a reliable connection chip-DBC, DBC-substrate, DBC–power terminals, to SCR thyristors and their subtypes (PCT, BCT, GTO, etc) where it is required to ensure a reliable connection between the power chip and molybdenum thermal compensator. **Dmitry Titushkin, Alexey Surma, Alexander Stavtsev, and Konstantin Stavtsev, Proton-Electrotex, Orel, Russia**

Sintering of high-powered single-chip thyristors and diodes experience is representing such advantages as improved cycling capacity (3, 4), reduced thermal resistance [2, 3, 4] as well as increased surge current values (1). Moreover, the technology possesses significant benefit of the emitted layer surface injection index values (6). However, to achieve all the above listed advantages one must pay attention to several specific aspects. The sintering technology is based on principles of diffusion welding and plastic deformation of silver particles. The driving force of sintering is to store energy on the surface of silver particles.

Specifically, reduction of silver particles size leads to an increase of free energy of silver particles in not sintered material. Thus an increase of free energy allows to reduce temperature during sintering. The temperature reduction in turn has a positive impact on the degree of residual deformations in silicon structure. However excessive free energy may lead to a very intensive sintering, resulting in internal mechanical stresses and joint cracking. One may eliminate this unfavorable effect with increased connection porosity, as higher porosity means higher elasticity (reduced Young's modulus). However increased connection porosity results in worse joint thermal conductivity having a negative impact on the device's thermal resistance.

Besides that, there is another negative effect of excessive porosity in joint weld porosity relevant only for thyristors and diodes with large area crystals installed in disc cases. When such devices undergo thermal cycling tangential mechanical stresses are transferred from lower and upper copper basements to semiconductor element by forces of friction. In such cases molybdenum thermal compensator as a part of the semiconductor element compensates such influence. However, reduced Young's modulus of the connection results in inability of the molybdenum thermal compensator to fulfill its task and the silicon plate gets damaged. For this reason, semiconductors with large diameter silicon crystals require to ensure such a connection porosity value that would eliminate the possibility of internal stresses during sintering but at the same time would not critically impair thermal resistance and mechanical strength of the connection.

Relation between cycling capacity and joint porosity

For research of the relation between thermocycling capacity and porosity of the joint and determination of the optimal temperature and pressure range during the sintering process experimental samples of 100 mm thyristor dies for repetitive reverse voltage of 2800 V and mean current of 2500 A were produced. Silver films based on silver nanoparticles were used as sintering material. The samples were produced in a temperature range of 195 to 235°C and pressure range 5 to 20 Mpa.

Using the experimental samples thermocycling capacity tests were carried out using thermal gradient from 25 to 150°C (value = 125°C) within a quantity of 100 cycles. The following results were obtained:

- Thermocycling capacity of the samples produced under the temperature less than 220°C did not exceed 10-15 cycles, i.e. the porosity of the result joint was obviously surplus.

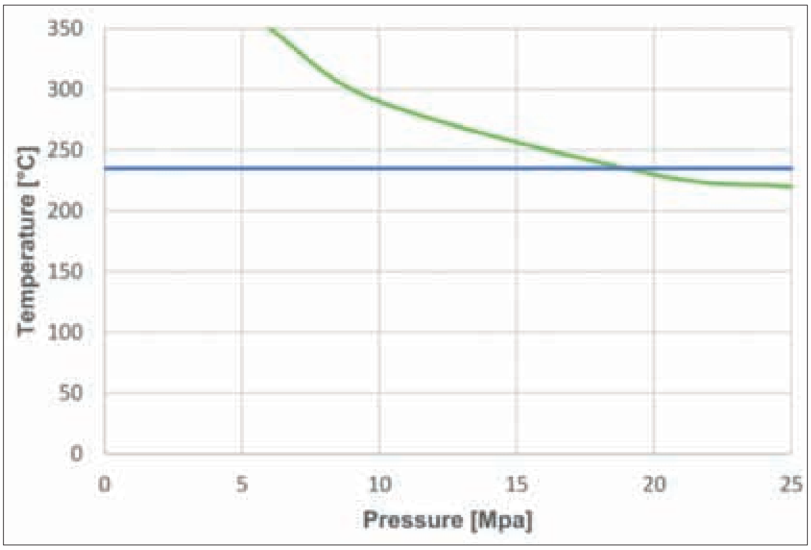
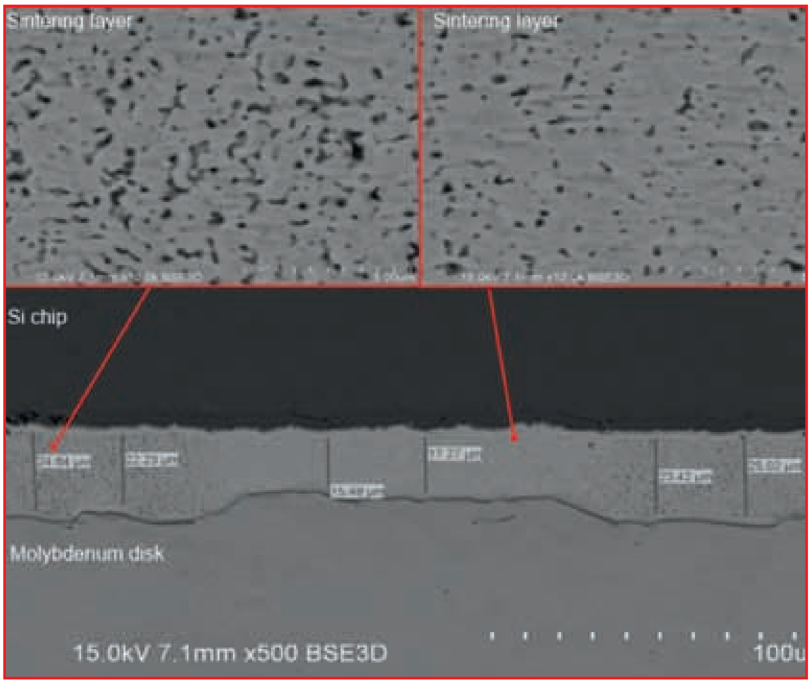
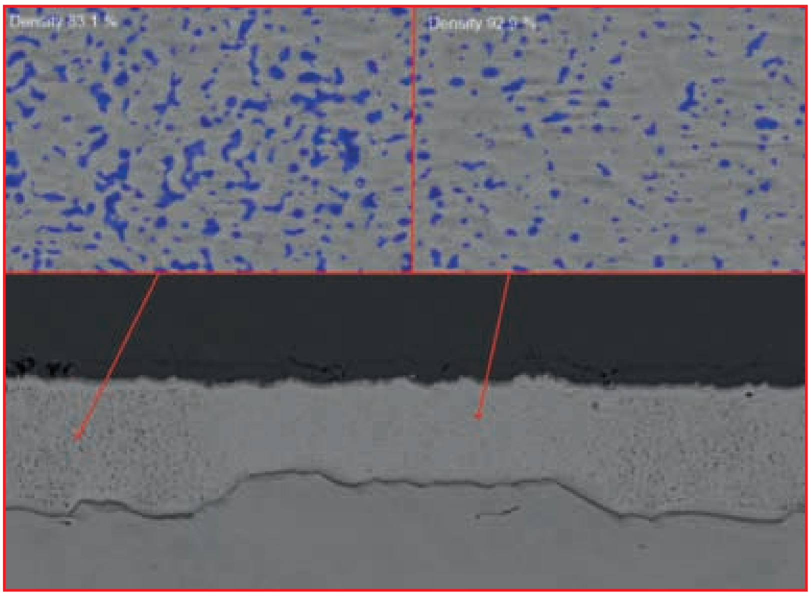


Figure 1: **The area of thermocycling capacity of samples (between the lines)**



RIGHT Figure 2: SEM-analysis of the sample sintered structure



BELOW Figure 3: Sinter beam density evaluation

- Thermocycling capacity of the samples produced under the temperature of 220-235°C and pressure not more than 10 MPa did not exceed 10-15 cycles as well.
- The increase of pressure up to more than 12 MPa leads to the thermocycling capacity boost.
- For the samples produced under the conditions of 20 MPa pressure and 235°C temperature the destruction and characteristics degradation was not determined.

The test results should be combined with the porosity alterations of the weld produced under various sintering process conditions (Figure 3). It could be derived from the picture that acceptable thermocycling capacity would be achieved providing the condition of weld porosity not more than 7 percent.

Then the samples produced under 20 MPa/235°C were subjected to electric thermal cycling testing using direct current 2500A with temperature gradient between cycles from 55 to 125°C (70°C), 30,000 cycles. There was no damage or properties reduction detected.

The results of the research allow to calculate and forecast the pressure and temperature value range, with which nano material sintering gives an opportunity to achieve a high thermocycling capacity silicon-molibdenum joint for thyristors and diodes with large area crystals, (Figure 1).

Porosity variation related to sintering technology

Usage of silver containing film requires attention to quality of the sintered surfaces. High values of surface roughness make it harder to ensure even distribution of the force during sintering. It is especially important if the sintering technology is used for crystals and molybdenum discs with area of 50 cm^2 or more. Mismatching roughness of the molybdenum disc to that of the silicon plate may cause uneven porosity of the joint weld across the connection area formed during sintering because of uneven pressure distribution. For this reason, usage of sintering for crystals with large area requires special attention to preparation of the molybdenum disc and plate surfaces.

For example, listed below are results of testing of a connection between semiconductor thyristor element with diameter of 100 mm and molybdenum discs with the following roughness values: Ra = 0,9 µm, Rz = 4,6 µm, R_{max} = 9,54 µm. Sintering took place on silver containing films Argomax 8010 with thickness 65 µm at 20 MPa and 235°C (thickness of silver containing joint after sintering within 20 µm). SEM-analysis of the sample was carried out after the sintering (Figure 2).

The image demonstrates that high roughness of the molybdenum disc causes unstable thickness of the joint (from 25 to 15 µm) affecting beam density. Evaluation of the sinter beam density has shown (Figure 3) that one and the same semiconductor has significant fluctuations of the beam density (from 83.1 to 92.9 %) and resulting high variety of porosity (from 16,9 to 7,1%).

Mechanical shear stresses arising during thermal cycles are localized in "harder" areas of the connection with lower porosity, and their amount respectively becomes higher. Thus various thickness of the beam results in significant drop of cycling capacity of the joint.

Conclusions

This article shows the influence of sintering process conditions using silver nanoparticles on the weld porosity and thermocycling capacity, obtained by joining silicon crystals of large area with molybdenum wafers. The relation between the thermocycling capacity of the experimental samples and weld porosity is demonstrated. Moreover, it is proved that a prerequisite requirement for maintaining the thermocycling capacity of thyristors and diodes with silicon crystals of large area in tablet housings is a value of weld porosity not more than 7 percent. Temperature and pressure value range for sintering process of silver-bearing materials based on nanoparticles is defined. This value range allows to calculate and forecast high level of thermocycling capacity of the weld referring to the components mentioned above. Also shown is that surface roughness of connected elements may lead to significant variations of porosity distribution across the area of the sinter beam, what may affect cycling capacity of the connection.

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Tailoring Circuit Materials for Power Electronic Applications

As electronic devices continue to shrink in size as they grow in power, demand grows for power electronic circuits with increased power density. Increased operating temperatures are one of the trade-offs of increased circuit power density, with an increase in thermal stress for the circuit materials that serve as substrates for modern power electronic circuits. This article provides an overview of a family of processes that can help take advantage of the many benefit available from ceramic circuit materials.

Manfred Goetz, Rogers Corporation Power Electronics Solutions, Eschenbach, Germany

The requirements for PCB materials capable of supporting high-density power electronics circuits are quite challenging, since they include both mechanical and electrical stability at high temperatures. To meet these demands, curamik® ADVANTAGE provides a ceramic-materials-based solution for the smaller, higher-power-density circuits of PCBs for modern power electronic applications. These materials feature ceramic substrates with low dielectric loss and low-loss copper conductors that support high voltages and currents in power-grid, energy, and industrial power applications. By design, ADVANTAGE is a family of features to optimize the performance of those materials.

A substrates family

The high-temperature, high-voltage circuit materials include four different ceramic-based substrates, each formulated to provide strengths and benefits in different applications. The materials are available with thick copper cladding for high-power circuits, with a direct-bonded copper (DBC) or active metal brazing (AMB) attachment of copper to substrate depending upon the substrate material. DBC materials employ a high-temperature melting and diffusion process in which pure copper is bonded to the ceramic substrate. AMB materials use high-temperature brazing to create a strong bond between the copper and the ceramic substrate material.

The four ceramic substrate materials provide different levels of power-handling and thermal-management capabilities (Figure 1). For example, curamik Power is based on Al_2O_3 ceramic substrates and is a good fit for cost-effective power electronic circuits. It has thermal conductivity of 24 W/m-K at 20°C. For slightly higher-power circuits, curamik Power Plus adds zirconium (ZrO_2) doping to the Al_2O_3 substrates to achieve thermal conductivity of 26 W/m-K and higher robustness. For a significant jump in operational lifetime and and thermal capabilities, curamik Performance uses silicon nitride (Si_3N_4) ceramic material to provide thermal conductivity of 90 W/m-K. Finally, for truly high-density power electronic circuits, curamik Thermal features aluminum nitride (AlN) substrates with outstanding thermal conductivity of 170 W/m-K. The materials can be supplied as master cards or formed into single parts as small as 15 mm × 15 mm.

Gaining an ADVANTAGE

These materials provide low loss with thermal properties well suited to a wide range of power electronic applications. For optimum performance, however, ADVANTAGE is a series of features meant to improve the performance and usability of these materials. This includes a choice of plating materials, addition of solder stop to control solder coverage, treatments for surface roughness, and a state-of-the-art silver sintering process that provides an attachment option to solder for critical high-temperature applications.

ADVANTAGE includes a wide selection of plating options for surface finishing of the copper patterns of the four mentioned above circuit materials, including nickel (Ni), nickel-gold (NiAu), and silver (Ag) plating. These different plating processes help to enhance solder wettability and improve the efficiency and effectiveness of a solder process used with the ceramic materials and improve wire bonding and ultrasonic welding. The in-house processes are performed by wet-chemical deposition and include a selective silver-plating capability so that sections of copper can remain bare as needed.

These ceramic circuit materials are manufactured by means of tightly controlled processes, resulting in consistent electrical and mechanical behavior from lot to lot and across the

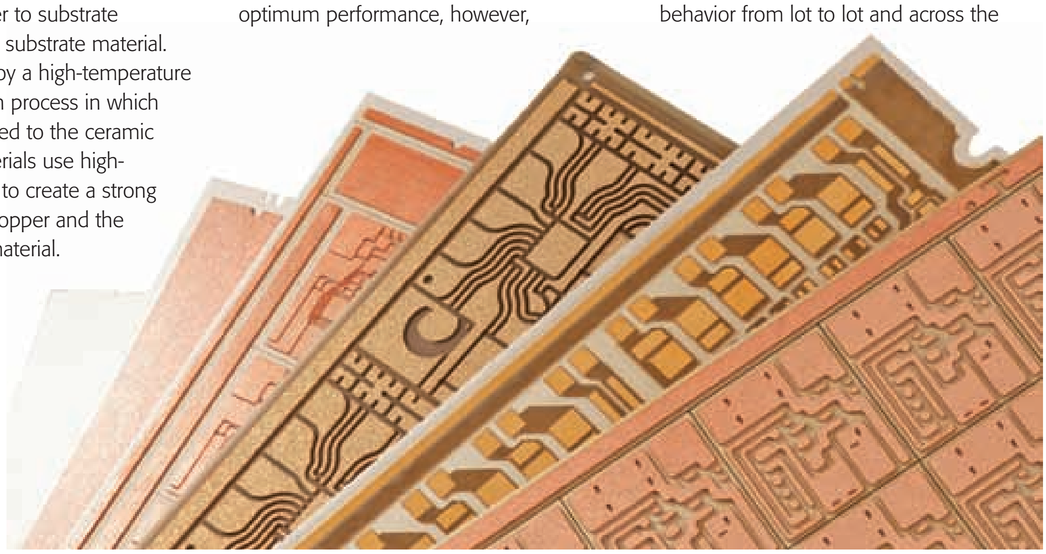


Figure 1: The four curamik ceramic circuit materials provide different levels of thermal dissipation

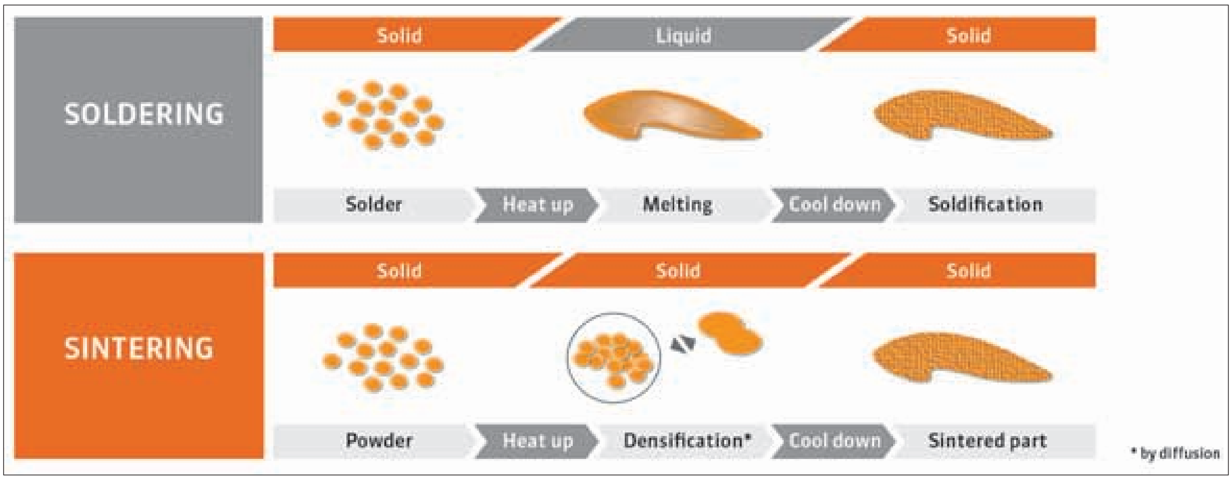


Figure 2: Silver sintering is a process in which heat is applied to a silver paste, resulting in densification (Soldering-Sintering graphic from curamik Substrates for Silver Sintering tech note)

surface of each master card. For most circuit wire-bonding and soldering processes, the normal surface roughness of curamik materials (with $R_{max} = 50$ µm and $R_z = 16$ µm) suitable for thick wire bonding and standard soldering process. But when thin wire bonds are required, the surface roughness should be minimized as much as possible. As part of the ADVANTAGE process, chemical or mechanical treatments are available to reduce the surface roughness of the materials to less than 50 % of the standard z-axis surface roughness: R_z less than 6 µm for mechanical treatment and R_z less than 7 µm for chemical treatment.

Formation of solder bridges during circuit fabrication is often difficult to avoid. The "overflow" of solder can not only jeopardize performance and reliability, but can decrease production yields. Fortunately, curamik circuit materials can be treated with solder stop to help streamline and stabilize the soldering process. The solder stop materials, which can be precisely positioned on a PCB, separate areas requiring solder from those that do not, such as wire-bonded connections. Solder stop for these circuit materials is available in standard and high-temperature versions, both in minimum width of 0.4 mm that can be positioned with a tolerance of ±0.2 mm. Standard solder stop is designed to withstand temperatures as high as 288°C for 10 s while high-temperature solder stop can handle temperatures as high as 400°C for as long as 5 min.

Handling the heat

As an alternative to soldering in high-power/high-temperature applications, silver sintering is available for all of the curamik ceramic materials as part of the ADVANTAGE family. Compared to a soldering process in which heat is applied until a solid reaches its melting point and is then allowed to cool down and solidify to form a bond, silver sintering is a process in which heat is applied to a silver paste, resulting in densification (Figure 2). During silver sintering, several actions occur simultaneously, including grain growth, pore growth, and densification.

Silver has a melting point of 961°C and excellent thermal conductivity of 240 W/m-K. The size of the silver particles in the sintering paste can be controlled for different degrees of thermal dissipation, with better dissipation coming from smaller particles. The use of smaller particles also allows application of the sintering paste by conventional printing methods to achieve fine-resolution features on the circuit materials. Sintering takes place in conventional ovens (Figure 3) in an air/nitrogen atmosphere and can be used for form silver sintered joints with thicknesses ranging from 50 to 100 µm, although thinner silver-sintered joints are becoming more popular. (For more information on silver sintering for the curamik ceramic materials, visit the Design Support Hub **(https://www.rogerscorp.com/pes/design/index.aspx)** and download a copy of the tech note "curamik® SUBSTRATES for Silver Sintering.")

ADVANTAGE processes also include treatment of DBC ceramic materials to achieve partial-discharge-free performance, essentially for high-power circuits at blocking voltages to 1.7 kV. DBC master cards are treated to close voids so that even at voltages to 3.8 kV, partial discharge is less than 10 pC. This elimination of voids in the ceramic material results in higher reliability and longer operating lifetimes for high-power circuit designs, including converters and inverters. Additional ceramic processes include laser drilling of holes with 1mm minimum diameter and tolerance of +0.05/-0.02 mm; engraving of text or numeric data matrix code onto a ceramic substrate for full traceability; etching of integrated copper steps and cavities; and organic surface treatment to help improve wire-bonding and soldering processes.

Process	Stencil Printing	Drying	Die Pick and Place	Sintering
Equipment	conventional printing equipment	conventional box oven	die placer with heated tooling	sinter press
Parameter	standard parameter	drying in air 10 min. at 100°C	die placement temperature 120°C	sinter pressure 5-30 Mpa sinter temperature 230°C sinter time 3 min. in air

Figure 3: Process flow for silver pastes with micro-particles

High-Temperature TIMs for Power Modules and Devices

The proliferation of the usage of power modules has driven the industry to push for higher performance and more demanding modules. This increase in performance is typically accompanied by higher power densities, hence higher thermal densities that need to be addressed. Significant improvements have been seen in all areas from the Semiconductors to packaging to software to better control the systems. Another area that has made significant progress in addressing these thermal challenges are the Thermal Interface Material (TIM) solutions. **Prashanth Subramanian, Market Development Manager, Advanced Energy Technologies LLC, a subsidiary of Graftech International, Lakewood, Ohio, USA**

TIMs are critical in getting the heat away from the modules into the cold plate / heat sink to quickly and effectively (Figure 1). The primary purpose of the TIM is to provide the path of least resistance (thermally) to enable heat to be moved away from the source and enable the semiconductors to perform to their rated capacity. While traditional silicon based devices would operate in the T_j ~ 100°C, they have significantly increased to well in to the high 100°Cs, it is well established that transistors lose over 10 % efficiency when junction temperatures increase by 50°C, placing greater emphasis on both removing the heat effectively while also operating in significantly elevated temperatures.

Traditionally this solution had been dominated by polymer based solutions like thermal grease, phase change material (PCM) etc which were effective in addressing temperatures in the range of ~120°C. While these materials have seen progress as well, most of them are limited to <150°C in operation, significantly reducing its effectiveness at higher temperatures. There is also a significant challenge to pumping and drying out due to thermal cycling, causing challenges at demanding environments like renewable energy, electric vehicles, locomotives, or inverters. Replacing a "worn-out" TIM is an expensive proposition and can lead to additional costs for maintenance and reliability of the system.

Metal based TIMs has also been around for a while, they tended to serve niche applications, as tend to have increased creep that can affect coverage, hence reliability. Graphite based TIMs traditionally have served the purpose of highly reliable long lasting TIMs (carbon is stable up to 400°C in an oxygen environment and ~3000°C in a non-oxidizing environment), but their usage has been restricted to small surface areas as they are stiff and cannot address large variations in flatness well.

A new generation of compressible graphite based TIM incorporates the compliance of thermal grease while providing the reliability of carbon at high temperatures. The eGRAF® HITHERM™ HT-C3200 Thermal Interface Material is the first of its kind of compressible graphite designed specifically to address the current and future needs of the power electronics market.

Device temperature

The temperature of the device ($T_{Resistor}$ or junction temperature) during the test is regarded as the key criteria to determine performance of the TIM solution. Thermal impedance is defined as the opposition to the flow of heat within an assembly. Figure 2 shows the performance of HT-C3200 in comparison with dry joint (no TIM), eGRAF® Hi-Therm HT-1210, and "Competitive

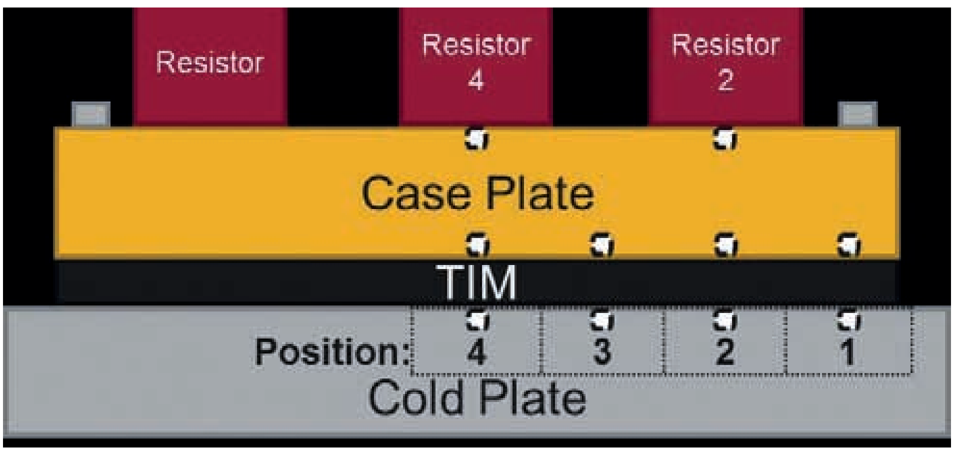


Figure 1: Schematic and temperature measurement locations in the assembly

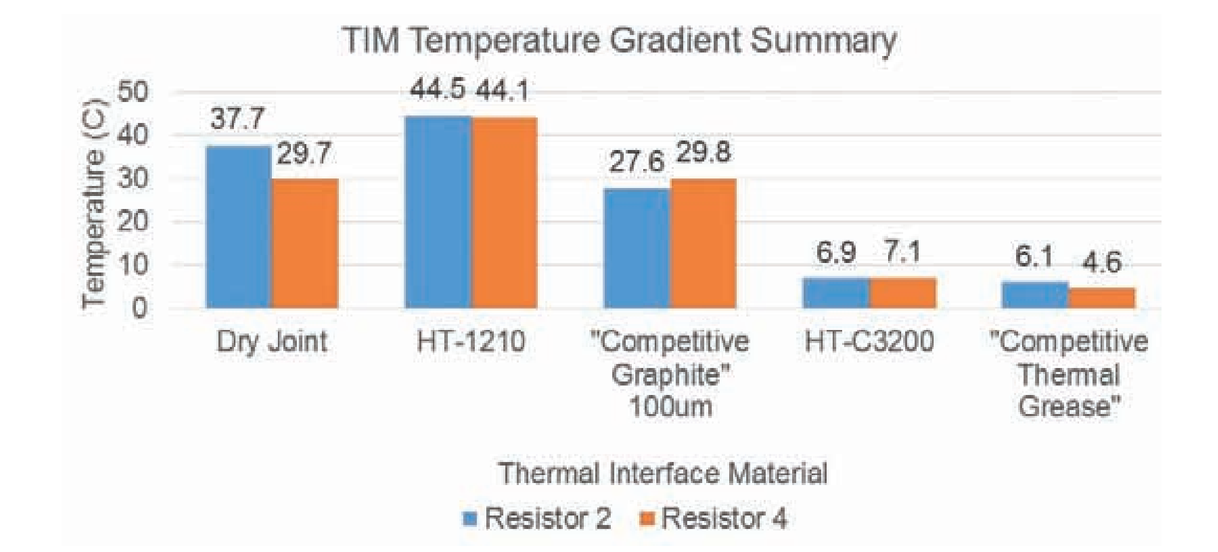


Figure 2: TIM temperature gradient through the thermal path

Graphite" - a commercially available 100 ?m thick graphite solution and "Competitive Grease" is a commercially available and popular silicone based solution and is widely used in the power electronics industry. The HT-C3200 shows comparable performance to grease while clearly outperforming both the HT-1210 and the dry joint. The temperature delta across the TIM shows the effectiveness of the heat transfer between the case plate and the cold plate and in turn the performance of the TIM. Temperatures were measured at four locations as described below in Figure 1.

Compressibility

One of the key advantages of using a grease like solution over a non-compressible foil like solution is the increased effective wetting aided by the ability of the material to flow and adjust to the flatness variations of the metal surfaces. Most rigid foil based solutions (including some graphite and metals) typically have less than 10 % compressibility and followability limiting their effectiveness in contacting both mating surfaces, hence allowing for air gaps that act as insulators.

For the foil based solutions to work more effectively, they must be able to effectively fill the variations in the bond lines between the mating surfaces. The HT-C3200 is an engineered graphite foil that can be compressed to about 70 % of its initial thickness under pressure (see **www.graftech.com/wp-content/uploads/2015/03/TDS319-HITHERM-HT-C3200.pdf**). This compressibility helps mimic the followability of the grease like substance while maintaining its ability to not pump-out under pressure. This purely graphite based solution does not pump out or dry out during thermal cycling or while applying pressure. This significantly improves the life of the material both during storage and during operation. Figure 3 shows the thickness of the material under compression. The difference in pressures between the edges and the center of the cold plate and case plate creates a bond line variation that can be between 50 and 100 µm based on the flatness of the metal surfaces, the torque applied and the thickness of the metal plates. The thickness was measured using a vacuum controlled thickness gauge.

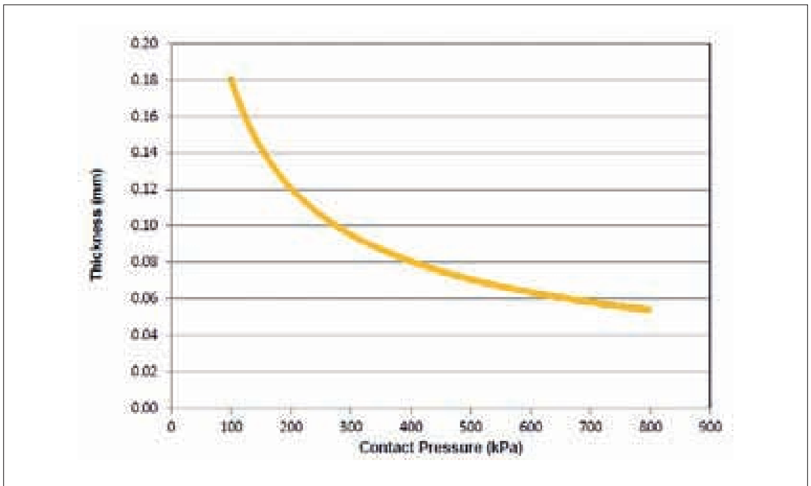


Figure 3: Thickness vs. pressure of TIM HT-C3200

Operating temperature

Most grease or Phase Change Material based TIMs have effective operating temperatures <150°C, the higher temperatures cause the material to dry out and lose its performance significantly. With the gradual but definite proliferation of Wide Band Gap material such as SiC and GaN based devices, the devices can operate comfortably in the 180°C to 220°C range, rending the current grease like solution inadequate. The HT-C3200 can operate in temperatures up to 400°C with no noticeable difference in performance. This graphite solution does not have the challenges like grease to pump out or dry out either during assembly or during operation.

Conclusions

The HT-C3200 is a highly engineered compressible graphite based TIM that provides both the surface wettability like grease while not having the same challenges with pump out and dry out that plague the long term performance of these paste like materials including Phase Change Materials. The HT-C3200 also does not require any dispensing equipment and is not messy in its application unlike the paste like

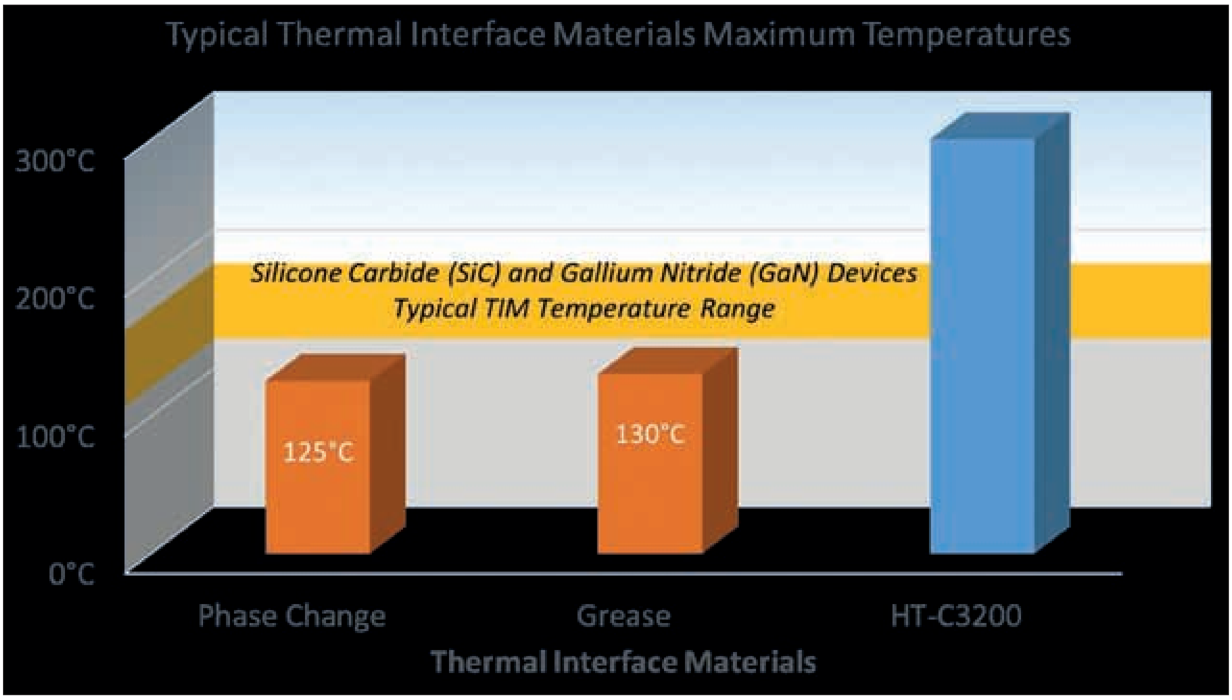


Figure 4: Thermal operating limits for TIMs

materials, enabling clean and easy assembly and maintenance options. The performance is comparable to the popular grease based solutions unlike the non-compressible foil based solutions including both graphite and metal based solutions. With the increase in the proliferation of the higher temperature Si based and the increase in the availability of SiC, GaN based modules, the need for a reliable, high performance TIM is critical. The HT-C3200 satisfies the most demanding needs of today and the future of power modules and other power devices.

Fast Heat Distribution Simulation And Visualization

A commonly used simulation method for heat distribution within the power module is the 3D FEM analysis. After the meshing of the solid model of the power module, entering power stimulus values and launching the simulation the heat distribution can be obtained. However the excitation signals are highly dependent on the application parameters. If an application parameter is changed the simulation must be run again, which can take a relatively long time for a full analyses. An alternative method is described below, that uses the linearity and superposition property of the heat equation for a quasi real time solution of the heat distribution problem. **Ernó Temesi, Application Engineering, and Vince Zsolt Szabó, Sr. Development Engineer, Vincotech. Hungary**

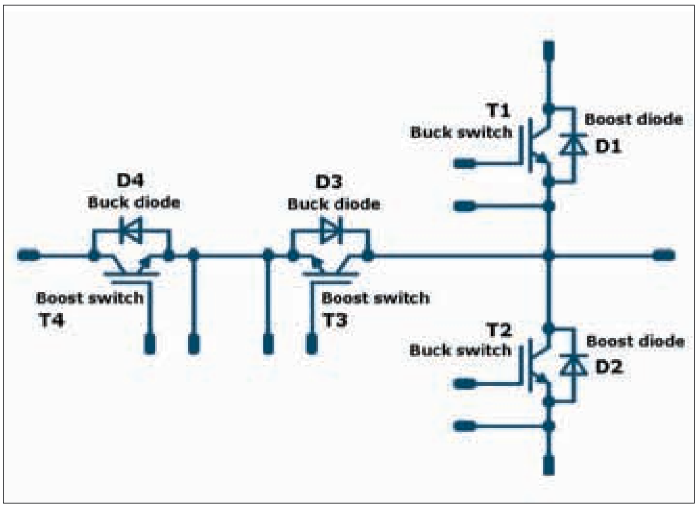


Figure 1: M260 schematic as a modeling example

The life time of power modules is inversely proportional to the operating temperature of the semiconductors. The semiconductors should work at possible lowest temperature in the given application to minimize the power losses and thus the size of the required cooling equipment.

The semiconductors produce heat during operation that increases the temperature of the semiconductor chip and have an influence on the operating temperature of the other chips placed near them as well. This is called heat coupling. In case of dense layout the coupled thermal resistance can be significant. It is difficult to measure the exact value of heat coupling between chips, however it is easy to calculate using 3D finite element simulation software.

Heat equation solution

The heat distribution can be defined with a partial differential equation which describes the distribution of heat (or variation in temperature) in a given region over time.

$$\frac{\partial T}{\partial t} = \alpha \left(\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2} \right) + \frac{1}{c_p \rho} q$$

where:

α - thermal diffusivity

$\frac{\partial T}{\partial t}$ - derivate of the temperature

$\left(\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2} \right)$ - Laplace operator (divergence of the gradient)

$\frac{1}{c_p \rho} q$ - heat source

From the equation arises the linear dependency between the heat source and the temperature rise:

$$q \rightarrow dT$$
$$2 * q \rightarrow 2 * dT$$

That is two times more heat will result in two times higher temperature rise. And the superposition of two heat sources:

$$q_1 \rightarrow dT_1$$
$$q_2 \rightarrow dT_2$$
$$q_1 + q_2 \rightarrow dT_1 + dT_2$$

That is the temperature rise generated by two heat sources is equal to the sum of the temperature rises generated by each heat source separately.

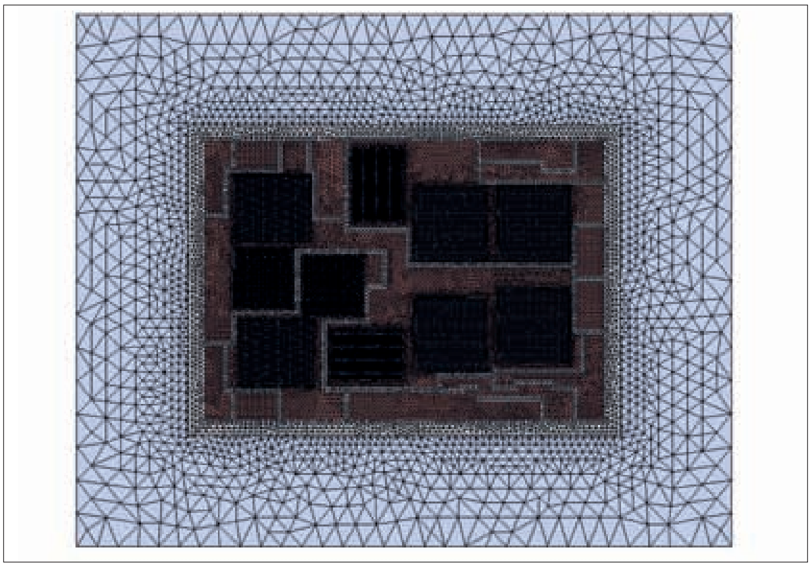
It is possible to modulate the temperature rise distribution caused by each heat source linearly with the actual power loss and finally superposition the temperature rises caused by all chips to get the total temperature rise distribution.

Temperature distribution and thermal resistance

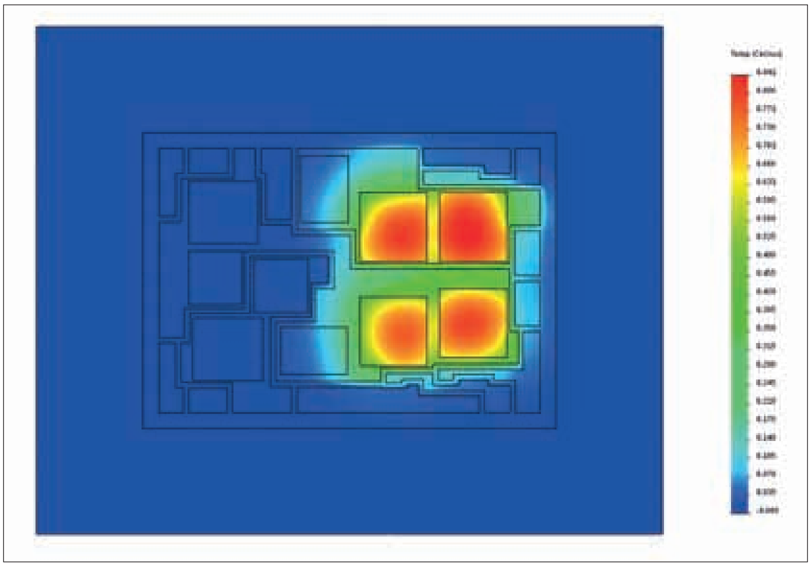
A three level MNPC inverter (M260) will be used as an example to show the procedure (Figure 1).

This module implements four different component electrical functions such as:

- 2 x buck switch (1200V; 2x40A chips paralleled)
- 2 x buck diode (600V; 75A)
- 2 x boost switch (600V; 75A)



RIGHT Figure 2: Mesh of the power module



LEFT Figure 3: Self R_{th} value of buck switch from 3D FEM simulation

$$\begin{bmatrix} 0{,}699 & R_{th_{buckSW-buckD}} & R_{th_{buckSW-boostSW}} & R_{th_{buckSW-boostD}} \\ R_{th_{buckD-buckSW}} & 0{,}1585 & R_{th_{buckD-boostSW}} & R_{th_{buckD-boostD}} \\ R_{th_{boostSW-buckSW}} & R_{th_{boostSW-buckD}} & 0{,}127 & R_{th_{boostSW-boostD}} \\ R_{th_{boostD-buckSW}} & R_{th_{boostD-buckD}} & R_{th_{boostD-boostSW}} & 0{,}1331 \end{bmatrix}$$

LEFT Figure 4: Self R_{th} in the matrix

- 2 x boost diode (1200V; 50A)

The following steps need to be done to get the heat distribution within the module:

1) Importing the modul layout into 3D FEM simulator;
2) creating the mesh (Figure 2);
3) exciting the chips of the same electrical functions by the same load conditions with unity power (1 W);
4) running one simulation for each function separately;
5) get maximum temperature to define R_{th} of chip and the temperature distribution (Figure 3).

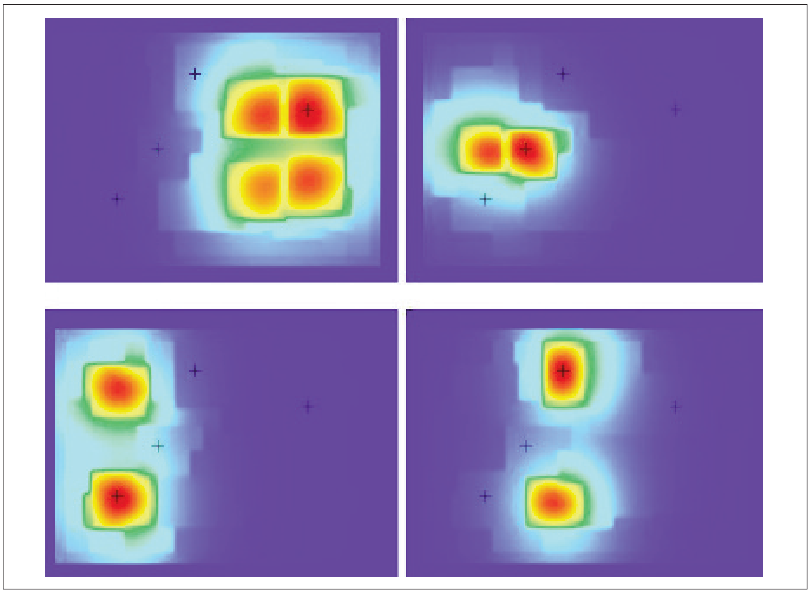
The coordinates of maximum heated points can be obtained separately for the different electrical functions and the values define the self R_{th} values in the heat coupling thermal resistance matrix (diagonal) – see Figure 4.

The remaining values (coupled R_{ths}) in the matrix describes the measure how the components heat each other.

Defining cross-coupled thermal resistances

Knowing all the chip positions and the temperature rise caused by the neighboring chips the coupled R_{th} values can be also gained by reading color codes of the different positions for all electrical functions (Figure 5). The black crosses indicate the coordinates of the virtual maximum temperature points.

The R_{th} matrix gives an easy and fast way for calculating each chip temperature of the power module under any load



LEFT Figure 5: Maximum points for different electrical functions

$$\begin{bmatrix} T_{j_{buckSW}} \\ T_{j_{buckD}} \\ T_{j_{boostSW}} \\ T_{j_{boostD}} \end{bmatrix} = \begin{bmatrix} 0{,}699 & 0{,}0393 & 0{,}0087 & 0{,}1179 \\ 0{,}0099 & 1{,}585 & 0{,}3269 & 0{,}0693 \\ 0{,}007 & 0{,}2676 & 1{,}127 & 0{,}0708 \\ 0{,}0415 & 0{,}183 & 0{,}1081 & 1{,}331 \end{bmatrix} \cdot \begin{bmatrix} P_{buckSW} \\ P_{buckD} \\ P_{boostSW} \\ P_{boostD} \end{bmatrix} + \begin{bmatrix} T_{sink} \\ T_{sink} \\ T_{sink} \\ T_{sink} \end{bmatrix}$$

Figure 6: Self (black) and cross-coupled (red) R_{th} matrix

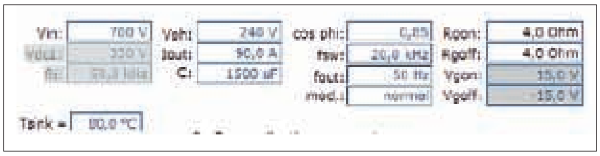


Figure 7: Application parameters

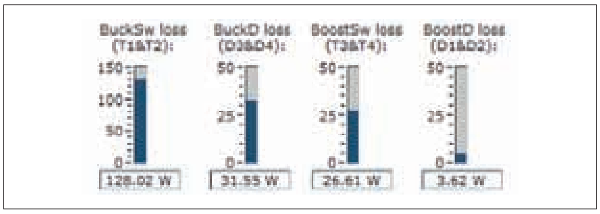


Figure 8: Heat power excitation values

$$\begin{bmatrix} T_{j_{buckSW}} \\ T_{j_{buckD}} \\ T_{j_{boostSW}} \\ T_{j_{boostD}} \end{bmatrix} = \begin{bmatrix} 0{,}699 & 0{,}0393 & 0{,}0087 & 0{,}1179 \\ 0{,}0099 & 1{,}585 & 0{,}3269 & 0{,}0693 \\ 0{,}007 & 0{,}2676 & 1{,}127 & 0{,}0704 \\ 0{,}0415 & 0{,}183 & 0{,}1081 & 1{,}331 \end{bmatrix} \cdot \begin{bmatrix} 128{,}02 \\ 31{,}55 \\ 26{,}61 \\ 3{,}62 \end{bmatrix} + \begin{bmatrix} 80 \\ 80 \\ 80 \\ 80 \end{bmatrix}$$

Figure 9: Full matrix equation

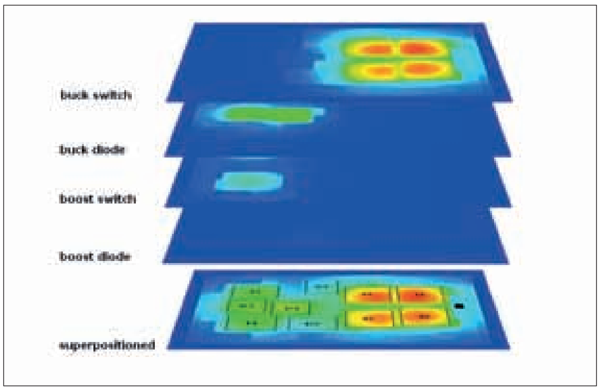


Figure 10: Layered and superpositioned thermal distributions

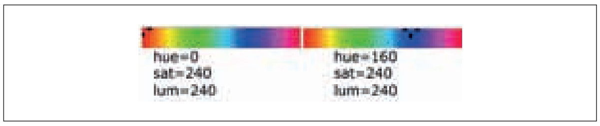


Figure 11: Define linear color range

condition (Figure 6).

Additionally by superimposing the temperature distributions caused by all functional components the total temperature distribution within the module is obtainable. The heating power for each function types is obtained from flowTHERM-M260 simulation launched with given application parameters (Figure 7). Heat powers for the specific application case is shown in Figure 8.

The temperature values for the functions are determined by substituting the heat power excitation values (Figure 9). By the superposition of all distribution layers caused by the functional components the total distribution can be gained (Figure 10). In the final distribution the colors are normalized to the T_{sink} heatsink (min) and to the allowed T_j maximal chip temperature (max) as shown in Figure 11. Thus each pixel temperature of the superpositioned picture can be read by a resolution of 1/160 due to the hue=0 ($T_{jmaxtot}$) and hue=160 (T_{sink}) range.

Conclusions

An alternative method as described above, which uses the linearity and superposition property of the heat equation, allows building power module loss and temperature simulators with very fast response to adjustments or changes in the application parameters. The simulation tool can easily be programmed to map the relations between virtual junction temperature of semiconductor chips inside the power module and a temperature sensing device (Figure 12). This information used in a real time temperature calculation of the application can be used for an accurate estimation of the virtual chip temperatures. As next steps the visualization of the fluctuation of the chip temperatures with the converters basic frequency is to be solved.

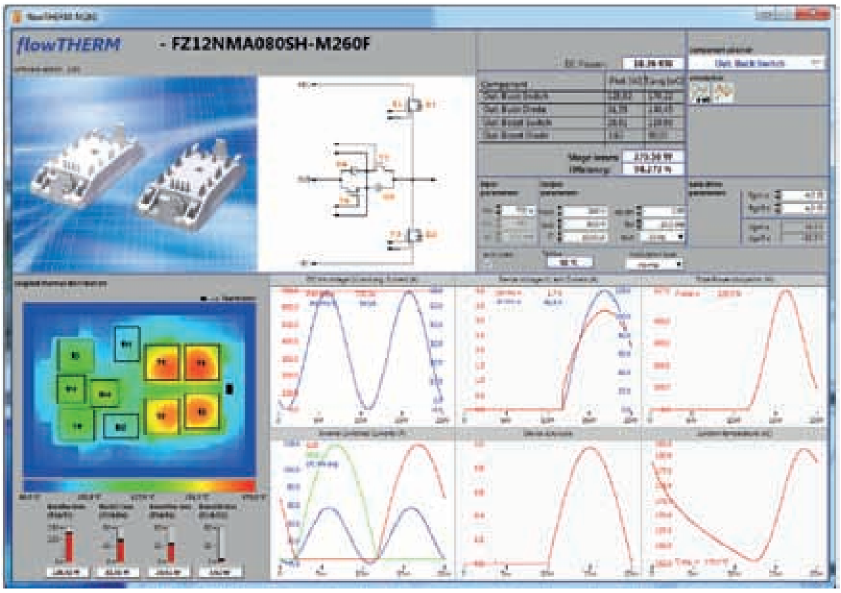


Figure 12: Power module simulator with thermal distribution inside

Multilayer Ceramic Capacitors in Automotive

Modern EV's, HEV's and PHEV's are sparking a revolution in the capacitor technology used in the control electronics. Higher temperatures inside the control circuits mean that conventional plastic film capacitors are no longer suitable for all applications and ceramic MLCC's are now being increasingly used, with the added benefits that MLCC's are generally surface mount direct to boards, yielding greater efficiency of assembly and allowing shorter circuit tracks with lower inductance. In many cases this last point allows lower capacitance values to be used, meaning that smaller components or less components can be used.

Steve Hopwood, Senior Applications Engineer, Knowles Capacitors R & D, Norwich, UK

According to Figure 1, MLCCs are being used extensively in modern cars. In considering the basic requirements for MLC chips, first we must consider the necessity for all components to meet the demanding requirements of AEC-Q200, the "Stress Test Qualification for Passive Components" laid down by Automotive Electronics Council (AEC) Component Technical Committee. These subject components to a set of rigorous tests to determine the basic reliability in application. Generally, the most severe tests for MLCCs relate to the mechanical stresses induced by the board bend and thermal cycling requirements, designed to ensure a component is capable of withstanding poor processing and handling, as well as the mechanical stresses experienced in application. Poor mechanical design and material selection can result in a component suffering from a mechanical crack which may result in a short circuit at a later date (see Figure 2).

Avoiding cracks due to mechanical stress

Knowles Syfer brand were the first MLCC manufacturer to develop a flexible termination system for their surface mount capacitors - FlexiCap™. This technology

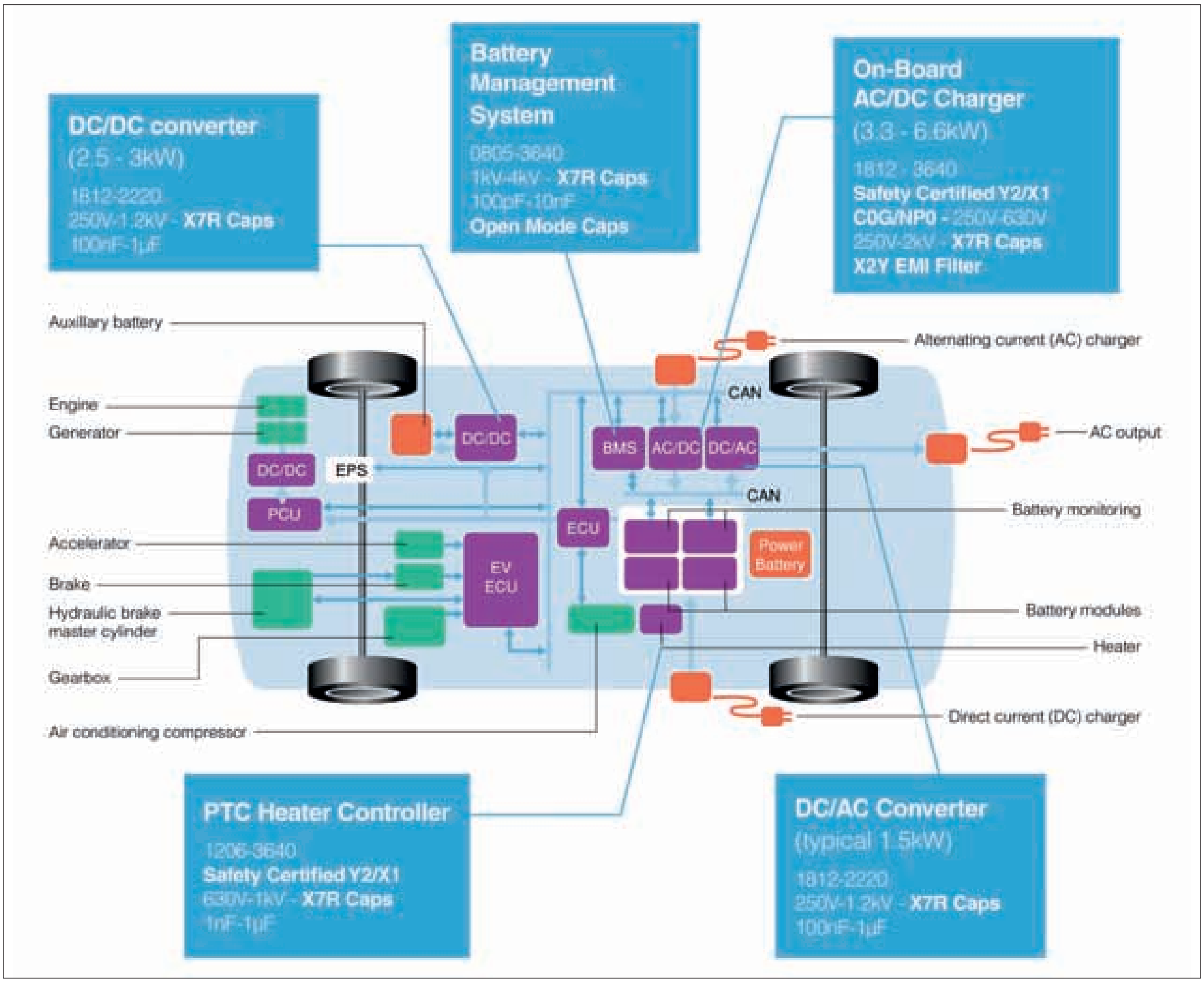


Figure 1: Some examples of locations where MLCCs are now being used in (electric) automotive applications

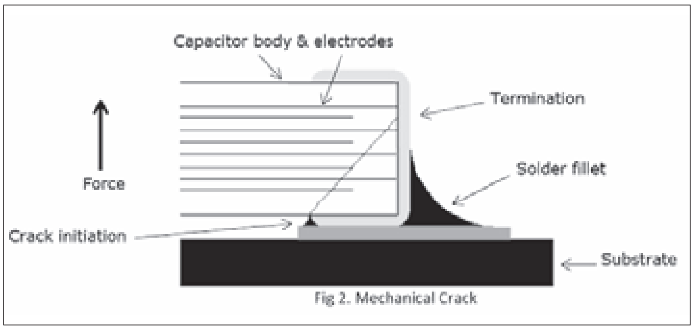


Figure 2: Mechanical crack mechanism

makes it possible for large case size MLCC's, up to 3640, to be approved to the AEC-Q200 requirements by isolating the ceramic from the mechanical stresses. This termination is essential to ensure type II (X7R, X5R & X8R) dielectrics meet the requirements of the AEC-Q200 specification, although it is also available on selected type I (C0G / NP0) dielectric ranges.

Alongside the termination, it is possible to design special internal electrode configurations to reduce the likelihood of catastrophic electrical failure in the case a crack does occur. Open-mode MLCC's (Figure 3) have the internal electrode patterns pulled back from the opposing end of the chip, meaning if a crack is induced, it is much less likely to propagate through an area of active overlap and cause an electrical short circuit. Tandem-mode designs (Figure 4) use a sequential electrode design, placing two capacitors in series within a single MLCC. Each capacitor is designed to withstand the full rated voltage of the component, so in the case of a failure in one, the capacitor the other end can withstand the full rating and the component continues to work, albeit at a reduced capacitance value. These recent developments have made the reliability of surface mount MLCCs exemplary, which in turn has seen an increase in their use throughout a car's electronics.

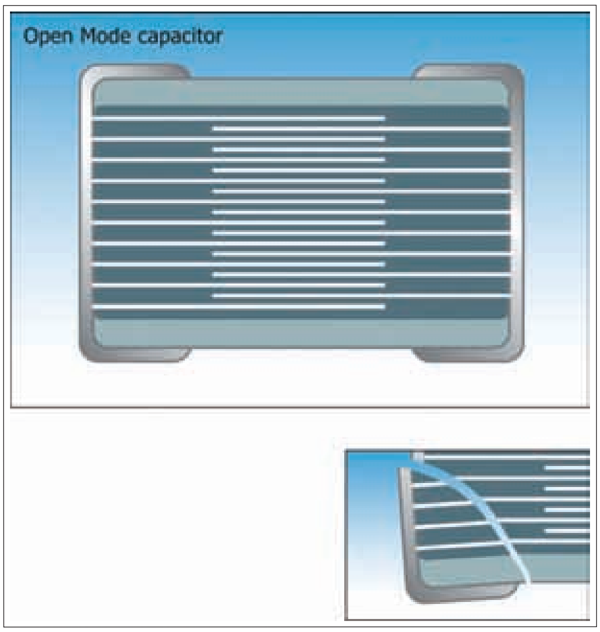


Figure 3: Open-mode MLCC's have the internal electrode patterns pulled back from the opposing end of the chip

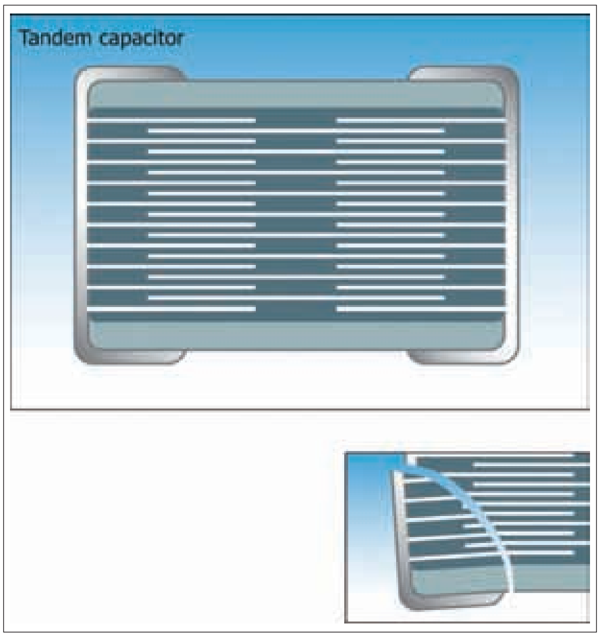


Figure 4: Tandem-mode designs use a sequential electrode design, placing 2 capacitors in series within a single MLCC

One noticeable trend of late has been the increasing ambient temperature of the electronic systems on board. Airflow, required for cooling, is more closely controlled as aerodynamic drag is more of a concern; miniaturization drives enclosures even smaller; the complexity of on-board systems has reached levels that could not have been imagined and, with the advent of battery and power train control systems, components are being asked to handle higher power ratings.

MLCCs with X8R classification (rated -55°C to +150°C) were developed many years ago specifically for automotive applications, but have always had poor volumetric efficiency compared to other dielectrics. Recent new dielectric systems are now addressing this and recent developments have seen significant improvements in the available ranges. This factor is actually a side effect of the new dielectrics being developed for environmental reasons, which have also seen the first 100 % lead free X8R capacitors reach the market.

Coming soon

Looking to the future, temperatures will continue to rise as passive components are moved closer to the power electronics, reducing the circuit tracks and therefore the effective inductance but also allowing lower capacitance values to be specified. Here, the automotive industry can look to developments in the oil exploration down-hole industry, which has seen 200°C MLCCs arrive on the market. For the first time, these are available with low-cost plated, nickel barrier, termination systems allowing the full requirements of aged solderability and dissolution of termination specifications to be met. These systems meet the full requirements of the AEC-Q200 specification on C0G type I dielectrics. Future developments will see available temperature ranges increase further, with 250°C rated parts already on the horizon.

Electric vehicles require higher voltages

Early on we stated that there was a revolution in the capacitor technology used in the control electronics being driven by modern EVs, HEVs and PHEVs. Of course, MLCCs have been used in automotive applications for years, but the big change that is being seen is the voltage rating and size of

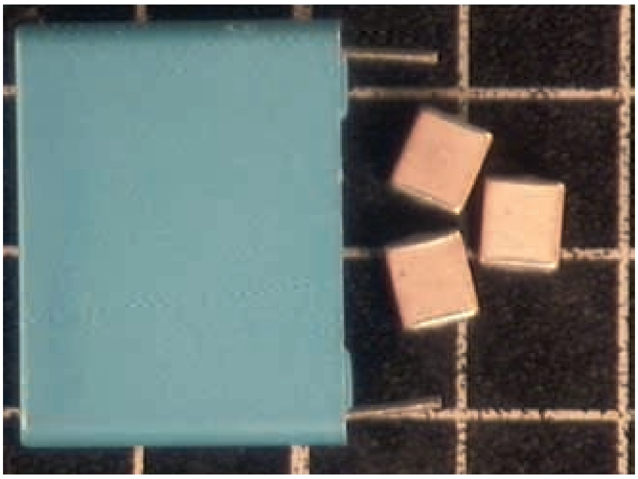


Figure 5: Examples of 400 V DC 1 µF Polypropylen film and 630 V 1 µF MLCC capacitors (right)

components now being used. Not so long ago, there was a rule of thumb that you didn't place an MLCC bigger than 1210 (0.12" x 0.10") directly onto a board due to the risks to reliability. The developments mentioned above have smashed this ceiling and it is now not unusual to see capacitor as large as 0.5" square and up to 0.3" thick placed directly onto substrates.

The size increase is being driven by the need for higher voltages, higher capacitance values and higher AC ripple currents (i.e. power dissipation). With reference to Figure 1, it can be seen that typical MLCC voltage in EV is 250 V DC to 2 kV DC, but 4 kV DC and higher is required in some cases, particularly to meet impulse or surge requirements. Typical capacitance in this application is 100 nF to 4.7 µF. The reason for these high values is the manner in which MLCCs are now being used to replace film capacitors in filtering circuits with high DC bias voltage and high ripple current requirements. Ceramic will never eradicate film capacitors from automotive applications as plastic film offers much higher capacitance ranges, but where possible an MLCC can offer a much smaller component size and weight for the equivalent plastic film (Figure 5).

Developments continue to drive the size of MLCC's ever smaller, and new dielectric systems are now obtaining impressive volumetric efficiency. The 0.22" x 0.20" x 0.18" 630 V DC rated 1 µF X7R MLCC is a typical example that is now in use in EV battery management systems. This capacitance / voltage combination is only possible due to Knowles patented StackiCapTM technology which allows increased component thickness without the electrostrictive failure mode that plagues thicker MLCC's.

In PHEV's and PEV's, it is also important that the appropriate safety rated class X & Y capacitors are used on the circuits directly connected to the mains and elsewhere were an electric shock situation could possibly occur. MLCCs are capable of safety approvals up to class Y2 and all Knowles safety ranges are also AEC-Q200 certified.

Of course it is important that the capacitor characteristics and performance under real life operating conditions are known and to this extent Knowles are investing heavily in research and development and working closely with a number of automotive electronics suppliers to assist with applications advice.

Finally, we can look forward to some new dielectric developments that are specifically aimed at the future requirements of automotive power electronics. An example of one such development is shown in Figure 6 - this particular dielectric development is currently being developed under the European Union's FP7 Clean Sky Joint Technology Initiative with project partners NPL and Euro support. These materials are at the R&D stage and promise to offer more stability under voltage stress, less dielectric losses and significantly reduced self-heating of the component under high RMS ripple current. These new dielectrics are already undergoing BETA trials in automotive applications in case sizes as large as 0.4" x 0.4" x 0.2", typical voltage and capacitance ratings of 600 V at 1.7µF.

Conclusion

MLCC's are experiencing a boom in automotive applications as their use expands into EV related power electronic applications. Larger case sizes and higher voltages are promoting replacement of film capacitors with the advantages of lower inductance, smaller case size and higher temperature ratings. New dielectric developments over the next 12 months will push MLCC's into further applications with their lower loss and more stable characteristics.

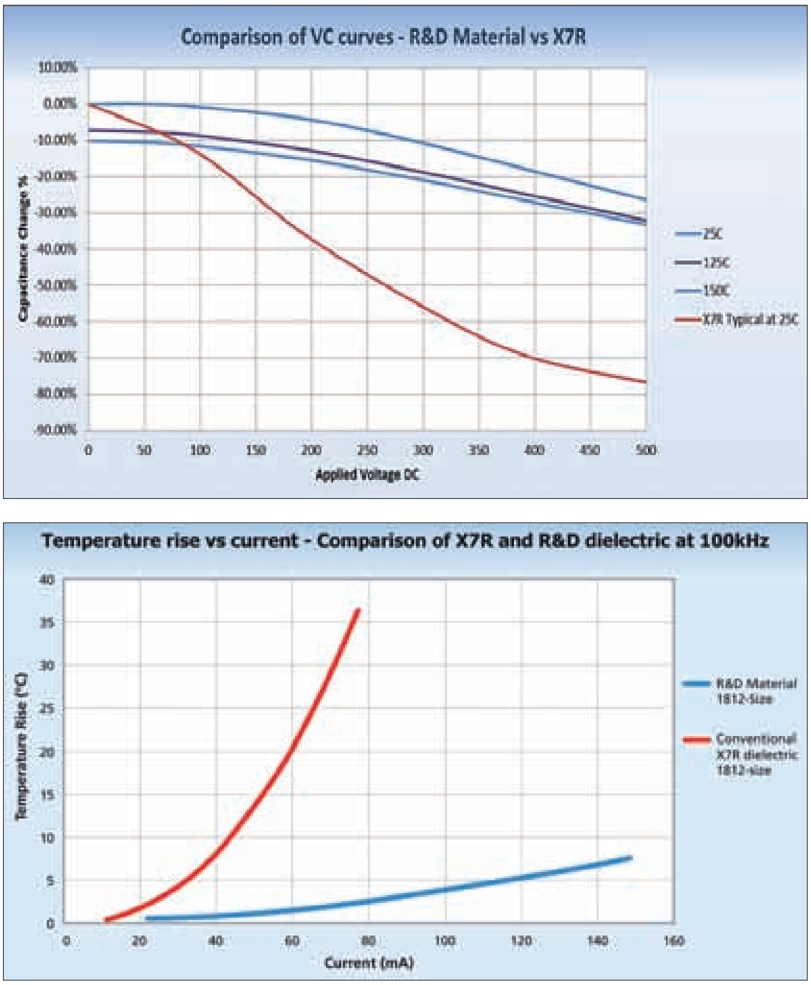
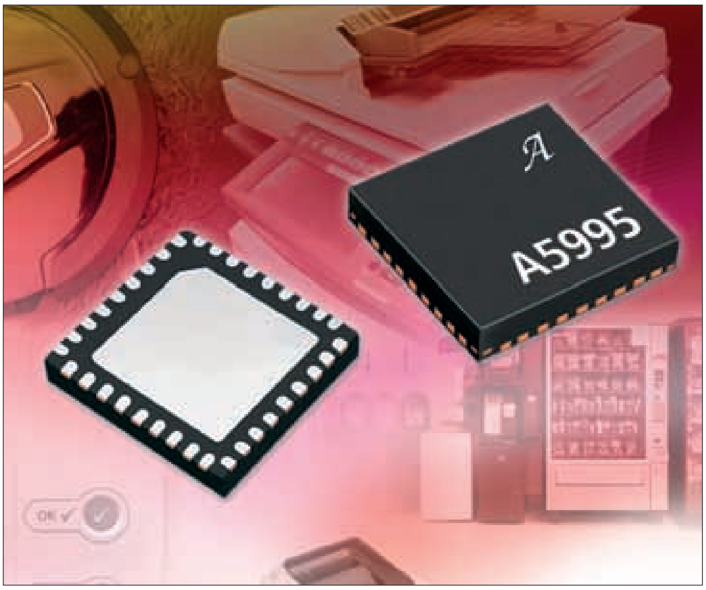


Figure 6: Dielectric development being developed under the European Union's FP7 Clean Sky Joint Technology Initiative, comparison of VC curves (top) and temperature rise versus current (above)

Dual Full-Bridge PWM Motor Driver IC



Allegro MicroSystems Europe has announced a new 40 V dual full-bridge driver A5995 capable of driving two DC motors with outputs rated up to 3.2 A. The device includes fixed off-time pulse-width modulation (PWM) regulators for current control. Each DC motor can be controlled in forward, reverse, coast and brake modes with industry standard PHASE and ENABLE inputs. Fast or slow PWM current decay is selected via the MODE input. Protection features include thermal shutdown with hysteresis, under-voltage lockout (UVLO), crossover current, and over-current protection. Low current sleep mode is included to improve efficiency. The A5995 is supplied in a leadless 6 mm ? 6 mm ? 0.9 mm, 36-pin QFN package with exposed power tab for enhanced thermal performance. The package is lead (Pb) free, with 100% matt-tin leadframe plating.

www.allegromicro.com

Quasi-Resonant PWM Controller for Power Adapters

The AP3301 quasi-resonant (QR) PWM controller from Diodes enables the implementation of cost-effective power supplies meeting DOE6/COC Tier 2 efficiency requirements at all load levels. Targeting the key market of AC/DC adapters for set-top box and gaming console applications, this controller also meets the auxiliary power requirements of ATX/BTX computer motherboards and is suited for use in open-frame switching power supplies. Multiple operating modes allow the AP3301 to achieve optimal efficiency at different load levels: Under low- or no-load conditions, the IC uses a burst mode to minimize standby power consumption while operating at a minimum switching frequency of approximately 20 kHz to avoid audible noise. At intermediate loads, a valley-lock QR mode with frequency foldback improves efficiency and EMI performance. For heavy loads, or under low-line input conditions, the controller enters a continuous conduction mode (CCM) at a fixed 62 kHz switching frequency. A built-in frequency dithering function helps reduce EMI emission in both CCM and QR modes. With just minor changes to external components, the SOT-26 packaged AP3301 provides a pin-compatible replacement solution for Diodes' existing AP3105/AP3125 PWM controllers. The AP3301 is priced at $0.20 each in quantities of 1k units.

www.diodes.com

OptiMOS5 150 V Delivers Reduced in On-Resistance

Aiming at high efficiency designs and applications, Infineon Technologies introduces the OptiMOS™ 5 150 V portfolio. The new 150 V product family is especially optimized for high performance applications which require low charges, high power density and yet high ruggedness. It is an important contributor to Infineon's system solutions for low voltage drives, synchronous rectification in telecom rectifiers and brick converters as well as solar power optimizers. Compared to the next best alternative, OptiMOS 5 150 V offers a reduction in on-state resistance of 25 % in a SuperSO8 package and the FOM is improved by up to 29 % over the previous generation. Increased commutation ruggedness is provided by the ultra-low reverse recovery charge, which is 72 % lower than the next best alternative in SuperSO8.

www.infineon.com/optimos5-150V

High-Voltage Transducers for Traction Applications

LEM introduces the DVM series for insulated nominal voltage measurements in traction applications. This family of devices spans the range from 600-4200 V RMS. Despite achieving very high levels of isolation with a safety insulation voltage of 12 kV, the DVM transducer is compact, measuring only 138 mm x 63.4 mm x 69 mm. It is fully compatible and outperforms the previous generation of transducers in terms of functions and performance with new improved levels of accuracy and temperature stability, thus greatly simplifying retrofits. DVM is also suitable for base mounting, but with slightly different outline dimensions to take into consideration for primary and secondary connections locations for example. The DVM is 30 % smaller in height, occupies 25 % less volume and is 56 % lighter. LEM developed the DVM to be fully compliant with the International Railway Industry Standards (IRIS), providing engineers in the railway industry, who are working with both rolling stock and sub-stations, with a versatile new transducer that is equally applicable to measuring network voltages, or the main converter DC link on-board trains. The feature set of the DVM voltage transducer also allows for a broad range of medium to high voltage measurements in industrial markets.

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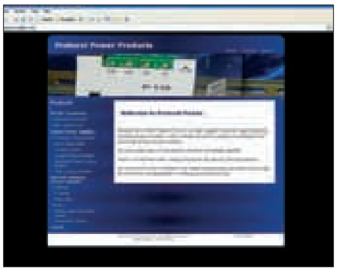

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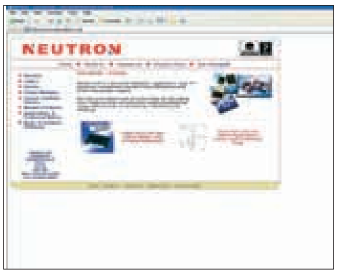

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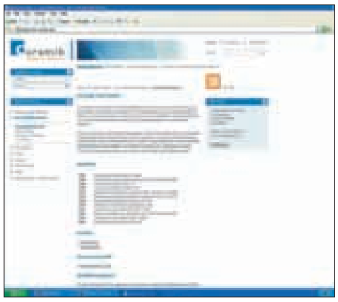

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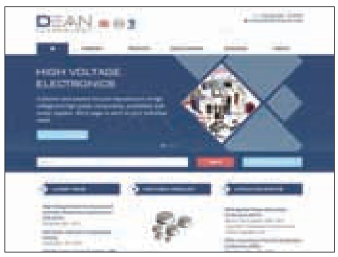

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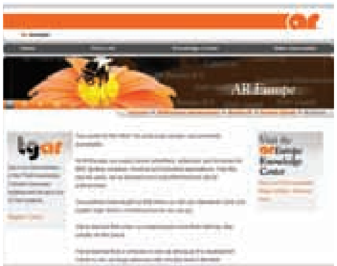

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