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WIRELESS POWER

GaN FETs Enable Large Area Wireless Power Transfer

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COVER STORY

GaN FETs Enable Large Area Wireless Power Transfer

To ensure widespread adoption, wireless power systems need to move beyond small charging pads and become active power sources over large surface areas. For magnetic resonant systems, this demands fundamental changes in coil technology, system architecture, and power amplifiers. Gallium nitride based amplifiers have proven capable of delivering 60 W with greater than 90 percent efficiency into the transmit coil over a wide load range.
The key to large area wireless power lies in both innovative coil technology and high power (>?60?W) amplifiers enabled by eGaN FETs. Large area wireless power coils have inherently different characteristics than traditional coils in that they have lower increase in inductance per increase in area, shorter magnetic field radiation, and are more immune to imaginary impedance shifting. A multi-coil, multi-amplifier approach using three eGaN FET-based, 60?W capable differential-mode amplifiers was constructed and tested. Both the class?E amplifier and the ZVS?class?D exhibited greater than 90 % efficiency at full power. Further improvements can be expected from the ZVS?class?D when fitted with lower RDS(on) eGaN FETs. The work presented in this article underscores the challenges ahead for large area wireless power systems design to achieve high-efficiency with high-power amplifiers. More details on page 24.

Cover image supplied by
Efficient Power Corporation, USA

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Market News

PEE looks at the latest Market News and company developments

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Industry News

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A System-Level Power Architecture Design Tool

Modern electronic systems have an increasing level of complexity. There can be a large number of power rails and supply solutions on a system board to power many different loads. Before choosing or designing each individual power supply, the system hardware engineer first needs to understand the system power needs and then architect the system power tree accordingly to optimize the power management system efficiency, size and cost. Due to the complexity of the system, sometimes system-level power optimization is not a trivial task. An intuitive system-level design tool addresses this need. **Henry Zhang, Applications Engineering Manager, and Tim Kozono, Applications Engineer, Linear Technology Corporation, USA**

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Products

Product update

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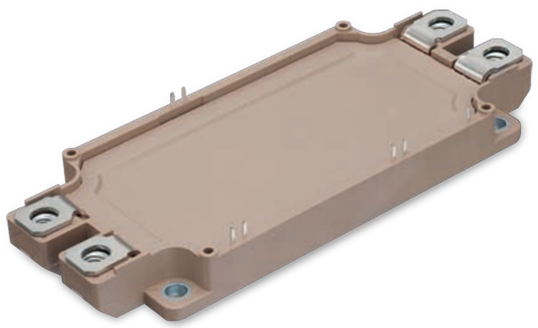
Website Product Locator

7th Generation Modules

Dual XT & Premium Dual XT



Dual XT – More power, lower losses

FEATURES

- 7G IGBT & FWD
- New internal layout
- Higher reliability
- Improved silicone gel
- Solder or Mini press-fit pins

Premium Dual XT – High power density

FEATURES

- 7G IGBT & FWD
- Advanced bond wire design
- High thermal conductive ceramic substrate
- Package material with CTI > 600
- V_{iso} = 4kV
- Improved silicone gel
- Solder or mini press-fit pins

www.fujielectric-europe.com

More Opportunities In 2018

A global transition to 100 percent renewable electricity is not a long-term vision, but already a tangible reality, a new groundbreaking study by the Lappeenranta University of Technology (LUT) and the Energy Watch Group (EWG) shows. Total levelized cost of electricity on a global average for 100 % renewable electricity in 2050 is € 52/MWh compared to € 70/MWh in 2015. And a transition to 100 % renewables would bring greenhouse gas emissions in the electricity sector down and drastically reduce total losses in power generation. It would create 36 million jobs by 2050, 17 million more than today.

Power semiconductors are a major contributor to increase renewable electricity generation and improved efficiency. According to market research global power semiconductor revenues grew by 3.9 percent in 2016, reversing a 4.8 percent decline in 2015. The automotive and industrial segments were particularly strong in 2016, with power semis in automotive growing by 7.0 percent and industrial by 5.0 percent. In the broad industrial sector the drive for energy efficiency improvement led to growth in renewable energy (solar and wind inverters), building and home control, and factory automation applications. This market conditions are highlighted by Infineon's fiscal year 2017/18 figures. Alongside electro-mobility, driver assistance systems and renewable energy, a further pillar of growth is its industrial business – including drives for increasingly automated production machinery and robotics. Demand is also strong for our highly efficient chips, by example for fast chargers for tablets. With future technologies such as Silicon Carbide and Gallium Nitride, Infineon is paving the way for tomorrow's success, CEO Reinhard Ploss underlined. Adjusted for exchange rate effects, growth in the 2018 fiscal year could even reach the double-digit mark. For the 2018 fiscal year, based on an assumed exchange rate of US dollar 1.15 to the Euro, Infineon expects year-on-year revenue growth of about 9 percent. The automotive segment is predicted to grow at a meaningfully faster rate than the Group average.

An explosion particularly of the GaN market with 84 percent CAGR between 2017 and 2022 is expected. In 2016 the power GaN market reached $ 12 million - it is still a small market compared to the impressive $ 30 billion Silicon power semiconductor market. However its expected growth in the short term is showing the enormous potential of the power GaN technology based on its suitability for high performance and high frequency solutions. LiDAR, wireless power and envelope tracking are high-end low/medium voltage applications, and GaN is the only existing technology able to meet their requirements, according to market researcher Yole. The power supply segment is still the biggest application for GaN. The data center market is adopting GaN solutions with a phenomenal speed, driving a plus 110 percent CAGR for power supplies through to 2022. Existing solutions from Texas Instruments and EPC for data centers, consisting of a DC/DC converter and point of load supply that steps down the voltage from 48 V to 1.2 V in a single chip, will propel the market. AC/DC power adapters for laptops or smartphones can be also implemented with GaN power IC solutions, which further reduces the size and cost of the system.

What new applications GaN FETs enable is shown in our cover story. The key to large area wireless power lies in both innovative coil technology and high power (> 60 W) amplifiers enabled by eGaN FETs. Large area wireless power coils have inherently different characteristics than traditional coils in that they have lower increase in inductance per increase in area, shorter magnetic field radiation, and are more immune to imaginary impedance shifting. A multi-coil, multi-amplifier approach using three eGaN FET-based, 60 W capable differential-mode amplifiers was constructed and tested. Both the class E amplifier and the ZVS class D exhibited greater than 90 % efficiency at full power. Further improvements can be expected from the ZVS class D when fitted with lower on-resistance eGaN FETs. The work presented in this article underscores the challenges ahead for large area wireless power systems design to achieve high-efficiency with high-power amplifiers.

Enjoy reading of this issue – see you next year!

Achim Scharf
PEE Editor

Renewable Electricity Worldwide is Feasible and Cost-Effective

A global transition to 100% renewable electricity is not a long-term vision, but already a tangible reality, a new groundbreaking study by the Lappeenranta University of Technology (LUT) and the Energy Watch Group (EWG) shows. The study was presented on November 8, 2017 during the Global Renewable Energy Solutions Showcase event (GRESS) on the sidelines of the United Nations Climate Change Conference COP23 in Bonn.

The results of the study are revealing: A global electricity system fully based on renewable energy is feasible at every hour throughout the year and is more cost effective than the existing system, which is largely based on fossil fuels and nuclear energy. Existing renewable energy potential and technologies, including storage can generate sufficient and secure power to cover the entire global electricity demand by 2050. Total levelized cost of electricity (LCOE) on a global average for 100 % renewable electricity in 2050 is €52/MWh (including curtailment, storage and some grid costs), compared to €70/MWh in 2015. "A full decarbonization of the electricity system by 2050 is possible for lower system cost than today based on available technology. Energy transition is no longer a question of technical feasibility or economic viability, but of political will", Christian Breyer, lead author of the study, LUT Professor of Solar Economy and Chairman of the EWG Scientific Board said.

A transition to 100 % renewables would bring greenhouse gas emissions in the electricity sector down and drastically reduce total losses in power generation. It would create 36 million jobs by 2050, 17 million more than today. "There is no reason to invest one more Dollar in fossil or nuclear power production", EWG President Hans-Josef Fell said. "Renewable energy provides cost-effective power supply. All plans for a further expansion of coal, nuclear, gas and oil have to be ceased. More investments need to be channeled in renewable energies and the necessary infrastructure for storage and grids. Everything else will lead to unnecessary costs and increasing global warming."

www.energywatchgroup.org

Power Semiconductor Sales Accelerate

Global power semiconductor revenues grew by 3.9 percent in 2016, reversing a 4.8 percent decline in 2015, according to IHS Markit. The industry megatrends of vehicle electrification, advanced vehicle safety, energy efficiency and connected everything will continue to drive growth over the next five years.

All categories of power semiconductors (power discretes, power modules, and power integrated circuits) were up for the year, with the discretes market seeing the biggest jump. Sales in all regions increased, with China revenues topping the list. IHS Markit expects the market to grow by 7.5 percent in 2017, to $38.3 bill and achieve yearly increases through 2021. "IHS Markit predicts that the compound-average annual growth rate (CAGR) from 2016 – 2021 will be 4.8 percent. Regionally, the highest growth is projected in China, at 6.0 percent CAGR, followed closely by the rest of Asia including Taiwan, Europe, Middle East and Africa, and the Americas – all with projected growth over 5 percent", commented senior analyst Kevin Anderson.

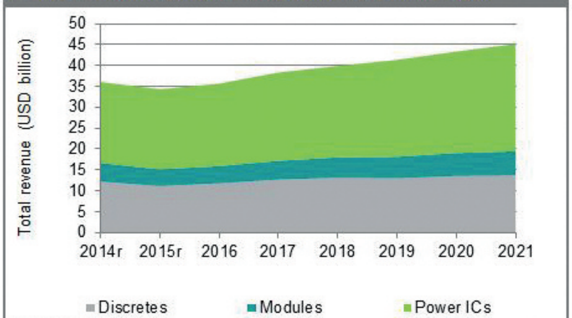
Automotive and industrial lead the way

The automotive and industrial segments were particularly strong in 2016, with power semis in automotive growing by 7.0 percent and industrial by 5.0 percent. Advanced driver assistance systems (ADAS) – such as blind-spot detection, collision avoidance, and adaptive cruise control – are moving from luxury to mid-level vehicles, driving double digit increases for power semiconductors in that category. Power semiconductors, especially power modules and discretes also saw sharp gains as the number of cars equipped with inverter systems for advanced start/stop and hybrid powertrains increased. In particular, power modules for cars and light trucks jumped more than 29 percent in 2016.

In the broad industrial sector the drive for energy efficiency improvement led to growth in renewable energy (solar and wind inverters), building and home control, and factory automation applications. Revenues from home appliances in the consumer segment also grew nicely as advanced motor control systems found their way into white goods, fans, kitchen, and cleaning products. Despite good gains, other categories were flat to down. Power module sales for industrial motor drives, a large sub-segment, slid 1.1 percent and modules for traction applications were down 17.5 percent for the year. Power ICs for consumer application declined 4.9 percent while power discretes for lighting applications were off 2.7 percent.

www.ihsmarkit.com

Power semiconductor market by major device type



r = revised since 2016 report
Source: IHS Markit
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Power GaN Opens New Market Opportunities

"The GaN market promises an imminent growth, 2015 and 2016 have been undoubtedly exciting years for the GaN power business. An explosion of the market with 84 percent CAGR between 2017 and 2022 is expected.

The market value will so reach $ 450 million at the end of the period", expects Ana Villamor, Technology & Market Analyst at Yole Développement. What make the power GaN technology so promising? Things are going on the right way - the power GaN supply chain prepares for production and 2017 has been showing significant investments that confirm the added-value of power GaN technology and its strong potential in numerous applications. In 2016 the power GaN market reached $ 12 million - it is still a small market compared to the impressive $ 30 billion Silicon power semiconductor market. However its expected growth in the short term is showing the enormous potential of the power GaN technology based on its suitability for high performance and high frequency solutions.

New applications enabled

"LiDAR, wireless power and envelope tracking are high-end low/medium voltage applications, and GaN is the only existing technology able to meet their requirements," explains Villamor. Beginning of the year, Velodyne Lidar opened a 'megafactory' to ramp up the latest 3D sensor for LiDAR manufacturing and this October they already announced a fourfold production increase." Other major companies, like Apple and Starbucks, started offering wireless charging solutions. Moreover, since 2016, EPC has been working with Taiwan's JJPlus Corporation to accelerate the wireless charging market's growth.

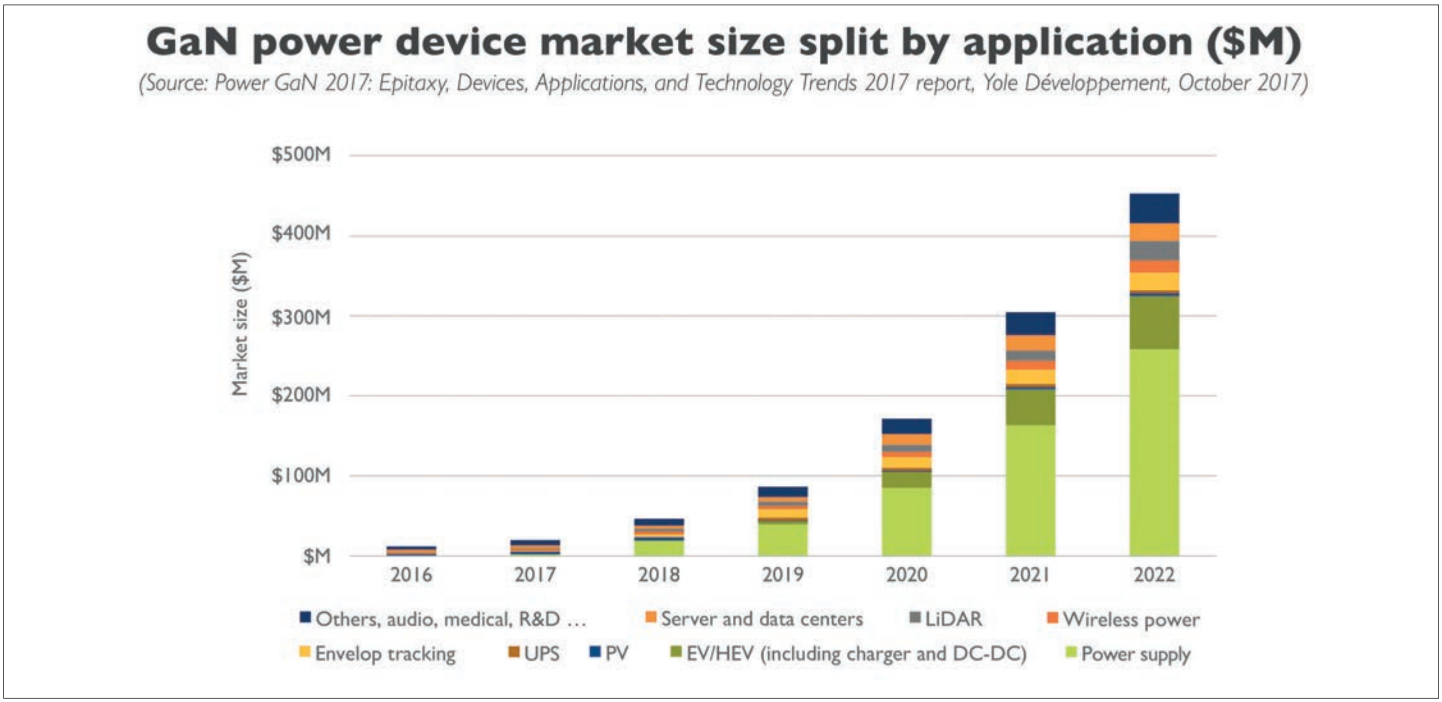
The power supply segment is still the biggest application for GaN. The data center market is adopting GaN solutions with a phenomenal speed, driving a plus 110 percent CAGR for power supplies through to 2022. Existing solutions from Texas Instruments and EPC for data centers, 0consisting of a DC/DC converter and point of load supply that steps down the voltage from 48 V to 1.2 V in a single chip, will propel the market. AC/DC power adapters for laptops or smartphones can be also implemented with GaN power IC solutions, which further reduces the size and cost of the system.

Therefore the consumer market is expected to grow during coming years and Yole's analysts envisage two different scenarios, depending on the acceptance in key markets like AC/DC adapters for laptops and cellphones.

GaN needs to hurry to gain adoption in the EV/HEV market because SiC MOSFETs are already replacing Silicon IGBTs in the main inverters. However, a future market for the 48 V battery's DC/DC converter is still possible for GaN due to its high-speed switching capability. Some main players, as Transphorm, have already obtained qualification for automotive, and this would help to finally ramp-up GaN production for EV/HEV. In parallel, the GaN power devices supply chain is acting to support market growth. Therefore it is close to being settle for the power GaN market and deals during 2017 show confidence that GaN will be a successful market.

Increasing manufacturing capacity

"First of all, there have been big investments from the main foundries to



increase their capacity to handle mass production", asserts Zhen Zong, Technology & Market Analyst at Yole Développement. "Navitas just announced the partnership with TSMC and Amkor ramp production capacity. Moreover, BMW i Ventures has just invested in GaN Systems. The Taiwan's Ministry of Economic Affairs is also interested in using GaN for clean and green technologies, also in collaboration with GaN Systems. GaN manufacturers clearly continue developing new products and provide samples to customers, as is the case with EPC and its wireless charging line. For example Panasonic announced the mass production of its 650 V products and Exagan successfully produced its first high voltage devices on 8-inch wafers. Other players are in the final phase of R&D or qualification for their GaN products to be launched in 2018."

www.yole.fr

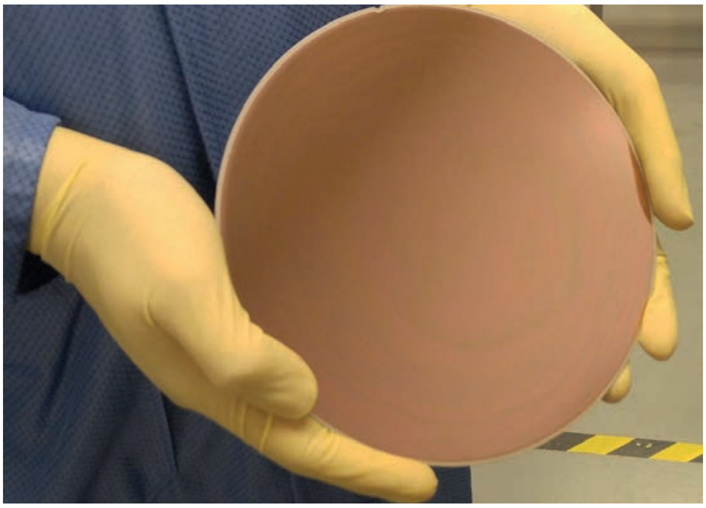
200-Millimeter Diameter GaN on QST Wafers

Kyma Technologies, Inc., a developer of wide bandgap semiconductor materials technologies, announced a hydride vapor phase epitaxy (HVPE) growth tool to produce high quality 200-mm diameter HVPE GaN on QST® (QROMIS Substrate Technology) wafers.

The announcement of Kyma's development of 200-mm diameter GaN wafers follows its announcement in 2016 of its demonstration of 150-mm diameter GaN on QST in partnership with QROMIS, Inc. (formerly Quora Technology, Inc.) and its recent announcement of the commissioning of Kyma's K200™ HVPE growth tool. The demonstrated HVPE GaN on QST consists of 10 microns of HVPE GaN grown on a 5 micron MOCVD GaN on QST wafer provided by QROMIS. X-ray diffraction rocking curve linewidths for the templates fall in the range of 250 and 330 arc-sec for the symmetric {002} and asymmetric {102} XRD peaks, respectively, which is consistent with high structural quality. Low wafer bow (~50 microns) and smooth surface morphology suggest these materials should support high performance device manufacturing.

"We have successfully transferred the process for making high quality GaN to our HVPE tool. The structural quality of the GaN produced on QROMIS' QST substrate is excellent. We are currently engaging with customers interested in large diameter GaN on QST templates", commented CEO Keith Evans. Its foundry partner Vanguard International Semiconductor (VIS) is planning to offer GaN power device manufacturing services on 8-inch diameter QST platform in 2018. "Our CMOS fab-friendly 200-mm diameter QST substrates and GaN-on-QST wafers represent a disruptive technology, enabling GaN epitaxy from a few microns to hundreds of microns for GaN power applications ranging from 100 V to 1,500 V or beyond in lateral, quasi vertical or vertical device forms, and device manufacturing on the same 8-inch or 12-inch diameter platform at Si power device cost. Kyma's HVPE technology represent an important value-add to QST-based GaN power device manufacturing by enabling the low cost deposition of a thicker and lower defect density GaN surface than is practically achievable using MOCVD growth alone", added QROMIS co-founder & CEO Cem Basceri. Kyma also teamed with a semiconductor equipment OEM to manufacture HVPE tools for customers who prefer to bring this GaN process in-house.

www.kymatech.com, www.qromis.com



200-mm diameter HVPE GaN on QST® templates which consists of 10 microns of HVPE GaN grown on a 5 micron MOCVD GaN on QST® wafer Source: Kyma Technologies

Stronger Position In Power Semiconductors

Infineon reported for fiscal year 2017 a revenue growth by 9 percent to Euro 7.63 billion. All four business segments contributed to this growth – in particular Automotive, Industrial Power Control, and Power Management & Multimarket.

"Infineon is the clear number one in the global MOSFET market, also in modules up to 900 volts. Apart from leading transistor technologies, our broad portfolio also includes the relevant drivers and controllers. Our CoolMOS family for higher and high voltages in the range from 400 to 900 volts is mainly used in power supply units of servers and notebooks. While the market for notebooks is hardly growing any more, we see great potential at data centers as a result of big data and applications in the field of artificial intelligence. Silicon Carbide has now achieved the breakthrough as a basic technology for power transistors. In fiscal year 2017, we generated revenue from our Silicon Carbide MOSFET for the first time. We are continuing on this path and expanding our portfolio step by step. We are also working on qualifying it for use in electric vehicles. Onboard chargers and main converters will become more compact, lighter and more efficient thanks to Silicon carbide. That means a car can run the same distance on a battery that is reduced in size – an extremely important factor for the success of electromobility. The growing prevalence of e-vehicles also necessitates a recharging infrastructure for them. Infineon supplies SiC power modules for ultra-fast recharging and is involved in important projects in China and Europe. We have also made major progress with Gallium Nitride. We launched the first products

from our CoolGaN family and generated revenue from them in the past fiscal year. When switching to compound semiconductors, our customers typically have to adapt their system architecture. We help them do that", CEO Reinhard Ploss pointed out by presenting the fiscal year 2017 results.

Infineon raised the outlook for the full fiscal year in March 2017 and achieved the higher targets, despite stronger headwinds caused by the weaker US dollar. „Our growth is very broadly based.

Alongside electro-mobility, driver assistance systems and renewable energy, a further pillar of growth is our industrial business – including drives for increasingly automated production machinery and robotics. Demand is also strong for our highly efficient chips, by example for fast chargers for tablets. With future technologies such as Silicon Carbide and Gallium Nitride, we are paving the way for tomorrow's success. Adjusted for exchange rate effects, our growth rate in the 2018 fiscal year could even reach the double-digit mark", Ploss expects. For the 2018 fiscal year, based on an assumed exchange rate of US dollar 1.15 to the Euro, Infineon expects year-on-year revenue growth of about 9 %. The automotive segment is predicted to grow at a meaningfully faster rate than the Group average.

www.infineon.com

"With future technologies such as Silicon Carbide and Gallium Nitride, we are paving the way for tomorrow's success", Infineons CEO Reinhard Ploss stated

Taiwan Supports GaN

GaN Systems and Taiwan's Ministry of Economic Affairs (MOEA) have signed in October a Letter of Intent to collaborate on expanding the economic and technical benefits of GaN technology to Taiwan's electronics companies. To further advance Taiwan's leadership role in the electronics industry, recognizing the importance and benefits of GaN, the MOEA will provide assistance to GaN Systems to extend its in-country business and representation. Working together, this alliance will collaborate to help solve some of the world's most daunting power challenges.

Ms. Mei-Hua Wang, Vice Minister of MOEA, commented on the development, "As Taiwan plays a preeminent role in the Asian electronics industry, we are pleased to provide GaN Systems with the resources to continue their success with our leading manufacturers. This Letter of Intent strengthens the bonds between GaN Systems and Taiwan's electronics industry." "We are delighted to join forces with Taiwan's MOEA. We see this as an important demonstration of how companies and government work together to reinforce partnerships amongst industry leaders and across industry segments, " added GaN Systems' CEO Jim Witham.

www.gansystems.com

Productronica SEMICON Europa 2017 Co-Location

SEMICON Europa 2017 took place in Munich from 14 to 17 November, co-located with the manufacturing-oriented fair Productronica. More than 400 exhibitors presented their products and services at SEMICON Europa 2017 to over 40,000 attendees at the co-located events.

The market for semiconductor production facilities is even more positive. SEMI Industry Association expects a worldwide growth of 19.8 percent with a volume of $49.4 billion for this year. China with more than sixty percent and Europe with over fifty percent recorded the biggest increases here. Among other things, the increased need for equipment is being created by high innovation pressure in the industry and growingly diversified customer needs. In addition, the entire semiconductor industry is going through deep-rooted changes. After approx. five decades, 'Moore's law', according to which twice as many transistors are packed on a microprocessor every two years, is gradually losing its validity. Physics no longer cooperates, the semiconductor fabrication plant (fabs) for the next chip generations are too expensive, and it no longer makes sense for an increasing number of chips to follow Moore's Law. For example, the focus in mobile devices is away from pure computing power to connectivity and power management.

One sign of the change is the consolidation of the industry. One billion deal after another has been concluded in the past few years. As a result, semiconductor manufacturers reduce costs and increase profitability, but also expand their product portfolios. Companies that previously mainly targeted the now saturated PC and smartphone market increasingly need to be active in growth segments such as the Internet of Things (IoT), industrial applications, automotive and data storage. Additionally, they need to do this in increasingly shorter cycles.

After a period of slow growth, Europe's semiconductor manufacturers are investing in new construction of 300 mm fabs in Germany, Italy and France. Four semiconductor and MEMS manufacturers have announced investments in Europe totaling more than $10 billion. Bosch will build a new fab in Dresden; ST Microelectronics is planning two new 300 mm fabs in Agrate and Crolles; and Infineon plan to expand their 300 mm production capacity for power semiconductors in Dresden. "The global industry will invest more than $100 billion in equipment and materials this year. Forecasts for 2017 also predict that semiconductor manufacturers worldwide will exceed $400 billion in revenue – a new record," says Ajit Manocha, president and CEO of SEMI. "An unprecedented number of new inflections and applications will broadly expand the digital economy and drive increasing silicon content — in areas including IoT, assisted driving in automotive, artificial intelligence, big data, and 5G. Assuming an average 7 percent CAGR, global chip sales could approach $1 trillion by 2030, and equipment and materials spending could similarly grow to nearly a quarter of a trillion dollars."

The market segments in which European companies hold strong market positions also shaped the conference program of SEMICON Europa 2017. More than 250 presentations, 50 conferences and additional discussions provided an overview of current trends. Key issues included materials, semiconductor manufacturing, advanced packaging, MEMS/sensors, flexible & printed electronics and power electronics.

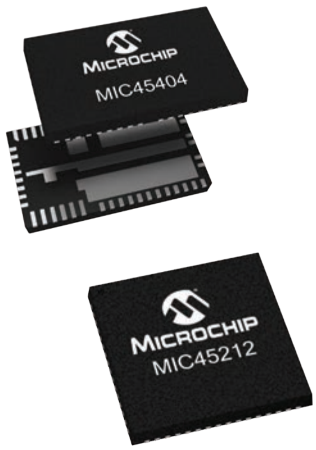
A power electronics keynote given by Prof. Florin Udrea from Cambridge University (UK) pointed out that Silicon still has a bright future, though SiC, GaN and even Diamond are in discussion. "The SJ FOM can be improved heavily by reducing the cell pitch. Thus the SJ MOSFET as well as the IGBT will survive in the future. Temperature is the only critical parameter where SiC and GaN have an advantage". He expects that GaN on Si is limited to 1200 V and maximum 200 A due to its lateral structure. SiC has the advantage of zero recovery losses for diodes and thus will be favoured also for lower-voltage diodes. GaN has no zero recovery. Diamond is in an initial stage for diodes on 2-inch wafers but more than 20 years away from adoption.

www.productronica.com, www.semiconeuropa.org

KNOWLEDGE IS POWER

Massive power density in the smallest packages

Microchip Technology now offers an integrated switching power module designed specifically for height-constrained telecom, industrial and solid-state drive (SSD) applications. These products come in an impressive thermally-enhanced package that incorporates inductors and passive components into a single, molded power converter. The slim packages simplifies board design, saves space and eliminates concern over passive components that may introduce unexpected electromagnetic interference (EMI).



Highlights

- Variety of module package offerings (small to large, fit to application)
- High power density with integrated magnetic and passive components
- Performance (efficiency, thermal, transient response)
- Reliable (power and thermal stress tested)
- Low EMI (CISPR 22 Class B ratings on modules)

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Nanocomposite Electrolyte for Next-Generation Batteries

Imec, the Belgium research company, and Panasonic announced that they have developed an innovative solid nanocomposite electrolyte for next-generation batteries with a lithium ion conductivity several times greater than its liquid equivalent. The ion conductivity already reaches several mS/cm at room temperature. Imec and Panasonic have set a goal to develop novel solid nanocomposite electrolyte materials towards 100mS/cm in the next few years, which would make them suitable for fast-charging high-energy cells for use in vehicles and electronics.

Li-ion batteries are the predominant type of storage in the portable electronics and electrical vehicle markets. They are also poised to take an important role in the future energy grid, where they have the capacity to store energy from sustainable energy sources. However, Li-ion batteries still require considerable innovation in order to achieve ultra-fast-charging high-energy cells. Imec's and Panasonic's SCE is a mesoporous silica monolith functionalized with specific surface chemistry and ionic salts. It has achieved Li-ion conductivities of 3 to 10 mS/cm at room temperature which is exceptionally high for solid electrolytes that are applied via wet chemical coating. Moreover, using our new electrolyte technology, we have demonstrated rechargeable solid-state Li-ion batteries with lithium titanate ($Li_4Ti_5O_{12}$) as negative electrode and lithium iron phosphate ($LiFePO_4$) as positive electrode. "The wet chemical preparation route allows the solid-state electrolyte to be casted into powder electrodes, where it solidifies while remaining mechanically pliable. This paves the way to batteries in flexible form factors," stated Philippe Vereecken, principal member of technical staff and program manager at Imec at the 58th Battery Conference in Fukuoka.

www.imec-int.com

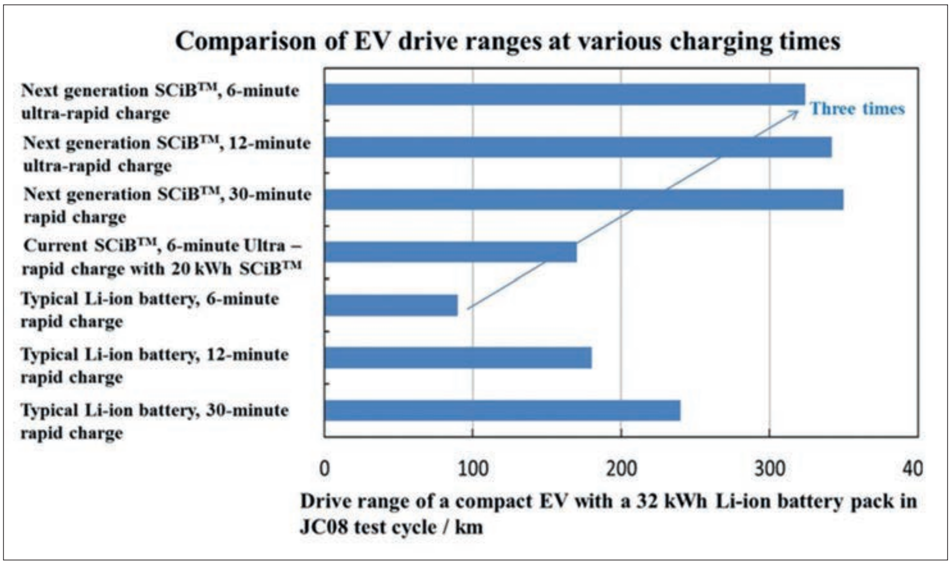
Next-Generation Lithium-ion Battery Featuring New Anode Material

Toshiba announced the development of its next-generation SCiB, which uses a new material to double the capacity of the battery anode. The new battery offers high- energy density and the ultra-rapid recharging required for automotive applications, and will give a compact electric vehicle (EV) with a drive range of 320 km after only six minutes of ultra-rapid recharging—three times the distance possible with current lithium-ion batteries.

Toshiba launched the SCiBTM as a safe, long-life, fast charging lithium-ion battery in 2008. Since then, the company has constantly refined the technology and improved real-world performance by developing a titanium niobium oxide anode material that has double the lithium storage capacity by volume of the graphite-based anodes generally used in lithium-ion batteries. The new battery also offers high energy density and ultra-rapid recharging characteristics, and its titanium niobium oxide anode is much less likely to experience lithium metal deposition during ultra-rapid recharging or recharging in cold conditions—a cause of battery degradation and internal short circuiting. "Rather than an incremental improvement, this is a game changing advance that will make a significant difference to the range and performance of EV. We will continue to improve the battery's performance and aim to put the next-generation SCiB into practical application in fiscal year 2019," stated Dr. Osamu Hori, Director of Toshiba's Corporate Research & Development Center.

Rigorous testing of a 50 Ah prototype of the new battery has confirmed that it retains the long life cycle, low-temperature operation, excellent safety and rapid recharging characteristics of the current SCiB. The energy density by volume of battery is twice that of the current SCiB. The next-generation SCiB maintains over 90 % of its initial capacity after being put through 5,000 charge/discharge cycles, and ultra-rapid recharging can be done in cold conditions, with temperatures as low as minus 10°C, in only ten minutes.

http://www.scib.jp/en/product/



EV Powertrain Optimization

Prof. Omar Hegazy, head of power electronics and electrical machines at the MOBI Research Centre, University of Brussels (VUB), recently highlighted his team's EV powertrain optimisation techniques. MOBI employs a multidisciplinary team of over 90 specialists who address the challenges that the transport value chain faces, by integrating engineering, economic, social and environmental sciences and policy issues.

MOBI possesses state-of-the-art infrastructure and models for the testing, development and design of components (i.e. batteries, supercapacitors, power converters etc.), vehicle powertrains, and inductive and conductive charging infrastructure. Simulation techniques have been developed to define energy-efficient and low-emission power control strategies in hybrid propulsion systems. There is also a team working on big data and analytics.

"The three largest barriers that we currently have in the electric transportation industry are a high purchase cost, a short driving range and a limited charging infrastructure," said Hegazy. "The solutions to the first two points can be found in the powertrains of the machines themselves. My team is focused on the optimization of powertrain sizing components and control system design, known collectively as co-design. We start by looking at the available space in EV or HEV powertrains; we then evaluate which components would work best before trying to find innovative ways to incorporate them – the perfect symbiosis of technology and topology. There are many things to consider, such as battery technology, energy consumption, battery pack voltage, charging power and charging time, but we use our 40 years' experience in electric, hybrid, fuel cell vehicles and stationary applications R&D to produce successful results."

Contract research examples include

- STIB-MIVB: Design of electrified buses and multi-criteria analysis of technological solutions aiming at recovering metro braking energy.
- JSR Micro: Testing, modelling and optimisation of Li-ion capacitors.
- Umicore: Characterisation and modelling of advanced Li-ion battery.
- Electrabel: Analysis of the unbalance between different renewable energy supplies. Comparison of various storage technologies together with assessment of the economical and the environmental impacts.
- Powerdale (PWD): Technical support on charging solutions and standardisations.
- Bluways International: Technical advice on supercapacitors and energy management. Testing and data analysis.

MOBI offers a life cycle assessment (LCA) methodology for the entire automotive sector to analyze the environmental, economical and societal impacts caused by the development and implementation of new vehicle technologies, components, materials and policy measures. "Using a large database with real-life measurements, we're able to provide accurate technical, economical and environmental assessments. The database is kept up-to-date with the latest information obtained during research projects and the execution of contracts. Methods and models are developed and then translated into practical tools that are tailor made primarily for the transport sector, but also for the energy sector. From a technological perspective, the center has a leading position in electromobility. Our international partners value the expertise that MOBI offers," Prof. Hegazy stated. Over the last five years, the centre has undertaken 23 major European projects, 51 direct contracts with the industry, and 76 projects funded by national organisations.

http://mobi.vub.ac.be/home/

"MOBI is focused on the optimization of powertrain sizing components and control system design and has undertaken many major European projects", said Prof. Omar Hegazy, head of power electronics and electrical machines at VUB

Semikron Sponsors Innovation Award

The SEMIKRON Innovation Award and the SEMIKRON Young Engineer Award is given for outstanding innovations in projects, prototypes, services or novel concepts in the field of power electronics in Europe, combined with notable societal benefits in form of supporting environmental protection and sustainability by improving energy efficiency and conservation of resources.

Both prizes have been initiated and are donated by the SEMIKRON Foundation which is awarding the prizes in cooperation with the European ECPE Network.

The Prizes will be awarded in the frame of the ECPE Annual Event in March 2018 in Stuttgart - a single person or a team of researchers can be awarded. The award targets at projects, prototypes, services and novel concepts developed in Europe, which did not yet appear on the market, which are used in a novel application, or which form an absolute novelty, and therewith fulfil the requirement to be extraordinary and remarkable. Sole project proposals are not in the scope of the call, the innovation should have been verified by experiment or simulation. The degree of innovation has to conform to international standards.

Proposals comprising 3 – 5 pages with the reference 'SEMIKRON Innovation Award' should be sent by email to Thomas Harder, General Manager of ECPE e.V., thomas.harder@ecpe.org. Deadline is January 15, 2018.

Radiation Hardened POL Sequencer

Intersil announced in November the ISL70321SEH and ISL73321SEH quad power supply sequencers designed to drive point-of load (POL) regulators that power high performance FPGAs and complex, multi-rail power systems. This radiation-hardened power supply sequencers ensure high reliability operation with fault monitoring to boost system health and performance, and they are the industry's first space-grade sequencers backed by single event effects (SEE) mitigation tests and complete radiation assurance testing.

Space radiation effects on electronic devices are an important system design consideration. They can cause problems ranging from operational malfunctions to severe physical damage to the devices. Total ionizing dose and single event effects are two most common effects that cause damage to an integrated circuit. TID effects are the result of accumulated exposure to ionizing radiation. SEE are the result of a single high energy particle that strikes the device. SEE can cause a transient on the output of a circuit, known as a single event transient (SET). However, they can also be destructive causing single event burnout (SEB) or single event latch-up (SEL).

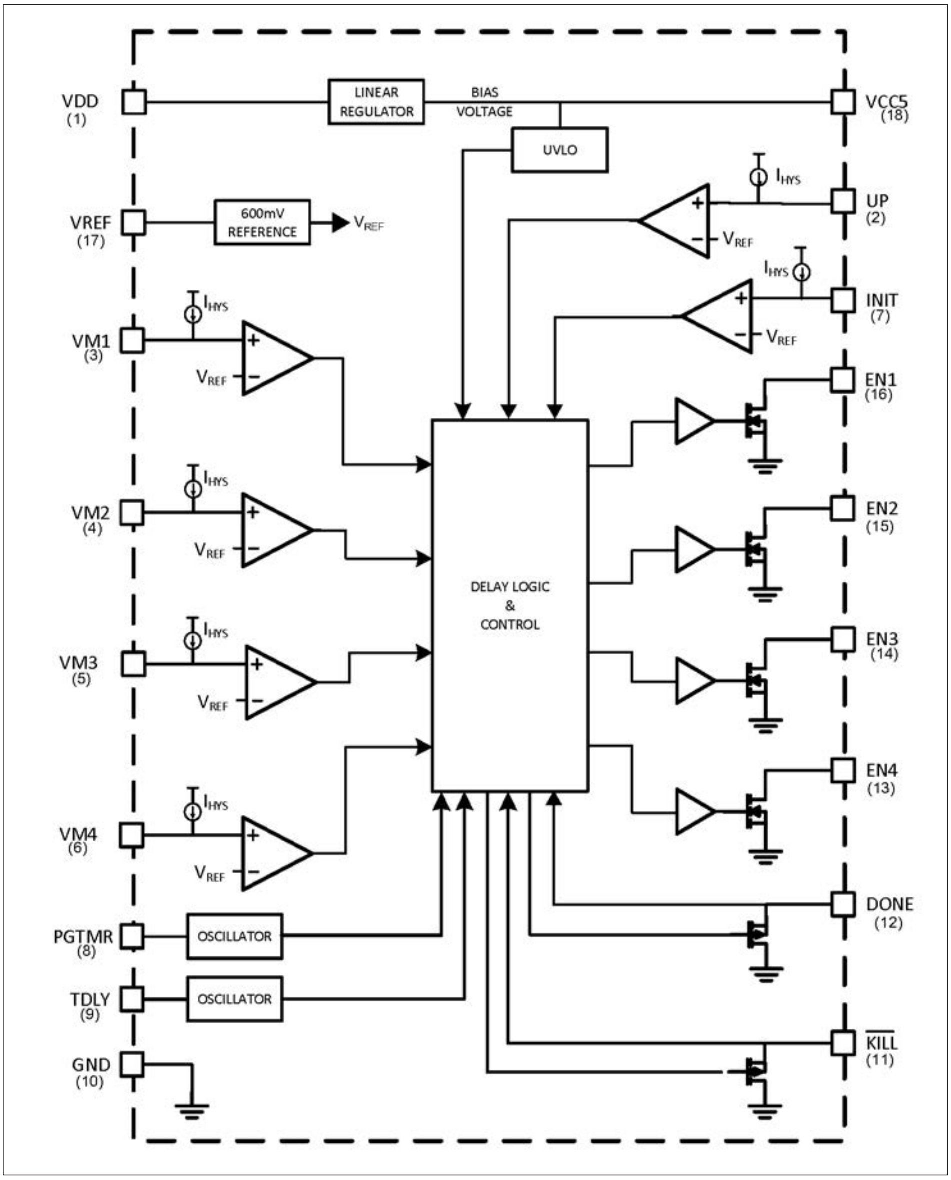
The ISL70321SEH sequencer is radiation assurance tested to 100 krad(Si) at high dose rate and 75 krad(Si) at low dose rate, while the ISL73321SEH is assurance tested to 75 krad(Si) at low dose rate. Both sequencers provide an accurate and scalable method to achieve the proper power-up and power-down sequencing of DC/DC converters essential to powering FPGAs, DSPs, RF communications ICs, and high density distributed power systems. They simplify design by using minimal external components, only requiring two resistors per power supply for voltage monitoring, and a single resistor to program the rising and falling delay. Up to four power supplies can be fully sequenced by a single device or multiple devices can be cascaded to sequence an numerous power supplies.

The highly integrated sequencers reduce bill of materials cost by replacing discrete solutions that employ several comparators, resistors, and capacitors. To ensure accurate monitoring and reliable system operation, the ISL70321SEH and ISL73321SEH integrate precision input comparators with an input threshold voltage of 600 mV ±1.5 %. Both devices actively monitor seven different fault conditions to provide comprehensive fault detection, and a DONE indicator gives system feedback that power-up and power-down have completed successfully.

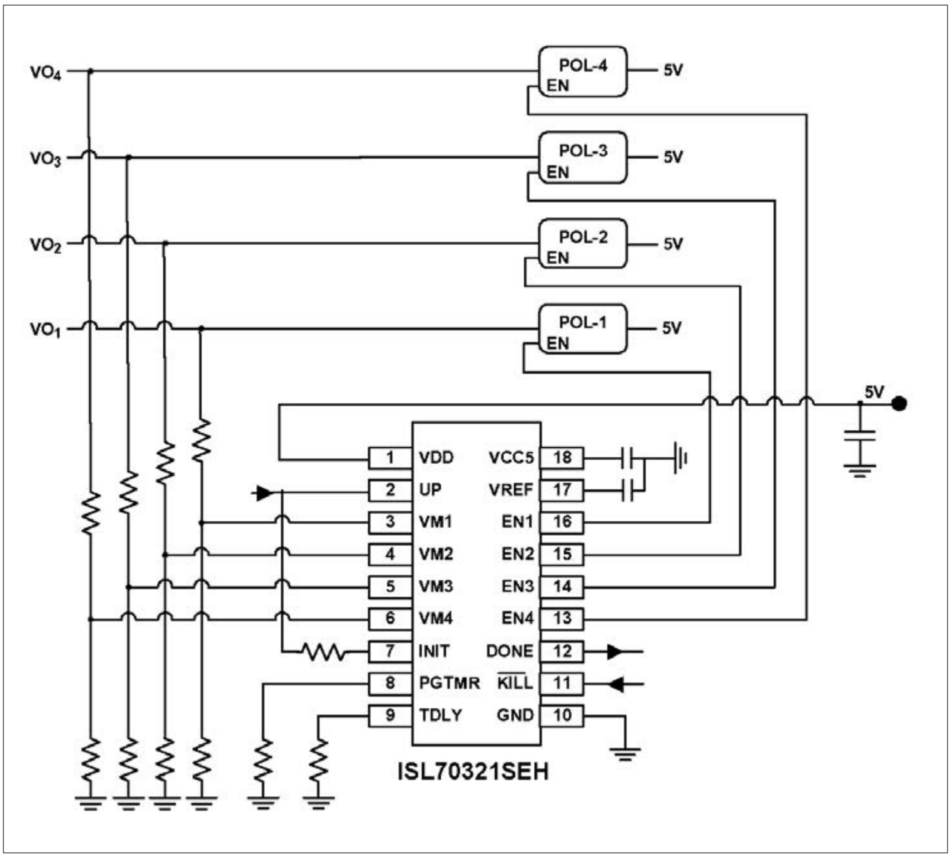
Typical application

The ISL70321SEH and ISL73321SEH are SEE mitigated sequencer circuits designed to drive multiple POL regulators with active high enable

POL sequenzer for space applications



ISL70321SEH functional block diagram



ISL70321SEH typical application schematic

inputs. Up to four individual sequenced events can be controlled by a single device or by cascading multiple devices increase to an unlimited number of sequenced events.

This power supply sequencer requires only two feedback resistors for output voltage sensing per sequenced power supply; a single resistor to set the rising and falling delay between sequenced supplies, and an additional single resistor for setting the power-good timer of each sequenced supply. This device features input comparators with an input offset voltage ≤3 mV and ±1 % threshold voltage reference to achieve precision voltage monitoring.

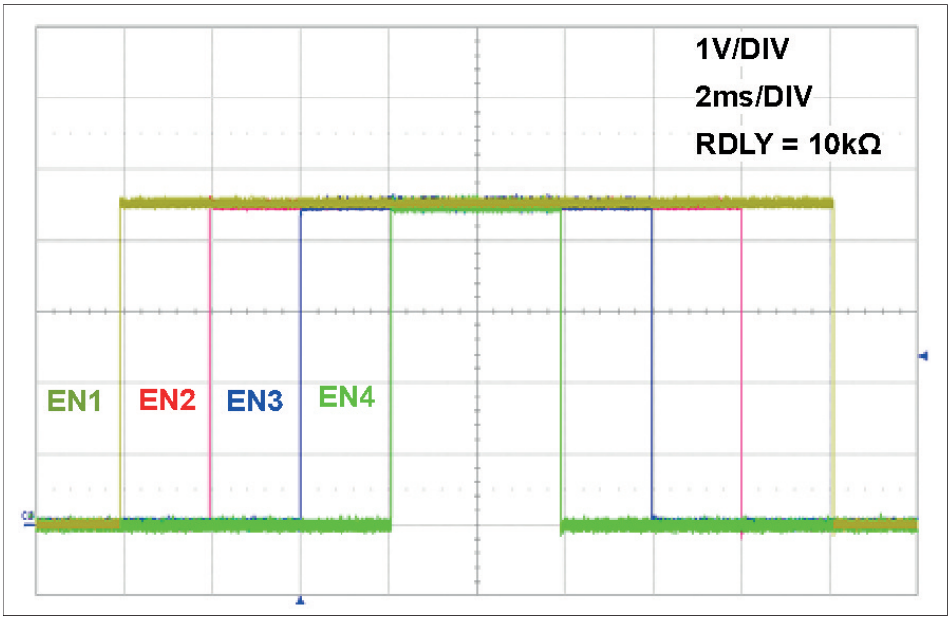
After an adequate V_{DD} bias voltage is applied, and with both the UP and INIT inputs high, the device will initiate the first event in the sequence by releasing EN1 to be pulled high through an external pull-up resistance. The output of the connected POL is then monitored for an adjustable threshold level by VM1 and when deemed 'good' within the power-good timer period, EN2 is released to be pulled high. This process is repeated until EN4 is released and the DONE output is finally released, signifying the sequence up is complete. The DONE output remains high and is pulled to GND after sequence down is completed.

The UP pin commands the IC to sequence up or down the power supplies using the ENx outputs. The UP detection circuitry is identical to the VMx pins and can be driven by a system controller to determine whether the sequence is up or down.

The INIT pin is the initiator of either an up or down sequence event chain. The INIT detection circuitry is identical to the VMx pins and can be driven by a system controller to initiate the up or down sequence activity. To sequence down, the UP and INIT are pulled low and during sequence down, the device deasserts the EN4 to EN1 outputs in that order (reverse from sequence up) after the voltages on pin VM4 to VM1 fall below their programmed thresholds.

The rising and falling delay, t_{DLY} , can be programmed in the range of 2 ms to 20 ms using a single resistor (10 kΩ to 100 kΩ) from TDLY to GND. The rising delay is from VMX crossing its threshold to ENX+1 being released. There is also a delay from UP crossing its threshold and EN1 being released. During power-down, falling delay is from VMN falling below the threshold to ENN-1 being asserted low. There is also a delay from UP falling below the threshold and EN4 asserted low.

A PGOOD timer, tPGTMR, in the range of 4 ms to 40 ms can be programmed using a resistor (10 kΩ to 100 kΩ) from PGTMR to GND. This is the amount of time from turn-on that a power rail has to cross the threshold. The PGOOD timer is active only during power-up sequencing and starts counting after each ENx pin is released to go high.



Four events up and down sequence

Methods for implementing sequencing

Sequencing and monitoring all power supplies can be accomplished several ways. However, these implementations may not be suitable for spacecraft operating in the harsh deep space environment, or for satellites in earth orbit.

The most basic way to implement sequencing is to utilize the power good (PG) and enable (EN) pins of the POL or LDO regulator. The PG pin of converter "n" will be connected to the EN pin of converter "n+1". This cascading configuration is repeated for all the rails in the system. To add a delay between the PG signal asserting and the startup of the next regulator in the sequence, a capacitor is added to the EN pin of the next regulator. This is by far the simplest method and it is essentially cost free; however, it does have major drawbacks, eg it does not support power-down sequencing in the reverse order or include the variation of the PG assertion level and the PG delay versus temperature.

A discrete solution implementation using

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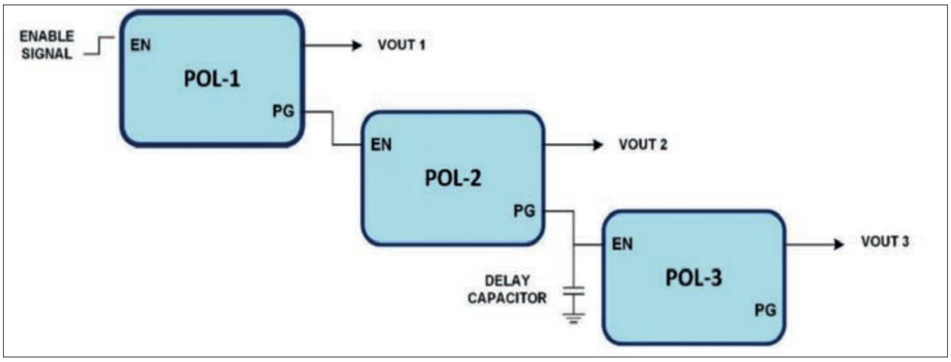
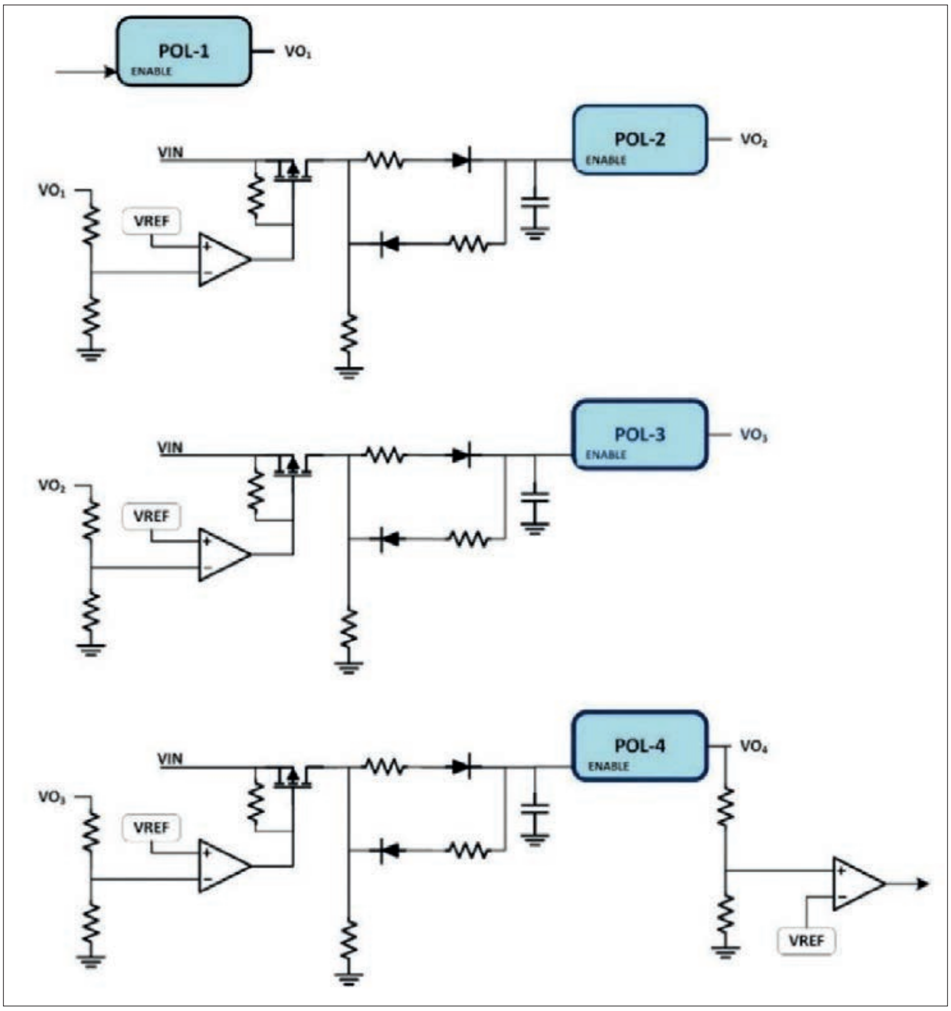
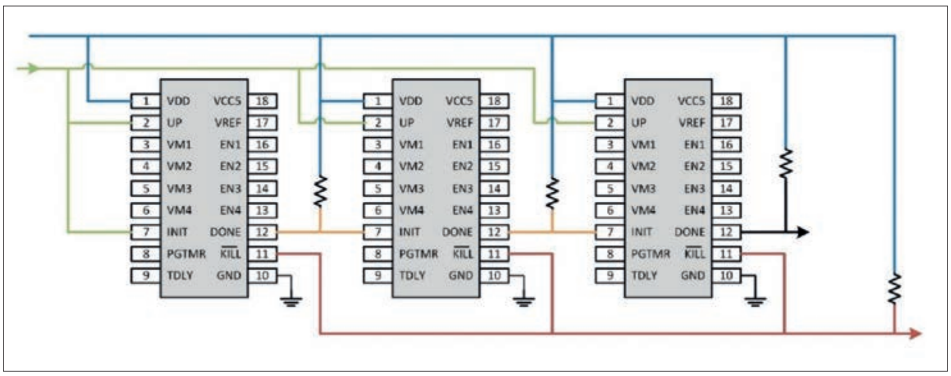


PGOOD to ENABLE sequencing



Discrete solution implements sequencing with delays



Sequencing 12 voltage rails

comparators, resistors and capacitors can provide power-up sequencing, but this method still does not allow power down in the reverse order. The added complexity does include the benefits of precision voltage monitoring and the ability to delay both the power up and power down. However, the discrete design increases the solution size and the bill of materials cost.

The two previous methods have one common flaw, the inability to power down in the reverse order, which may be needed to ensure system reliability. For example, high-end FPGAs require that the rails for the core, auxiliary and I/O voltages power down in reverse order to avoid excessive current draw and possibly damage the digital load.

To meet the power-up and power-down requirements, the ISL70321SEH radiation-hardened quad power supply sequencer may be used. The benefits of using an analog power sequencer are effortless design with minimal external components, and accurate fault monitoring to ensure reliable system operation. A resistor divider connected from the power supplies to the corresponding voltage monitor (VM) pin is all that is needed to monitor each rail, this divider also sets the turn-on and turn-off voltage of the next sequenced device. The simple open drain EN outputs make it easy to drive voltage regulators with different enable thresholds. Programmable rising and falling

delays are easily achieved by use of a single external resistor. This delay can be programmed between 2 ms to 20 ms. A power good timer is also included to detect if a rail does not come up within a programmed window of time from 4 msto 40 ms.

For more complex multi-rail power systems, such as those in RF applications where the number of rails can easily exceed more than a dozen, the ISL70321SEH can be cascaded to sequence virtually an unlimited number of rails. Through the use of the UP, INIT and DONE pins, cascaded

devices communicate to achieve power-up and reverse power-down sequencing of all the rails.

Five Output Digital Voltage Regulator

Infineon Technologies launches the IRPS5401, a five output Point of Load (POL) digital voltage regulator for FPGAs, ASICs, and other multi-rail power systems. The IRPS5401has been developed as a fully integrated PMIC solution that replaces multiple regulators with a single device in a compact 7 mm x 7 mm 56 pin QFN package usable for current and future applications in high density ASIC and FPGA. Additional applications comprise CPU multi-rail systems, embedded computing systems, and communication and storage systems.

The IRPS5401 forms a key part of the UltraZed System on a Module (SOM) from Avnet. The compact package size combined with PMBus communication for real-time monitoring and control provides the optimized power management solution that the UltraZed requires. With two devices onto an UltraZed SOM gives ten rails that can be fully monitored and controlled with software, while maintaining a business card size footprint for the SOM.

The IRPS5401 is designed for single rail operation ranging from 5 V to 12 V, where most PMICs are only 5 V. It has one 500 mA LDO output, and four configurable switching regulator outputs, two at 2 A, and two at 4 A. The outputs can be used to provide the typical rails required for core, memory, and I/O voltages. The voltage output range is between 0.5 V and 3.6 V for regulators A to D, and between 0.25 V and 5.1 V for the LDO. Switching regulator A can output up to 50 A if combined with an external Power Stage. Switching regulators C and D can be combined to deliver 8 A in a low ripple, dual-phase configuration. All outputs are well within the power requirements of most FPGAs and ASICs ranging between 10 W to 50 W, including integrated voltage sequencing. Industry standard PMBus commands provide an easy-to-use interface for status and telemetry, and PMBus can be used to configure the output voltages in 5 mV steps.

The IRPS5401 switching regulators utilize fixed frequency Emulated current mode control, and thus no external compensation is required.

The IRPS5401 switchers provide precisely regulated output voltages programmable from 0.25 V to 2.55 V without a resistor divider and up to 5.1 V with a resistor divider. The device can operate with an internal bias supply (LDO), typically 5.0 V. This allows operation with a single supply by connecting the input of the LDO (VSUPPLY) to the bus voltage (Vin_x). A 1 µF capacitor should be used at the VSUPPLY pin for decoupling purposes. The output of this LDO is brought out at the Vcc pin and must be bypassed to the analog ground (pin 50) with a 1.0 µF decoupling capacitor. An additional voltage, VDRV, required by the internal driver circuitry is derived by using a 2 Ω / 1µF filter from the Vcc pin to the VDRV pin. The Vcc pin may also be connected to the VSUPPLY pin, and an external Vcc supply between 4.5 V and 5.5 V may be used, allowing for an extended operating bus voltage (Vin_x) range from 1.2 V to 14 V.

The device utilizes the on-resistance of the low-side MOSFET (synchronous MOSFET) as the current sense element. This method enhances the converter's efficiency and reduces cost by eliminating the need for external current sense resistors.

One-time programmable (OTP) memory

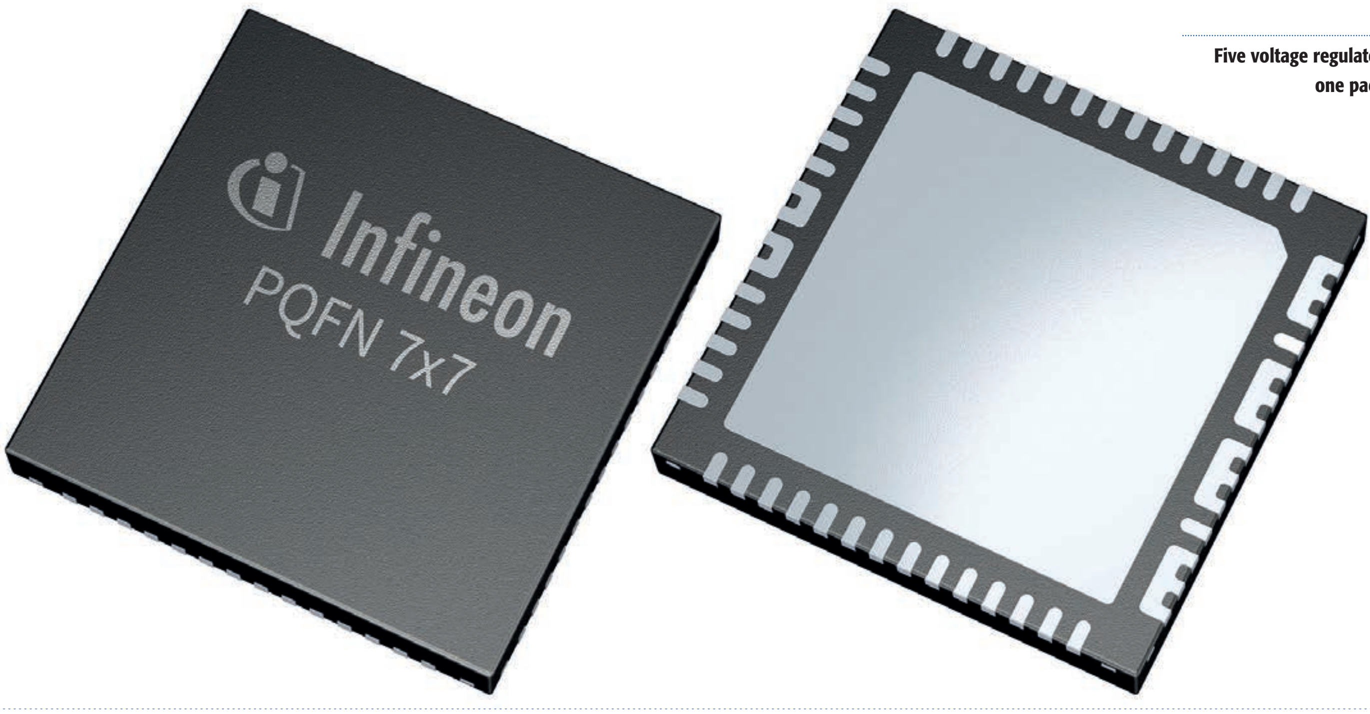
The IRPS5401 has 64K of OTP non-volatile memory based on a patented split-channel non-volatile anti-fuse memory cell.

The OTP memory has a data retention rating of ten years and an operating temperature range of -40°C to 150°C (-55°C to 150°C storage rating). This memory space is divided up into 20 OTP segments that can be programmed one time. The memory space is therefore referred to as Multiple-times Programmable (MTP). This allows the user to a) change the configuration registers and reprogram the MTP up to 20 times or b) save up to 15 configuration files during initial programing and use the MTP pin to choose which file to load at start up.

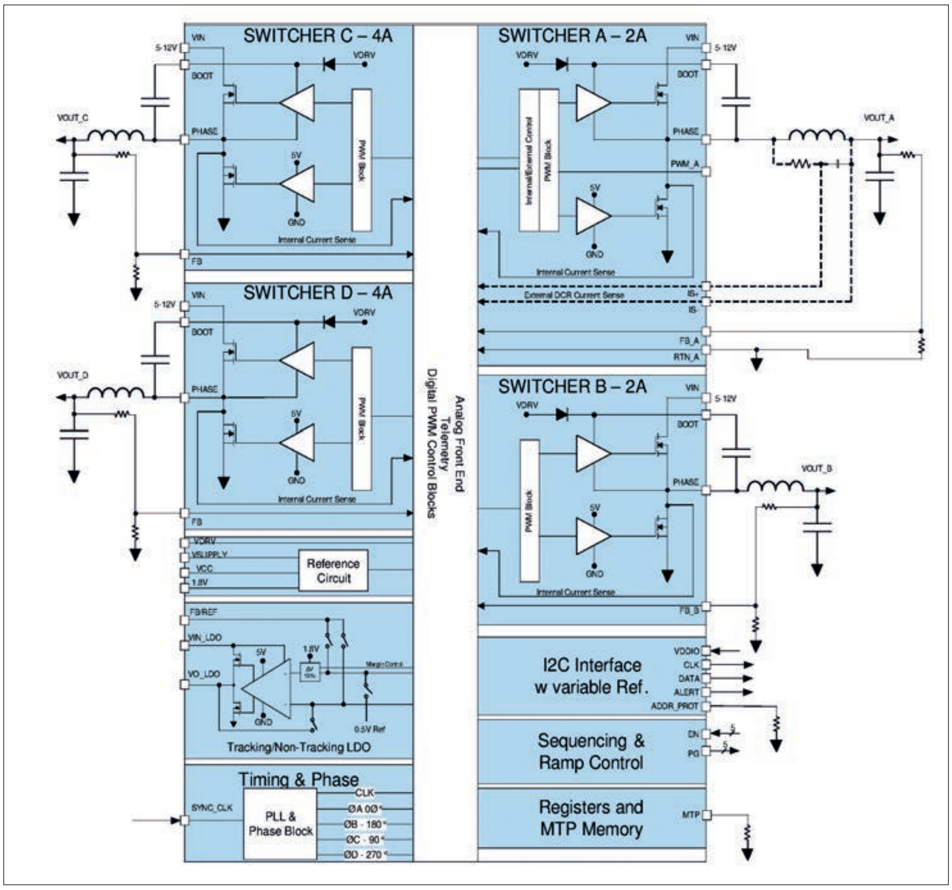
If option b is used, the remaining unused MTP segments are available for the user to make additional changes to the configuration file and save to MTP using the Rocky GUI device programmer utility.

Power-up and initialization

During the power-up sequence, when VIN is brought up, the internal LDO converts it to a regulated 5.0 V at VCC. There is another LDO which further converts this down to 1.8 V to supply the internal digital circuitry. An under-voltage lockout circuit monitors the voltage of the VCC pin and the P1V8 pin, and holds the POR low until these voltages exceed their thresholds and the internal 48 MHz oscillator is stable. When the



Five voltage regulators in one package



RIGHT: IRPS5401 block diagram

device comes out of reset, it initializes an MTP load cycle, where the contents of the MTP are loaded into the working registers. Once the registers are loaded from MTP, the designer can use I²C/PMBus to re-configure the registers to suit the specific VR design requirements if desired, irrespective of the status of the enable pins.

In the default configuration, power conversion for a given loop is enabled only when the corresponding En_x pin voltage is asserted high, the Vin_x bus voltage exceeds its under-voltage threshold (as stored in the MTP registers and commanded by the PMBus commands VIN_ON and VIN_OFF), the contents of the MTP have been fully loaded into the working registers and the device address has been read. IRPS5401 provides additional options to enable the device power conversion through software and these options may be configured to override the default by using the I²C interface or PMBus.

Switching frequency setting

The switching frequency (FSW) setting is stored in MTP and can be configured by using the PMBus command FREQUENCY_SWITCH. The IRPS5401 will ACK any FREQUENCY_SWITCH command from 200 kHz to 2 MHz in increments of 1 kHz (increments of 2 kHz with commands above 1 MHz).

Internally the command is decoded and the actual FSW is set to the nearest value that can be supported with a 48 MHz internal clock. For example, 500 kHz can be supported with ninety-six (96) 48 MHz clocks.

Telemetry and faults

The IRPS5401 provides true differential remote sensing for the Switcher A output. The FB_A and RTN_A pins are connected to the load sense pins of the Switcher A output voltage to provide true differential remote voltage sensing with high common-mode rejection. This allows Switcher A (in external power stage mode) to provide excellent regulation even in high current applications.

Switcher loops B, C and D have single ended feedback connections for sensing and regulation. Each loop has a high bandwidth error amplifier that generates the error voltage between this remote sense voltage and the target voltage.

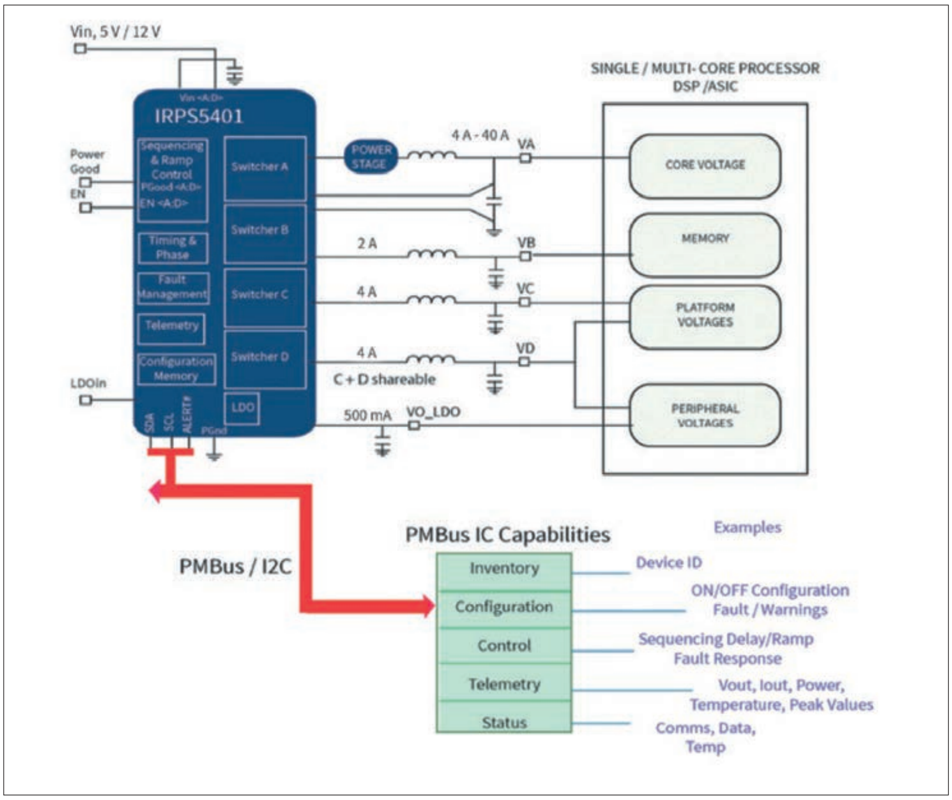
The error voltage is digitized by a fast, high-precision ADC. This digitized error is used for Vout under-voltage fault and warning detection as well as for Vout over-voltage fault warning detection. Vout is reported using the READ_VOUT PMBus command. The reported Vout is the DAC reference value and not the actual measure output voltage.

Linear regulator

The IRPS5401 also has a linear regulator (LDO) in addition to the four switchers. This regulator can accept a wide input voltage range from 1.2 V to 5.5 V and provide output voltages from 0.5 V to 3.3 V, delivering up to 0.5 A of continuous current with a low dropout voltage of 0.6 V.

Moreover, the regulator can be configured using an MTP register bit ldo_track_config. To operate in source-only mode, set ldo_track_config to 0. To operate in tracking mode, set ldo_track_config to 1. The tracking mode of operation makes it ideal for use in memory termination tracking applications. The LDO also supports a manufacturer specific PMBus command, MFR_LDO_MARGIN, to allow margining the output voltage ±15 %.

www.infineon.com/irps5401



RIGHT: IRPS5401 typical application schematic

Tackling Thermal Challenges In Power Semiconductor Applications

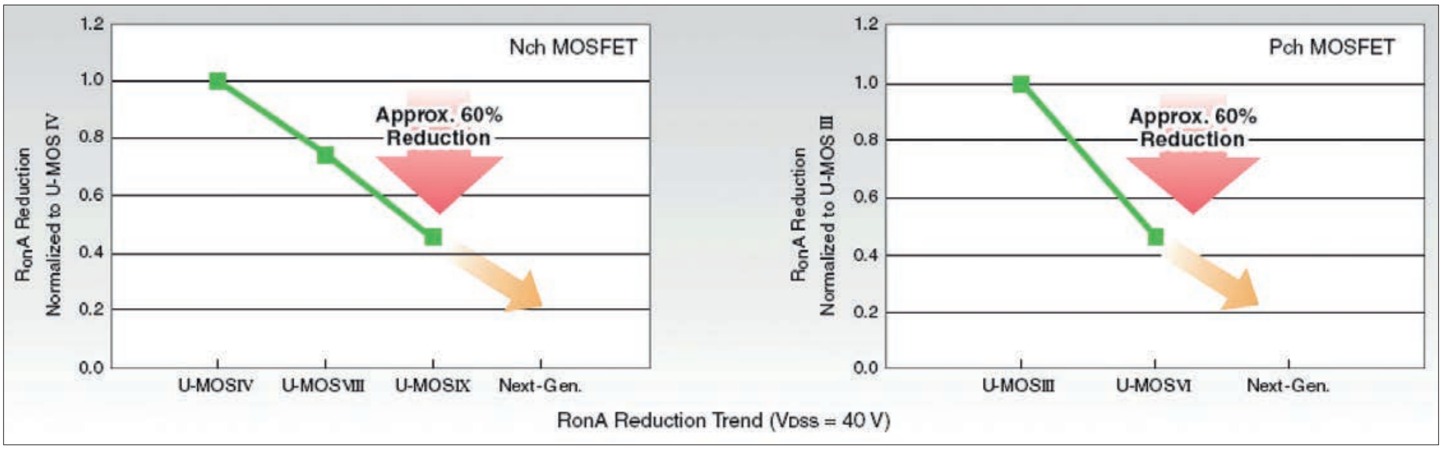
Heat is the enemy of electronic designers, and also of equipment end users. To designers, high chip temperatures are a threat to reliability and promote early failure. Cooling electronics with fans, heatpipes, or heatsinks introduces unwanted engineering challenges, and forces the design to be larger and heavier than is ideal. Moreover, if a fan is needed, this adds to the overall system power demand, introduces an extra potential point of failure, and prevents sealing the enclosure to prevent ingress of dust or moisture. The latest power semiconductors introduce improvements at the Silicon level, which improve power-conversion efficiency leading to reduced heat generation, while improvements in package design not only contribute to reducing heat generation but also enhance heat dissipation to allow increased power handling.

As far as the efficiency of power MOSFETs is concerned, reducing on-state resistance ($R_{DS(ON)}$) to improve conduction performance has traditionally been achieved at the expense of poorer switching characteristics. On the other hand, optimizing the device to reduce the gate charge (Q_g), which helps improve switching efficiency, tends to result in increased $R_{DS(ON)}$). The trade-off between these two parameters is expressed in the common figure of merit (FOM) applied to power MOSFETs: RDS(ON) x Q_g. The latest trench MOSFET technologies have overcome the traditional limitations on these two parameters, allowing lower conduction losses and better switching performance to be achieved at the same time.

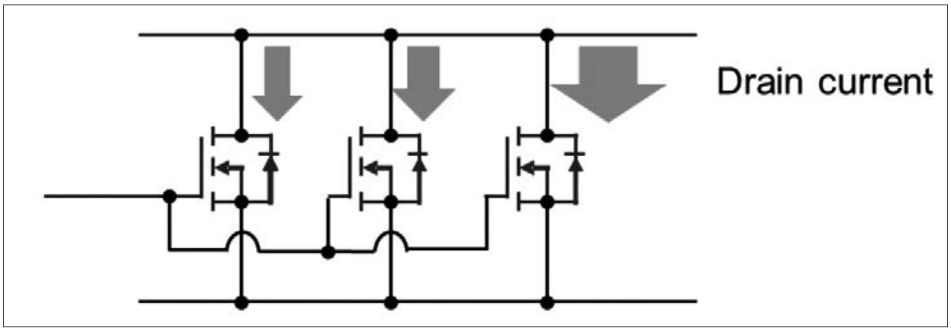
Improved silicon technology

Trench MOSFETs have evolved through several generations. One of the most important targets, with each successive process generation, has been to improve trench filling and so achieve closer spacing between trenches resulting in lower $R_{DS(ON)}$ per die area. Device capacitances and therefore gate charge can be kept low, which is essential to maintain switching performance and minimize the load placed on gate-driver circuitry. Improvements in trench fabrication have reduced these parameters in successive technology generations.

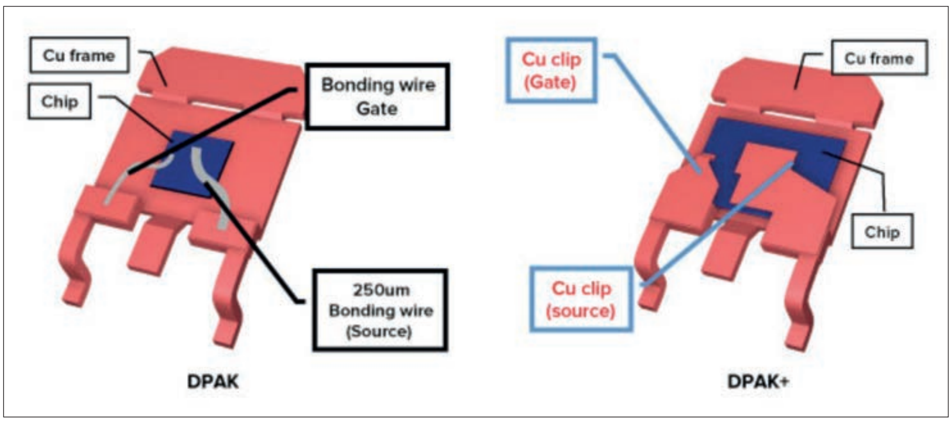
Devices based on Toshiba's UMOS VIII-H



ABOVE: Advances in trench MOSFET technology have enhanced conduction and switching performance



ABOVE: Not evenly distributed drain currents in case of wider Vth spec



LEFT: Copper-clip technology replaces bondwires with electrically and thermally efficient gate and source connections

process offer switching ripple suppression capability and can help designers reduce overall EMI noise. This can be seen in the latest products such as the TK160F10N1L MOSFET for automotive applications. Featuring a maximum $R_{DS(ON)}$ of 2.4 mΩ, this 100 V / 160 A power MOSFET delivers a much tighter threshold voltage (V_{th}) specification – a very important consideration for switching applications - than previous devices.

In automotive power switching applications a tighter V_{th} specification could contribute to a dead time reduction in half-/H-/B6-bridge schemes. This is because the maximum V_{th} difference between low-side MOSFET and high-side MOSFET is smaller. In applications where MOSFETs are connected in parallel, a tighter V_{th} spec leads to improved synchronous switching among paralleled MOSFETs. As a result, the switching loss will be distributed more evenly among the MOSFETs. If a single MOSFET turns on earlier or turns off later than other MOSFETs in parallel, the switching loss concentrates on this single MOSFET.

UMOS VIII-H semiconductor process has been used in the TK160F10N1L. U-MOS VIII-H suppresses switching ripple and can contribute to EMI noise reduction. Target applications for the new MOSFET include automotive motors in 48 V systems, DC/DC converters and load switches.

UMOS IX-H MOSFETs improve transistor FOM such as $R_{DS(ON)}$ x A (on resistance x die area) and $R_{DS(ON)}$ x C_{iss} (on resistance x input capacitance), resulting in better conduction performance and lower gate-drive losses. In addition, reduced output capacitance (C_{OSS}) reduces output charge (Q_{OSS}) leading to better switching efficiency.

Toshiba has reduced die resistance by 42 % in its latest UMOS IX-H Silicon, compared to the UMOS VIII generation, leveraging advances such as improved trench filling – 30 V and 60 V N-channel UMOS IX-H MOSFETs are now in the market. The 30 V devices have ultra-low $R_{DS(ON)}$ of 0.6mΩ (max.) at V_{GS} = 10 V, and 2160 pF typical COSS. For the 60 V MOSFET, $R_{DS(ON)}$ is 1.3 mΩ and typical C_{OSS} is 960pF.

Package technology minimising DFPR and more

As the $R_{DS(ON)}$ of successive device generations has fallen continuously from one generation to the next, the impact of package parasitic effects on overall device performance has become more significant. Increasing the cross-sectional area of the package leadframe and terminations, together with more efficient ohmic connections to the die metallization, helps to reduce the die-free package resistance (DFPR), leading to lower overall MOSFET on-state resistance.

A new DPAK+ power package has been developed, which has the same dimensions and outline as the conventional DPAK but uses copper clips to connect the gate and source pins directly to the metallized electrodes on the die. These copper clips replace the aluminium bondwires, and benefit from a large cross-section and increased contact area at the die. This has yielded a 73 % improvement in DFPR. This significantly reduces I^2R losses due to the package, and also allows higher maximum current. The TO-220SM(W) power package featuring copper-clip technology has an outline comparable to that of the conventional D2PAK (TO-263), but in addition a source pin more than three times wider. These enhancements boost maximum current rating to 200A, while reducing the total board footprint by more than 13 % to just 13 mm x 10 mm.

The enhanced electrical conductivity of the connections in packages such as copper-clip lowers overall energy loss within the device and therefore contributes to reducing heat generation. The larger conductors also increase the package-limited current-carrying capability. Although this can help equipment designers increase the power density of new designs, increased current obviously increases power dissipation due to I^2R. The imperative to remove heat effectively from the package becomes even more urgent.

Additionally DSOP Advance connects the source metallization on the upper surface of the die directly to a large electrode on the top side of the package. This not only utilizes the upper package surface to dissipate heat, but allows the drain electrode on the underside to be much larger than is possible in the conventional SOP. DSOP devices can be used with an ordinary FR4 substrate and can help to significantly reduce system temperatures. Testing the DSOP Advance alongside the conventional SOP has shown a 26 % improvement in dynamic thermal resistance (R_{TH}). DSOP Advance has the same footprint as the standard 5 mm x 6 mm SOP designed for single-sided cooling.

Other thermally enhanced packages such as SOP Advance, TSON Advance and PS-8 maximize heat dissipation through the underside of the device only, and are suited to cost-sensitive applications at lower power levels. TSON Advance achieves comparable power dissipation to the conventional 5 mm x 6 mm SOP-8, but within a 64 % smaller footprint of just 3.3 mm x 3.3 mm.

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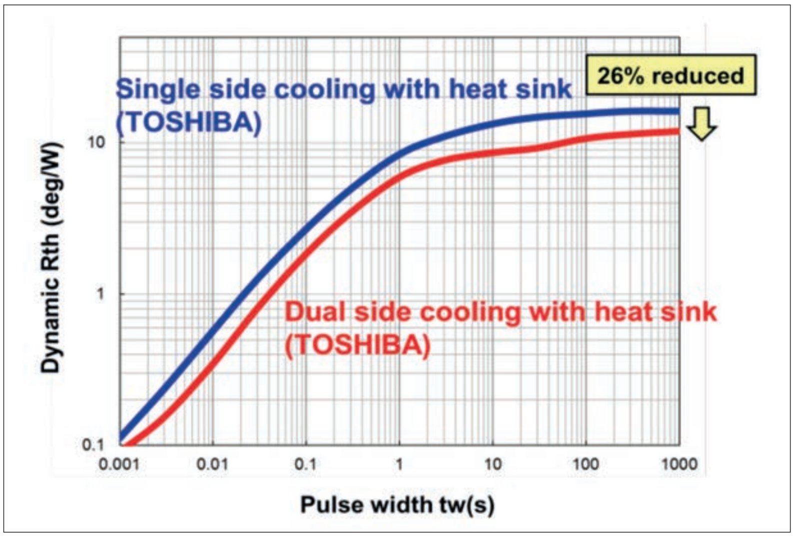
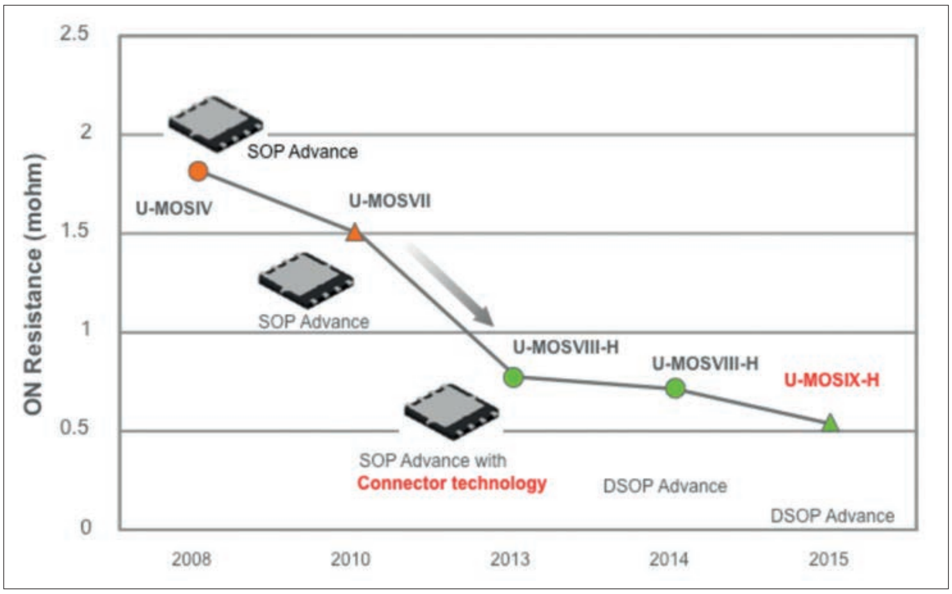


DSOP Advance significantly improves dynamic thermal resistance



Reduction in trench MOSFET RDS(ON) with Silicon and package technology advances

GaN FETs Enable Large Area Wireless Power Transfer

To ensure widespread adoption, wireless power systems need to move beyond small charging pads and become active power sources over large surface areas. For magnetic resonant systems, this demands fundamental changes in coil technology, system architecture, and power amplifiers. Gallium nitride based amplifiers have proven capable of delivering 60 W with greater than 90 percent efficiency into the transmit coil over a wide load range [1]. **Yuanzhe Zhang, Applications Engineer and Michael A. de Rooij, V.P. Applications Engineering, Efficient Power Conversion Corporation, USA**

Today's 6.78 MHz highly resonant wireless power solutions are dominated by mobile device charging based on the AirFuel™ standard [2], which offers numerous discrete transmit power levels; for example 16 W [3] and 33 W [4]. These discrete power levels limit users to relatively small charging pads with areas less than 650 cm^2 (100 in^2). Large area wireless power systems have already demonstrated to be feasible with a small office desk by developed by Efficient Power Conversion Corporation, shown in Figure 1.

Large area wireless power system architecture

There are many architectures and configurations that can be employed to create a large area wireless power system – concepts from using a primary amplifier with repeaters, a smaller induction coil to a large resonant coil powered by a single high power amplifier, to using multiple coils each with its own amplifier which is the approach used in this article and shown in Figure 2.

Multiple coil systems scale in discrete steps but require precise synchronization among the amplifiers. This is needed to ensure that any device (load) large enough to couple to two or more coils receives power, in-phase, from each of the sources. The physical distance between the amplifiers however, makes it challenging to distribute the 6.78 MHz clock with low jitter and minimal timing distortion.

A negative aspect of the multiple coil architecture is that the coils cannot be located too close to each other as they will couple and energy from one amplifier can flow back into another. This problem can be reduced by using high output impedance amplifiers, such as the Class E. Coil separation with coupling lower than -17 dB yields the best performance but will have a power gap between the coils that may be deemed unacceptable.

Amplifiers for high power wireless power transfer

Large area wireless power coils are expected to power many devices simultaneously and therefore require higher power amplifiers with power ratings that increase proportionally to the surface area to be powered. The choice of wireless power architecture also affects the amplifier topology and configuration

Figure 1: Highly resonant wireless powered table with various devices

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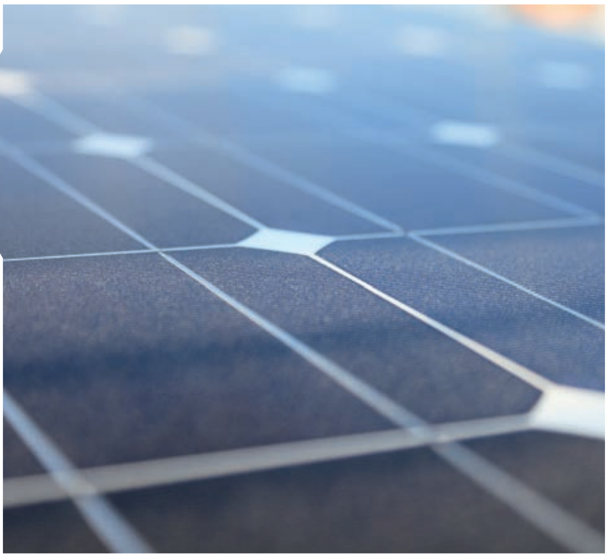

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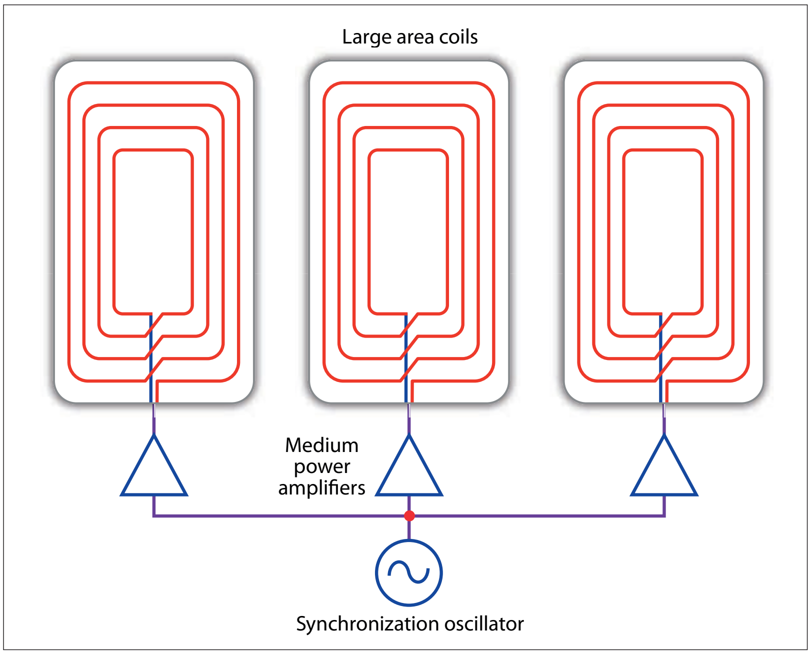

Figure 2: Multiple coil and amplifier architecture for a large area wireless power system

Device description	*Power*	*Function*
Laptop	25 W - 45 W	Power and charging
Monitor (< 27")	20 W - 40 W	Power
Tablets	13 W	Charging
Smartphone	5 W - 13 W	Charging
Lighting	5 W - 10 W	Power
Miscellaneous	5 W - 10 W	Power
Total Power Requirement	**73 - 131 W**	

Table 1: List of devices with power requirements and function for a small office desk

choices based on higher voltage or current drive requirements.

Power requirement is directly related to the targeted application. In the case discussed here, the target application is an office desk (about 5000 cm^2) that can accommodate multiple devices with various power requirements. Table 1 gives a list of typical devices that can be found on such an office desk with their respective power requirements and power function. Table 1 also shows that the maximum total power needed for this application is 131 W. Losses in the system also need to be accounted for when determining the power requirements for the source coil and amplifier. The larger the power surface area the higher the operating losses become and methods for efficiency improvement become increasingly important given this application will be subject to efficiency standards [6].

For the multiple-coil system, an increase in power capability for the amplifier can still be achieved using existing topologies [7]. High power amplifiers have higher operating voltage and current that increases the stress on the switching devices. eGaN FETs are excellent candidates due to their significantly lower parasitic capacitance and zero reverse recovery charge. A large area wireless power system for a small office desk [1] will require amplifier topologies capable of delivering 60 W.

Only the differential-mode versions of the class E [7, 8, 10] and ZVS class D [7, 8, 9, 10, 11] amplifiers will be considered for this example. The class E amplifier remains a popular choice, and due to its simplicity and the reduction in imaginary impedance shift from the large area coil due to external influences allows it remains a viable candidate for higher power. The choice of ZVS class D amplifier is based on its proven track record at higher power [8].

Evaluation of wireless power amplifiers

The circuits used to evaluate the multiple-coil large-area wireless power system suitable for an office desk is shown in Figures 3 and 4. The target power capability is 180W, sufficient to power the loads, including system losses, are described in Table1. The system is comprised of three wireless power coils, each with an area of 980 cm^2 (22.5 cm x 43.5 cm). The use case for the operating impedance range for each coil needs to be determined, as there is no AirFuel standard to reference for guidance.

The three coils are evenly spaced to cover a total area of 5000 cm^2 (100 cm x 50 cm). The separation between coils was experimentally determined that magnetic coupling needed to be lower than -17 dB in order to prevent impacting its neighbor. Each amplifier is required to deliver at least 60 W into the coil, which is double its previous capability [8, 10].

A differential-mode class E amplifier was designed based on the EPC2046 eGaN FETs [11] chosen for its low $R_{DS(on)}$ and low C_{OSS}. In particular, the low C_{OSS} made it possible to design this amplifier to be capable of delivering 60 W into the coil without the use of a heat sink for the reflected resistance range.

A differential-mode ZVS class D amplifier was designed using EPC2007C [12] FETs, which were chosen for their low $R_{DS(on)}$ and low C_{OSS}. This amplifier design has already

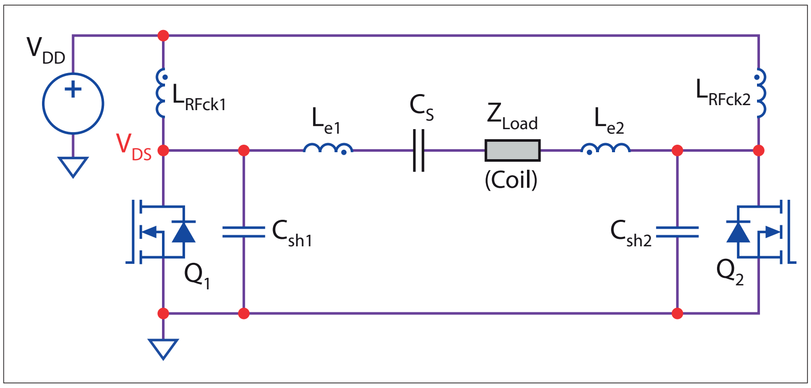

Figure 3: Differential class E amplifier

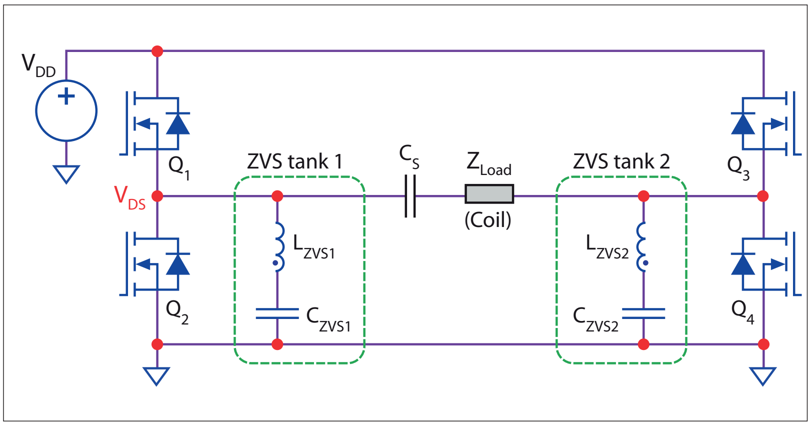

Figure 4: Differential zero-voltage switching (ZVS) class D amplifier

proven capable of delivering 100 W into the coil [13]. The design methodology is given in [7].

At the heart of the multiple coil architecture is the synchronization circuit to ensure that each amplifier operates in-phase. The details of the synchronization circuit are given in [1].

Experimental results

Both the class E and ZVS class D amplifiers were tested using a discrete programmable load. The tests performed were limited, based on either FET drain-source voltage reaching 80 % of rated or device temperature exceeding 100°C in an ambient of 25°C.

The efficiency performance of the class E amplifier is shown in Figure 5 and reveals that the amplifier efficiency largely exceeds 90 % when delivering 60 W full power across the reflected imaginary impedance range. At 60 W, the class E amplifier is capable of driving a relative imaginary impedance range of 35j Ω. Figure 6 shows the measured drain-source voltage across one of the FETs in the class E amplifier while delivering 60 W into a 15.5 + 0j Ω load. At this operating point, the load current is 2 A and the supply voltage to the differential-mode class E amplifier is 26.8 V.

Measured efficiency of the ZVS class D amplifier based on the EPC2007C eGaN FET was tested, with efficiency shown in Figure 7. Off-resonance operation has a large impact on this amplifier due to the C_{OSS} of the EPC2007C that requires energy to maintain ZVS and contributes to the ZVS transition time. This shows that an optimal FET with lower COSS than the EPC2007C will yield higher off resonance amplifier efficiency.

Figure 8 shows the measured drain-source voltage across one of the FETs in the EPC2007C based ZVS class D amplifier while delivering 60 W into a 15.5 + 0j Ω load. At this operating point, the load current is 2 A and the supply voltage to the differential-mode class E amplifier is 36.6 V.

The class E amplifier used a new EPC2046 fifth-generation eGaN FET, which has a lower C_{OSS}·$R_{DS(on)}$ figure of merit than previous generations of eGaN FETs, such as those used in the ZVS class D amplifier. A 100 V fifth-generation eGaN FET with optimal $R_{DS(on)}$ suitable for this application will be tested once it becomes available.

Finally, a multiple coil large-area wireless power system was constructed that covers a total power surface area of 5000 cm². The system was made up of three ZVS class D amplifiers, three large area coils (each approximately 1000 cm²), and the synchronization circuit. The measured timing mismatch between each of the four outputs of the synchronization circuit was less than 600 ps, thus ensuring precise phase alignment of each amplifier in the system. The large-area, multiple coil system was provided with various loads such as a laptop rated at 25 W, a 20" monitor rated at 21 W, office lamp rated at 6 W, and more. The operation of the large area system was discussed in [14].

Conclusions

The key to large area wireless power lies in both innovative coil technology and high power (> 60 W) amplifiers enabled by eGaN FETs. Large area wireless power coils have inherently different characteristics than traditional coils in that they have lower increase in inductance per increase in area, shorter magnetic field radiation, and are more immune to imaginary

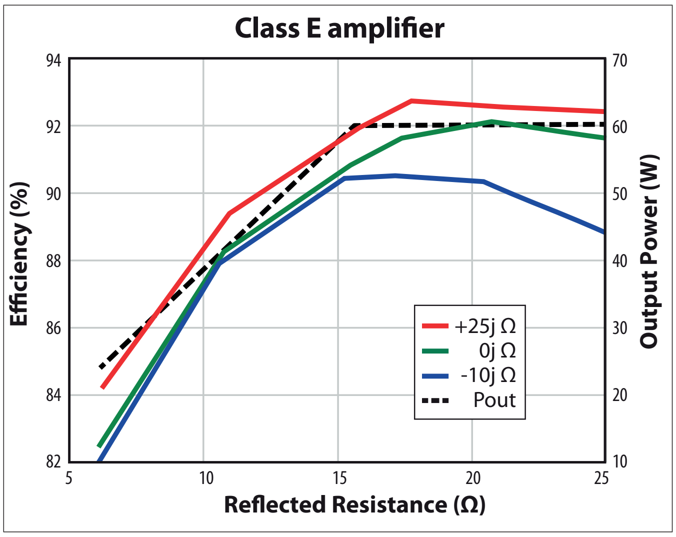

Figure 5: Measured efficiency and output power of the class E amplifier for a range of load impedance

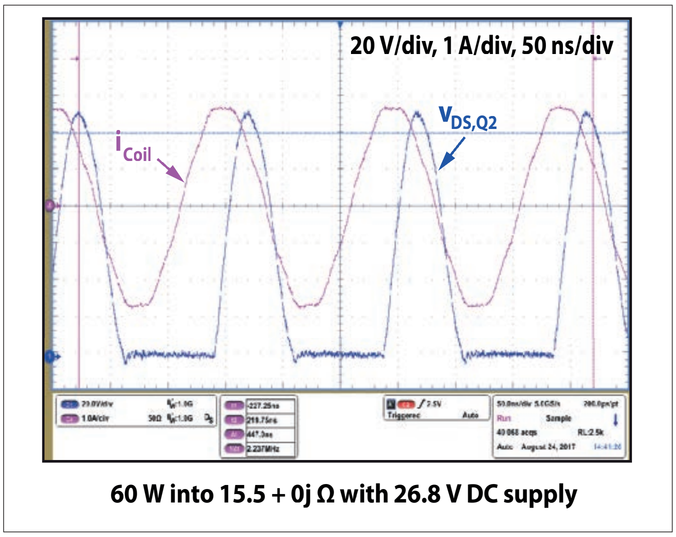

Figure 6: Measured drain-to-source voltage (V_{DS}) and output current (i_{coil}) waveforms of the Class E amplifier delivering 60 W into 15.5 + 0j Ω with 26.8 V DC supply

impedance shifting.

A multi-coil, multi-amplifier approach using three eGaN FET-based, 60 W capable differential-mode amplifiers was constructed and tested. Both the class E amplifier and the ZVS class D exhibited greater than 90 % efficiency at full power. Further improvements can be expected from the ZVS class D when fitted with lower $R_{DS(on)}$ eGaN FETs. The work presented in this article underscores the challenges ahead for large area wireless power systems design to achieve high-efficiency with high-power amplifiers.

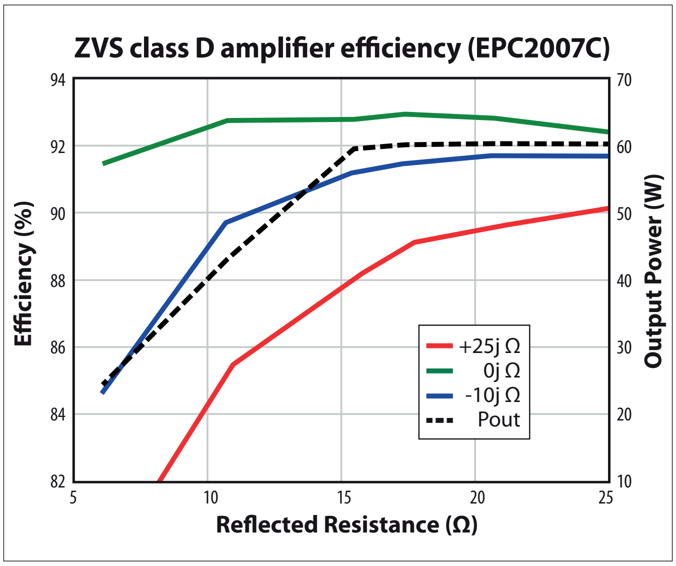

Figure 7: Measured efficiency and output power of the EPC2007C based ZVS class D amplifier for a range of load impedance

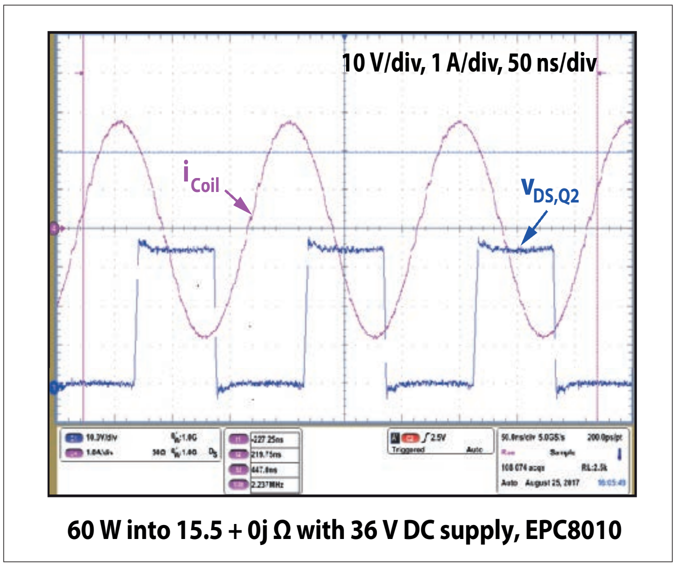

Figure 8: Measured drain-to-source voltage (V_{DS}) and output current (i_{Coil}) waveforms of the ZVS Class D amplifier delivering 60 W into 15.5 + 0j Ω with 36.6 V

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A System-Level Power Architecture Design Tool

Modern electronic systems have an increasing level of complexity. There can be a large number of power rails and supply solutions on a system board to power many different loads. Before choosing or designing each individual power supply, the system hardware engineer first needs to understand the system power needs and then architect the system power tree accordingly to optimize the power management system efficiency, size and cost. Due to the complexity of the system, sometimes system-level power optimization is not a trivial task. An intuitive system-level design tool addresses this need.

Henry Zhang, Applications Engineering Manager, and Tim Kozono, Applications Engineer, Linear Technology Corporation, USA

The LTpowerPlanner program is a system-level power tree design tool to help system designers plan, design and optimize a power management system. It provides an intuitive graphic user interface (GUI) to greatly simplify system-level design tasks.

The LTpowerPlanner tool helps users to

- draw a "power tree" type system block diagram
- calculate/estimate total system input power, output power, power loss, efficiency and board size
- compare different power architectures for system-level optimization
- interface with the LTpowerCAD supply design tool and with the LTspice circuit simulation tool
- intuitively document and present the system solution.

The design tool is part of the LTpowerCAD design tool program. To open the LTpowerPlanner tool, users can click the "System Design" icon on the LTpowerCAD main page, as shown in Figure 1. The LTpowerCAD program is an off-line program running on a Windows PC and is available for free download.

Three basic design steps

To get started, here are three basic steps to use the LTpowerPlanner design tool.

Step 1 - drawing a system power tree

Figure 2 shows an example of using the LTpowerPlanner tool to draw a simple system power tree. There are three types of key components in a power tree: input power source, power supply converter and load device. The power source component only has an output terminal and the load component only has an input terminal. As to each converter component, the left side terminal is a power input terminal, and the right side terminal, is a power output terminal. The

Figure 1: Click the "system design" icon to open ltpowerplanner tool

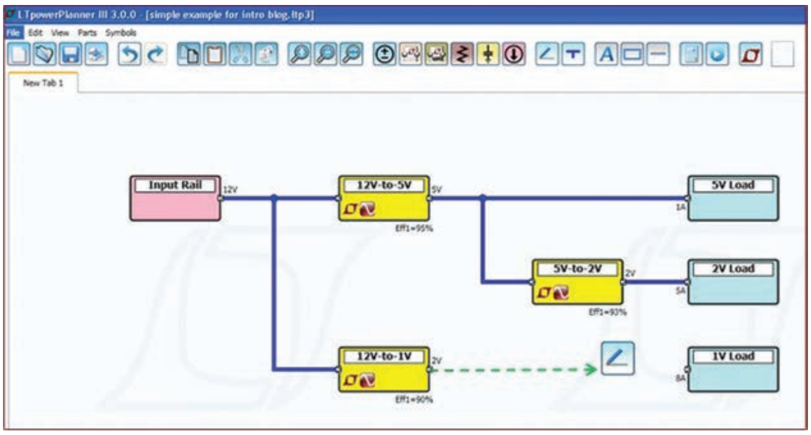


Figure 2: Drawing a system power tree

converter component can have multiple output rails to represent a multi-channel power supply. Similarly, the load component can have multiple input rail terminals. The user can place these components first, then connect the components with power wires from left to right, which is the default current/power flow direction.

Step 2 - updating component parameters

The user can double click on each component to update its key power parameters in its "Properties" window, such as input voltage range, output voltage, maximum load current, etc. The user also may enter the expected efficiency and estimated size for each power converter component for a system calculation (see Figure 3).

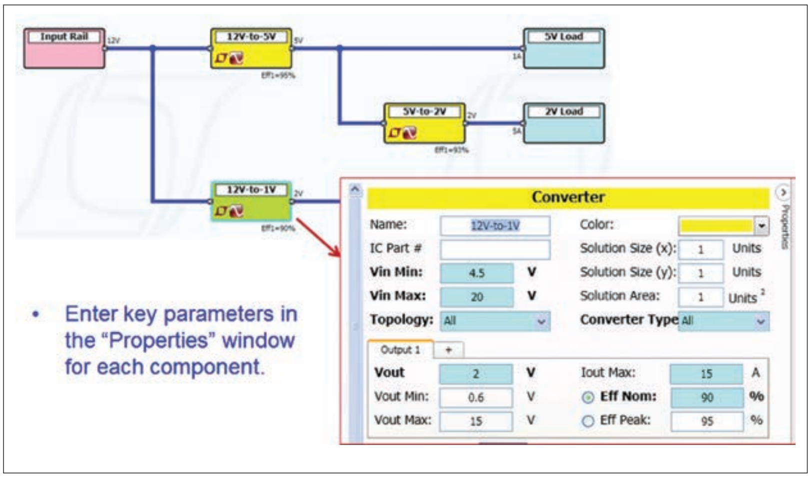


Figure 3: Updating key converter parameters

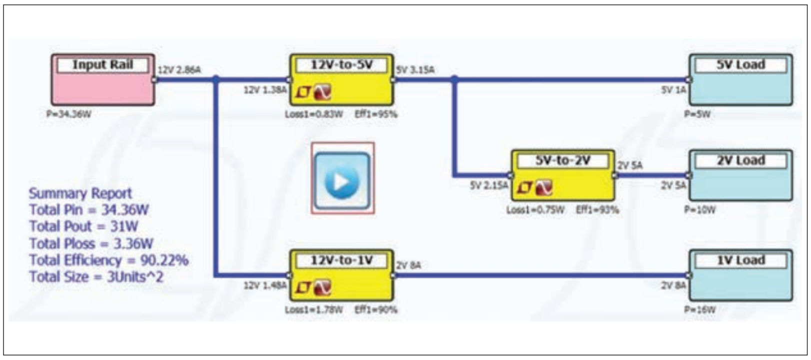


Figure 4: Running a system calculation

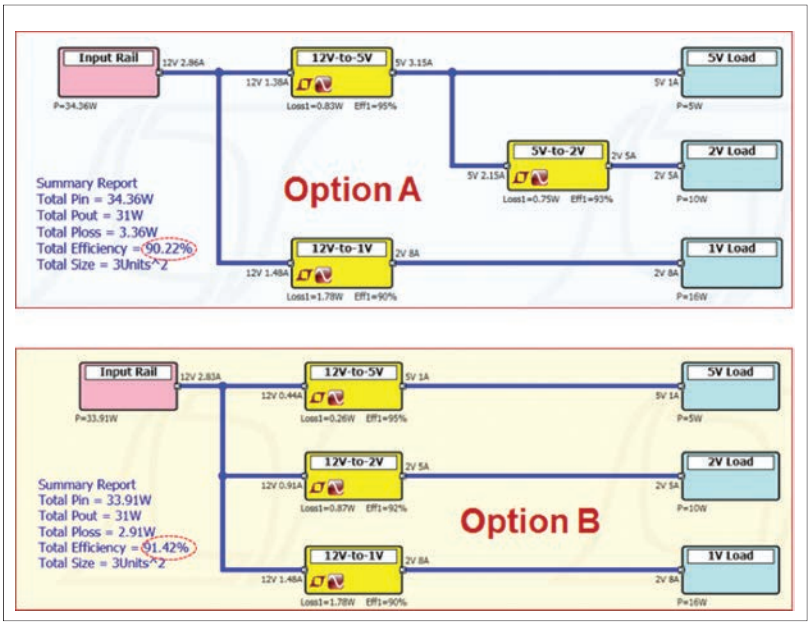


Figure 5: Comparing two power system architectures (A and B)

Step 3 -running a system calculation

After a user completes the power tree and updates all key parameters, the user can run a system calculation. Based on the entered parameters for each component, the program calculates and displays the following values in its on-screen "Summary Report:" total system input power, output power, power loss, efficiency and the sum of the converter PC board areas. As shown in Figure 4, each component terminal also displays its input or output voltage and current. Each converter's efficiency and power loss are displayed under the converter. Each load and power source's power level is shown as well. This GUI interface provides a very intuitive display with lots of details of the system power tree.

The LTpowerPlanner tool can be used to compare different power architectures to achieve an optimum system solution. Figure 5 shows a simple example of comparing two slightly different power tree options A and B. In this case, the LTpowerPlanner tool shows that a small architectural change from option A to option B can quickly improve the system efficiency.

Example of an FPGA power tree

The planner tool can be used to draw much more complicated systems. An example is given in Figure 6. There are multi-output power converters and multi-input loads shown in this example. Multiple output terminals with the same voltage can be paralleled for current sharing as well. There are also resistive components available to represent voltage drop and power loss. Please see the LTpowerPlanner User Guide for details of the tool's advanced features and functions.

Although the LTpowerPlanner program is a generic system tool, it allows a user to link a power converter to existing design and simulation files generated by the LTpowerCAD supply design tool and the LTspice circuit simulation tool. To do so, in the converter "Properties" window, a user needs to link the converter to the specific files on their PC disk. After the links are established, users can directly open the linked LTpowerCAD design file or LTspice simulation file by clicking the

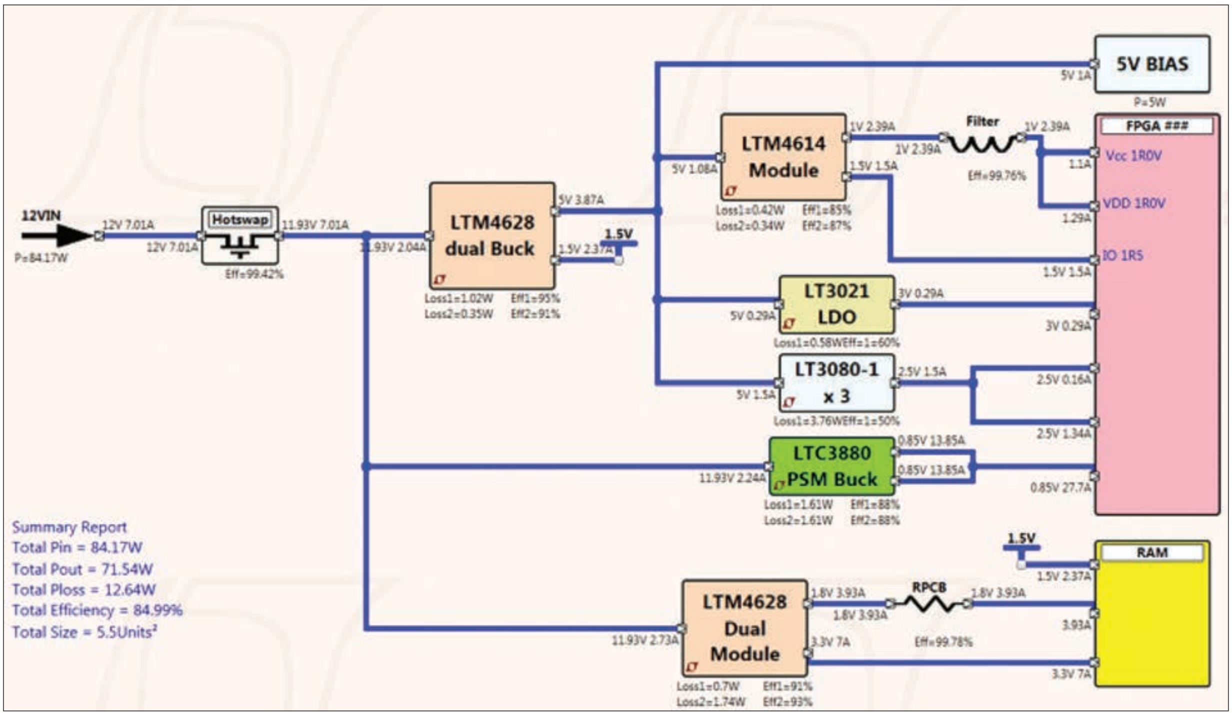


Figure 6: An example FPGA power tree

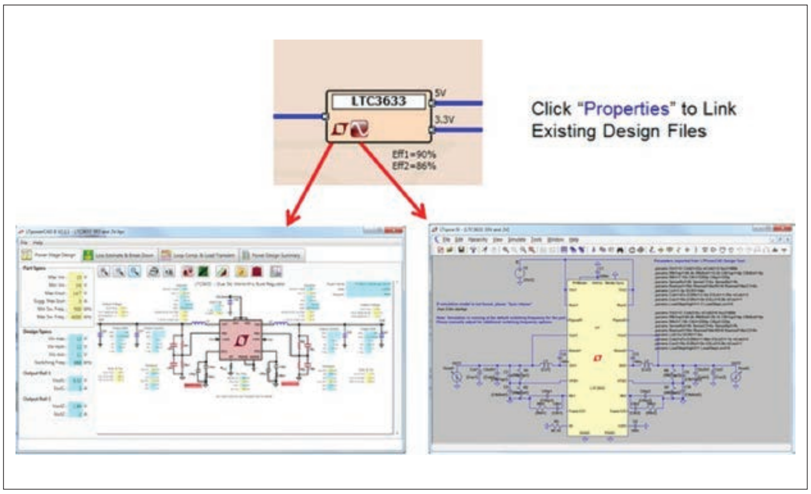


Figure 7: Linking to existing LTpowerCAD and LTspice files

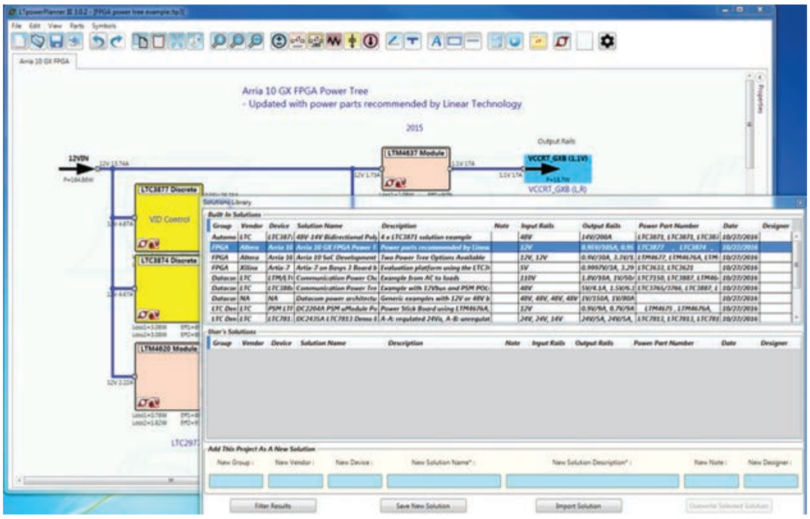


Figure 8: LTpowerPlanner Power Tree Solution Library

corresponding icons on the LTpowerPlanner converter as shown in Figure 7. This feature provides a convenient and systematic way to organize all the design files for a power management system.

Power tree solution library

There is also a built-in LTpowerPlanner power tree solution library to provide many reference power tree designs to users. As shown in Figure 8, by clicking the "Solution Library" soft key, users can leverage many existing solutions for applications such as FPGAs, processors, data communication and automotive systems, etc. These existing designs save engineers time to understand and design a similar power management system. Furthermore, users can also save their designs and build a user solution library for future use.

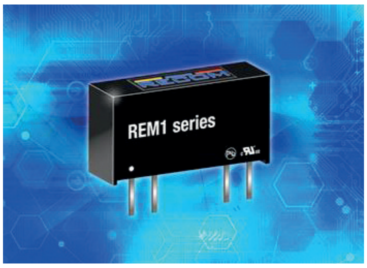
Conclusion

The LTpowerPlanner design tool can help system engineers to design and optimize a power management system in a very effective and intuitive way. Based on the user's inputs, the tool calculates total input power, output power, power loss, efficiency and physical size of the system. System designers can use this tool to draw, design, compare and optimize the power system tree. This tool also provides a nice and convenient way to document and present the system power architecture.

2MOPP 1-Watt DC/DC Converter in Compact SIP7 Module Save Space, Energy, and Time at the Test House

Ready to save space in medical-device designs, the RECOM REM1 series, now available from Dengrove Electronic Components, is a 1-Watt DC/DC converter family certified to medical IEC/EN/ANSI/AAMI 60601-1 and general IEC 62368-1 equipment safety standards. The series is also covered by a CB Test Report, which simplifies access to international markets.

Packaged as compact SIP7 modules, the converters provide two means of patient protection (2MOPP), with 250V working voltage, 5.2kV/1-minute isolation, and 8mm creepage and clearance, within the 19.6mm x 6.0mm x 10.2mm outline.



In addition to meeting high safety standards and helping new OEM products pass approval tests quickly and economically, the REM1 series also delivers flexibility and high performance. Input-voltage options are 3.3V, 5V, 12V, 15V, or 24V, and the output can be 3.3V, 5V or 12V. Maximum efficiency of 85% keeps power dissipation low, and enables the converters to operate in ambient temperatures from -40°C to 90°C without derating.

The 1W REM1 series complements the existing RECOM 3W, 6W and 10W REM families of medical DC/DC converters. The new devices comply with IEC 60601-1-2 medical EMC specifications, and meet Class B EMC with a simple L-C filter placed at the output.

The full line is in stock now, and comes with a five-year manufacturer's warranty.

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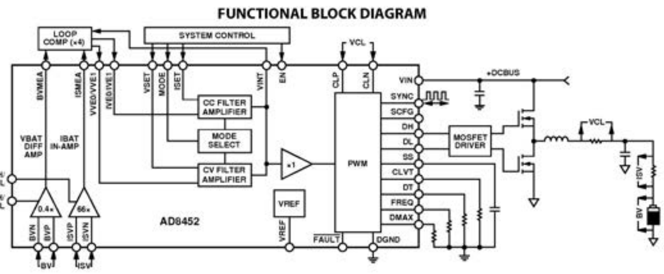
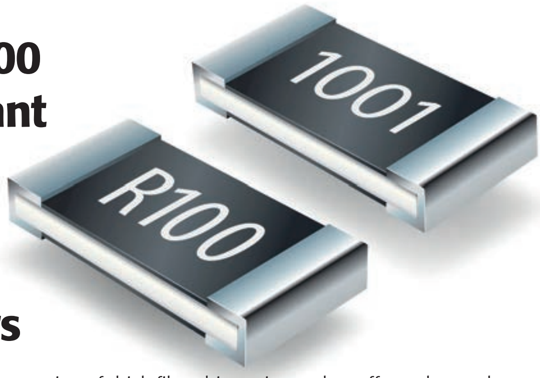


Li-Ion Testing & Formation Pack

Analog Devices introduced a precision integrated analog front end, controller, and PWM for battery testing and formation capable of increasing system accuracy and efficiency in lithium-ion battery formation and grading. According to company information, the new AD8452 provides 50 % more channels in the same amount of space, adding capacity and increasing battery production throughput. The AD8452 uses switching technology that recycles the energy from the battery while discharging and delivers 10 times more accuracy than conventional switching solutions. The higher accuracy allows for more uniform cells within battery packs and contributes to longer living batteries in applications such as electric vehicles. It is suitable for systems of 20 Ah or less with up to 95 % power efficiency. It also enhances the safety of manufacturing processes by providing better detection and monitoring to help prevent over and undercharging which can lead to battery failures. The AD8452 delivers bill of material (BoM) cost savings of up to 50% for charging/discharging boards and potential system cost savings of approximately 20 %. System simulating demonstration boards will be available and can enable lower R&D engineering cost and shorter time to market for test equipment manufacturers.

www.analog.com/AD8452?adicid=PRLS_EU_P1704

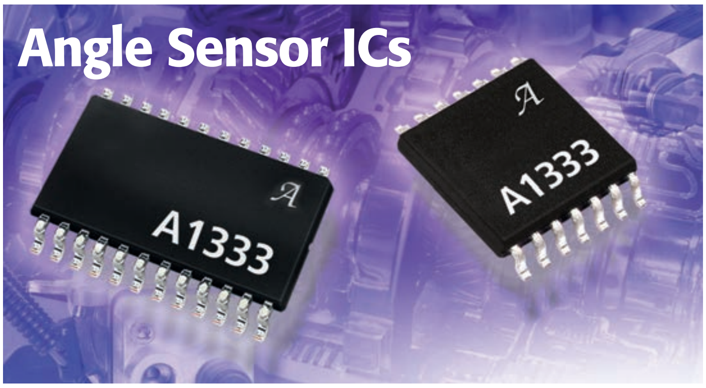
AEC-Q200 Compliant Thick Film Chip Resistors



Bourns released two series of thick film chip resistors that offer enhanced power ratings up to 2 W at 70 °C. The CRMxxxxA and CRSxxxxA are sulfur-resistant and AEC-Q200 compliant making them well-suited for automotive driver assistant, information, entertainment and lighting applications, as well as commercial, automation, industrial, power supply and stepper-motor drive designs. Designed to operate in harsh environments where there are elevated levels of sulfur contamination, the resistor series have been tested in accordance with ASTM B809-9 methods. Made using a thick film element printed onto a ceramic substrate, the resistors offer additional product lifespan benefits compared to standard film resistors when exposed to a sulfurous gas environment. The chip resistors are available in six different footprints from small 0603 (1608 Metric) up to 2512 (6431 Metric). The Model CRMxxxxA provides a wide resistance range up to 1 MΩ and low resistance values from 0.05 Ω. This models' high power rating makes it a solution for current sensing. In addition, the Model CRSxxxxA delivers superior pulse load capabilities for enhanced protection of today's smaller, more sensitive electronic designs.

www.bourns.com/products/fixed-resistors/sulfur-resistant

Angle Sensor ICs



Allegro MicroSystems Europe has introduced two 0° to 360° angle sensor ICs that provide contactless high-resolution angular position information based on magnetic Circular Vertical Hall (CVH) technology. Allegro's A1333 and A1339 devices include a system-on-chip (SoC) architecture that includes a CVH front end, digital signal processing, and supports multiple digital output formats, including Allegro's first motor commutation outputs (UVW), and encoder outputs (A, B, I) for angle sensor ICs that can operate at either 3.3 V or 5 V. The A1333 and A1339 are offered in both single and dual die versions for systems that require redundant sensors. They both include on-chip EEPROM technology, capable of supporting up to 100 read/write cycles, for flexible end-of-line programming of calibration parameters. Both devices are ideal for automotive applications requiring 0° to 360° angle measurements, such as motor position measurements for steering and braking systems and other high speed actuators for pumps and transmissions that require low latency and high resolution. The A1339 also includes an integrated turns counter and low power mode features that enable it to track changes in the target magnetic field in automotive applications even when the vehicle is in the "key off" state.

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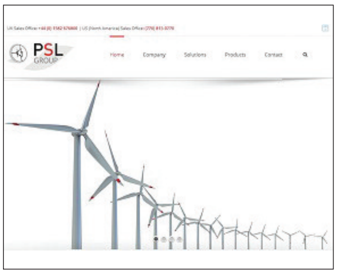

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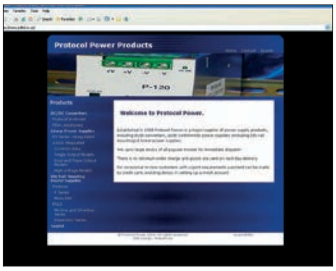

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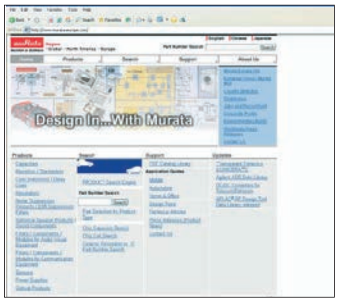

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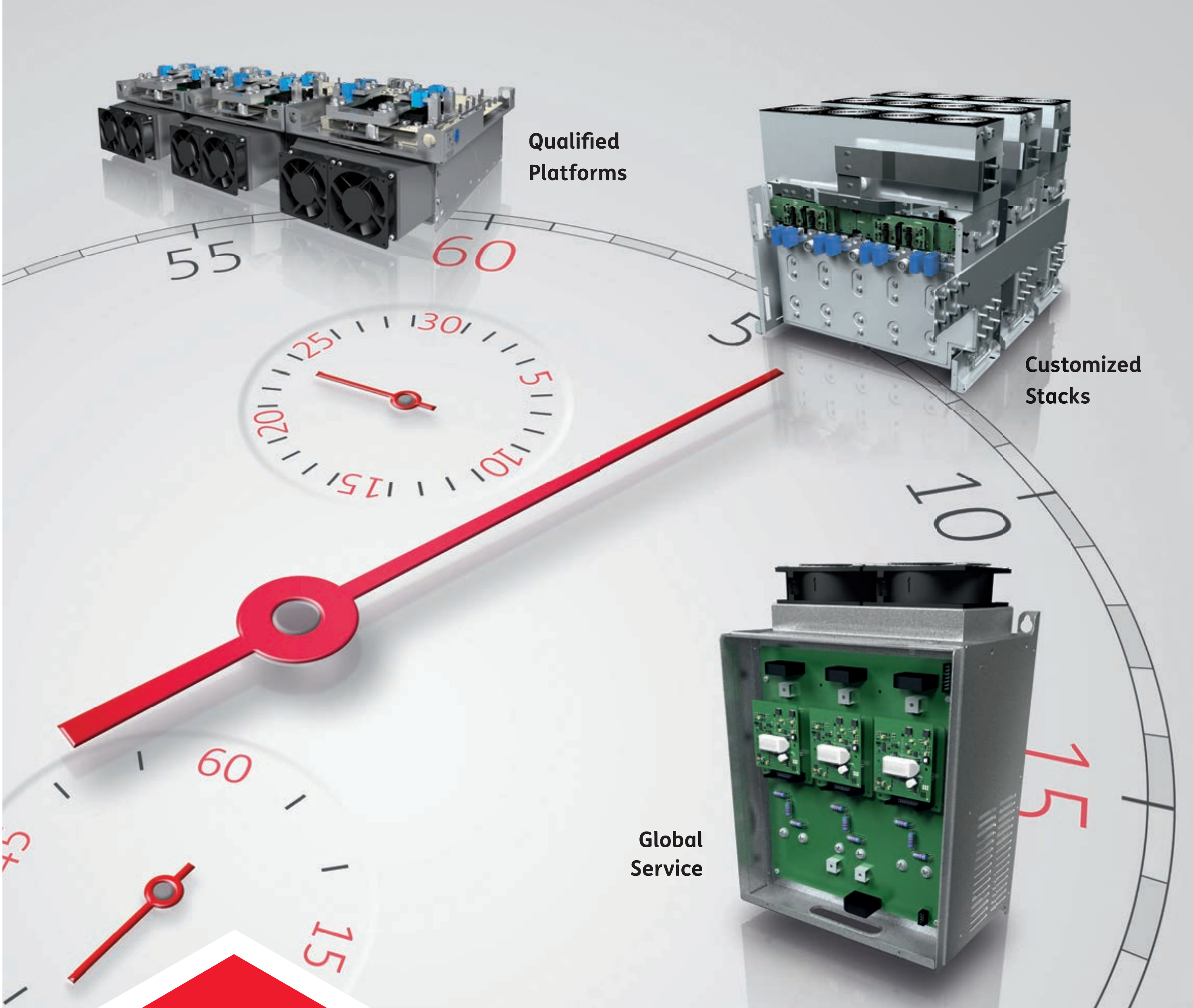

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