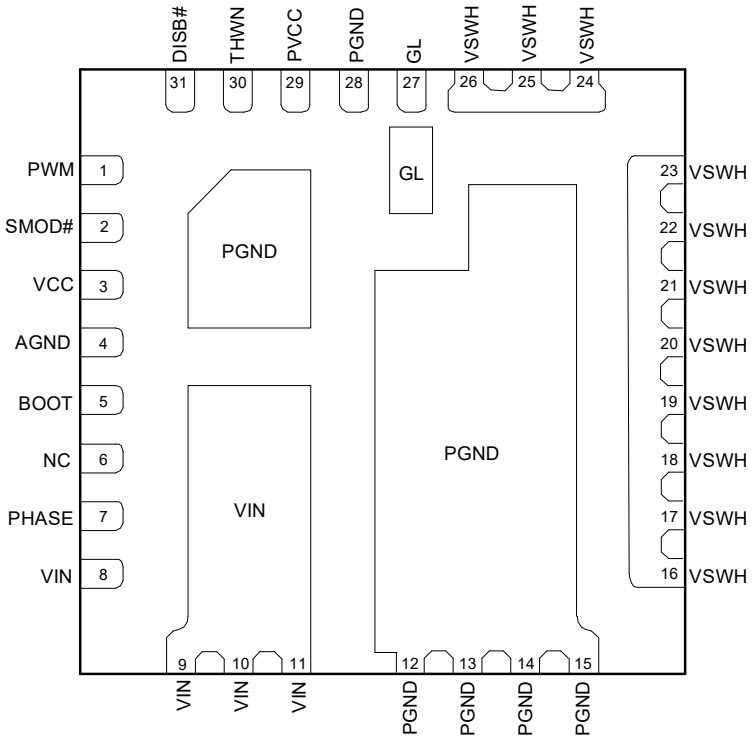
Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ5311NQI	-40°C to 125°C	QFN5x5-31L	RoHS

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration

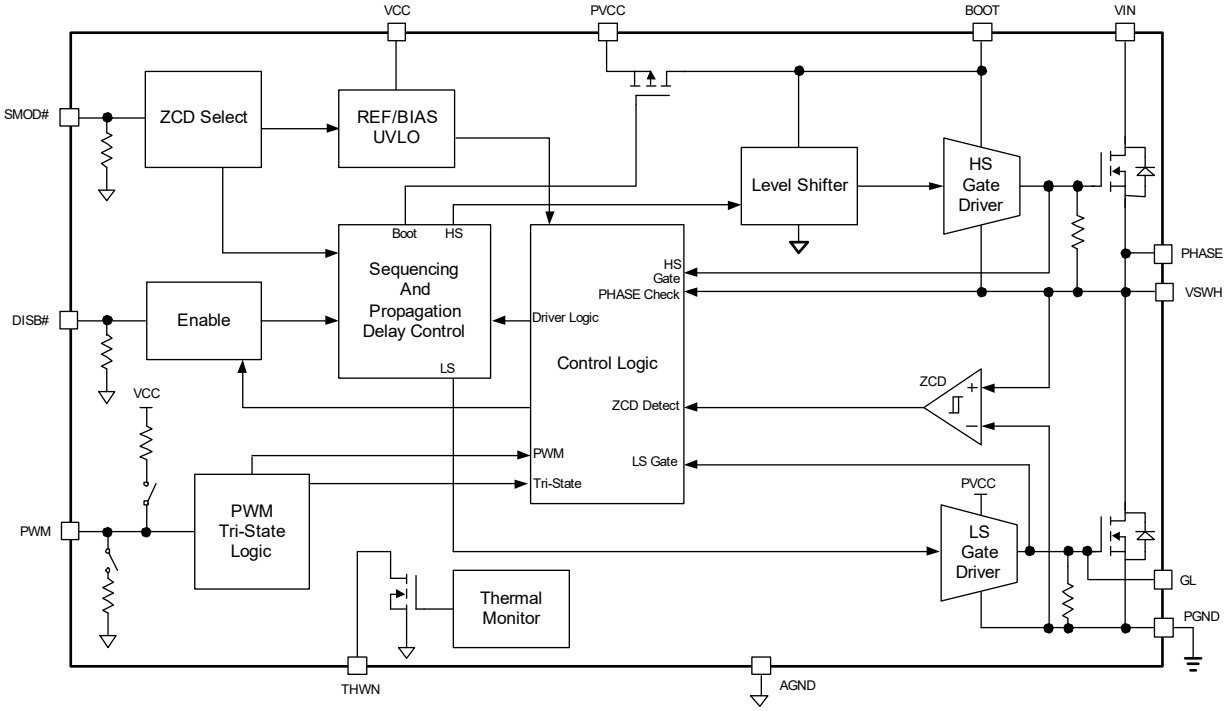


QFN5x5-31L
(Top View)

Pin Description

Pin Number	Pin Name	Pin Function
1	PWM	PWM input signal from the controller IC. When DISB#=0V, the internal resistor divider will be disconnected and this pin will be at high impedance.
2	SMOD#	Pull low to enable Discontinuous Mode of Operation (DCM), Diode Emulation or Skip Mode. There is an internal pull-down resistor to AGND.
3	VCC	5V Bias for Internal Logic Blocks. Ensure to position a 1µF MLCC directly between VCC and AGND (Pin 4).
4	AGND	Signal Ground.
5	BOOT	High-Side MOSFET Gate Driver supply rail. Connect a 100nF ceramic capacitor between BOOT and the PHASE (Pin 7).
6	NC	Internally connected to VIN paddle. It can be left floating (no connect) or tied to VIN.
7	PHASE	This pin is dedicated for bootstrap capacitor AC return path connection from BOOT (Pin 5).
8, 9, 10, 11	VIN	Power stage High Voltage Input (Drain connection of High-Side MOSFET).
12, 13, 14, 15	PGND	Power Ground pin for power stage (Source connection of Low-Side MOSFET).
16,17,18,19, 20,21,22, 23, 24, 25, 26	VSWH	Switching node connected to the Source of High-Side MOSFET and the Drain of Low-Side MOSFET. These pins are used for Zero Cross Detection and Anti-Overlap Control as well as main inductor terminal.
27	GL	Low-Side MOSFET Gate connection. This is for test purposes only.
28	PGND	Power Ground pin for High-Side and Low-Side MOSFET Gate Drivers. Ensure to connect 1µF directly between PGND and PVCC (Pin 29).
29	PVCC	5V power rail for High-Side and Low-Side MOSFET gate drivers. Ensure to position a 1µF MLCC directly between PVCC to PGND (Pin 28).
30	THWN	Thermal warning indicator. This is an open−drain output. When the temperature at the driver IC die reaches the Over Temperature Threshold, this pin is pulled low.
31	DISB#	Output disable pin. When this pin is pulled to a logic low level, the IC is disabled. There is an internal pull−down resistor to AGND.

Functional Block Diagram



Electrical Characteristics[4]

T_A = 25°C to 125°C. Typical values reflect 25°C ambient temperature; VIN = 12V, VCC= PVCC= DISB# = 5V, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
GENERAL						
V_{IN}	Power Stage Power Supply		2.5		20	V
V_{CC}	Low Voltage Bias Supply	PVCC = VCC	4.5		5.5	V
$R_{\theta JC}$[5]	Thermal Resistance	Reference to High-Side MOSFET temperature rise		2.5		°C/W
$R_{\theta JA}$[5]		Freq = 300kHz. AOS Demo Board		12.5		°C/W
INPUT SUPPLY AND UVLO						
V_{CC_UVLO}	Under-Voltage Lockout	VCC Rising		3.5	3.9	V
V_{CC_HYST}		VCC Hysteresis		400		mV
I_{VCC}	Control Circuit Bias Current	DISB# = 0V		1		µA
		SMOD# = 5V, PWM = 0V		550		µA
		SMOD# = 0V, PWM = 0V		535		µA
		SMOD# = 0V, PWM =1.65V		430		µA
I_{PVCC}	Drive Circuit Operating Current	PWM = 400kHz, 20% Duty Cycle		13		mA
		PWM = 1MHz, 20% Duty Cycle		33		mA
PWM INPUT						
V_{PWMH}	Logic High Input Voltage		2.7			V
V_{PWML}	Logic Low Input Voltage				0.72	V
I_{PWM_SRC}	PWM Pin Input Current	PWM = 0V		-150		µA
I_{PWM_SNK}		PWM = 3.3V		150		µA
V_{TRI}	PWM Input Tri-State Window		1.35		1.95	V
V_{PMW_FLOAT}	PWM Tri-State Voltage Clamp	PWM = Floating		1.65		V
DISB# INPUT						
$V_{DISB\#\_ON}$	Enable Input Voltage		2.0			V
$V_{DISB\#\_OFF}$	Disable Input Voltage				0.8	V
$R_{DISB\#}$	DISB# Input Resistance	Pull-Down Resistor		850		kΩ
SMOD# INPUT						
$V_{SMOD\#\_H}$	Logic High Input Voltage		2.0			V
$V_{SMOD\#\_L}$	Logic Low Input Voltage				0.8	V
$R_{SMOD\#}$	SMOD# Input Resistance	Pull-Down Resistor		850		kΩ
GATE DRIVER TIMING						
t_{PDLU}	PWM to High-Side Gate	PWM: H⟶L, VSWH: H⟶L		30		ns
t_{PDLL}	PWM to Low-Side Gate	PWM: L → H, GL: H → L		25		ns
t_{PDHU}	Low-side to High-Side Gate Deadtime	GL: H → L, GH[6]: L → H		15		ns
t_{PDHL}	High-Side to Low-side Gate Deadtime	VSWH: H → 1V, GL: L → H		13		ns
t_{TSSHD}	Tri-State Shutdown Delay	PWM: L → V_{TRI}, GL: H → L and PWM: H → V_{TRI}, VSWH: H → L		25		ns
t_{TSEXIT}	Tri-State Propagation Delay	PWM: V_{TRI} → H, VSWH: L → H PWM: V_{TRI} → L, GL: L → H		35		ns
t_{LGMIN}	Low-Side Minimum On-Time	SMOD# = L		350		ns

Typical Performance Characteristics

T_A = 25°C, VIN = 12V, PVCC = VCC = 5V, unless otherwise specified.

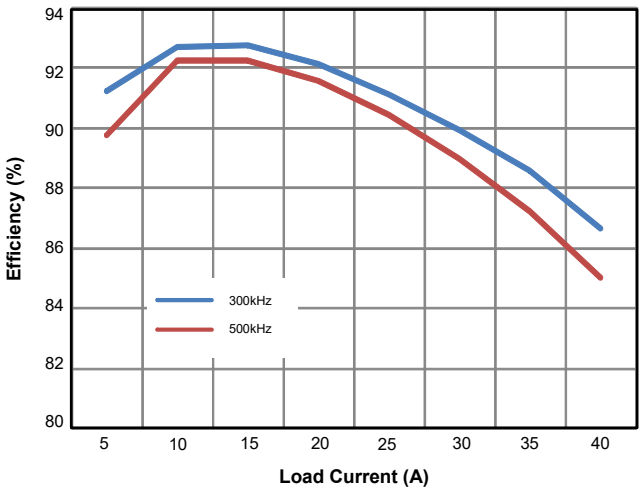


Figure 3. Efficiency vs. Load Current

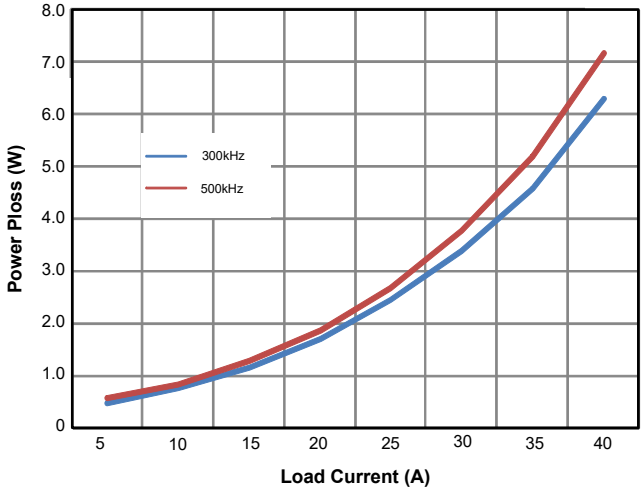


Figure 4. Power Loss vs. Load Current

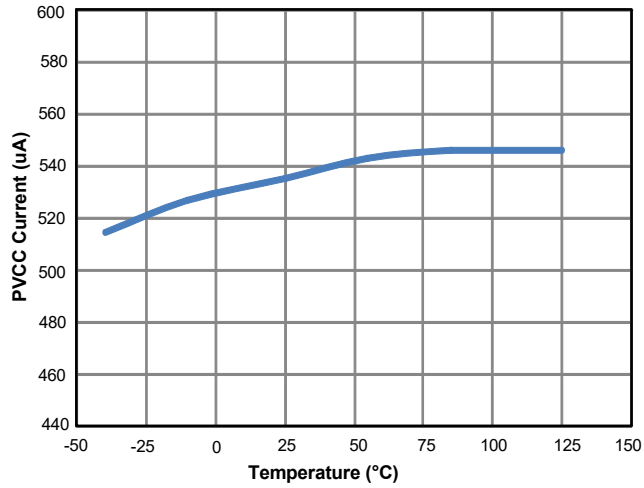


Figure 5. Supply Current (I_{PVCC}) vs. Temperature

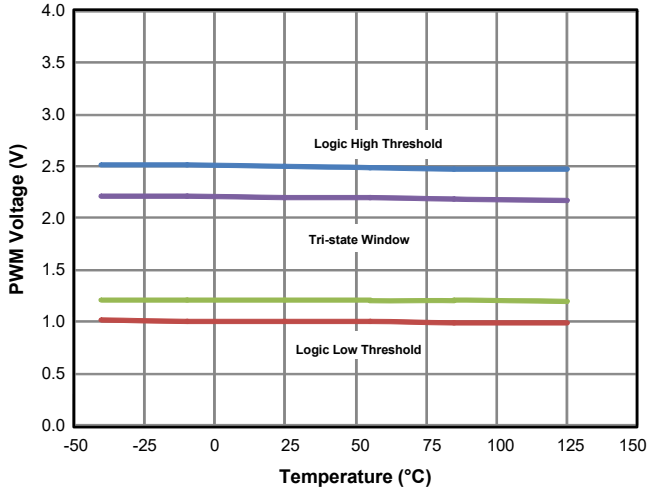


Figure 6. PWM Threshold vs. Temperature

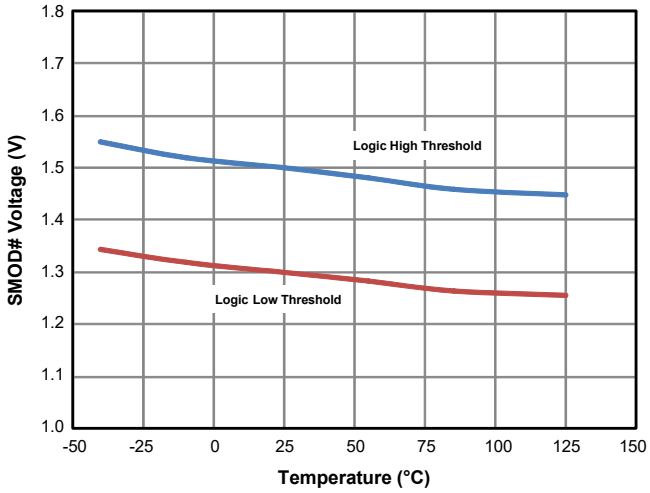


Figure 7. SMOD# Threshold vs. Temperature

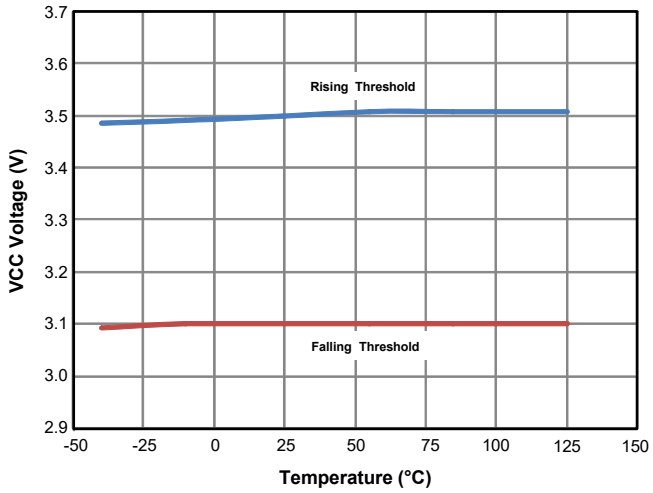


Figure 8. UVLO (VCC) Threshold vs. Temperature