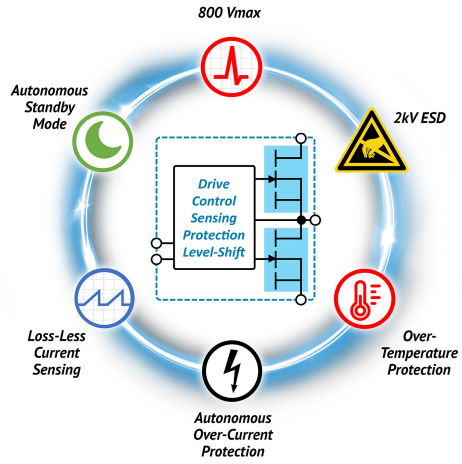
New GaNFast™ Half-Bridge Power ICs with GaNSense™ Technology

Tom Ribarich, Sr. Director Strategic Marketing



Introduction

Each NV624x GaNFast half-bridge IC with GaNSense includes two GaN FETs and drivers, plus control, level-shifting, sensing and protection features for 100-300 W applications across mobile, consumer and industrial markets. Comprehensive integration delivers high reliability, efficiency, and density and reates an easy-to-use system building block.

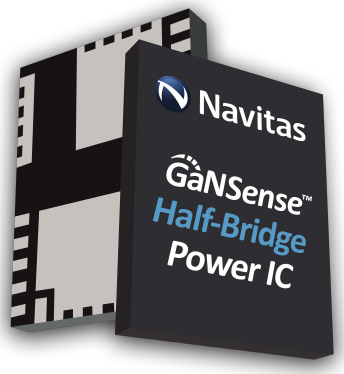
Benefits of Integration

- Reliability: No gate ringing and glitching due to monolithic integration of GaN FET and GaN driver (no parasitic gate-loop inductance). Real-time over-current (OCP) and over-temperature protection (OTP) deliver fast and reliable protection against short-circuit and overload fault conditions plus wide-range V_{CC}, 2 kV ESD protection, shoot-through protection, and UVLO are included.
- Efficiency: Loss-less current-sensing eliminates external current-sensing resistors (R_{CS}) to increase system efficiency, reduce PCB footprint and eliminate R_{CS} hot-spots. A thermally-enhanced 6x8 mm PQFN package with dual large cooling-pads enables a small PCB footprint with excellent cooling, and auto-standby mode reduces off- or sleep-state losses.
- Easy-to-use: Simple, independent, low-side-referenced PWM inputs feed an integrated level-shifter and bootstrap for isolated, high- and low-side half-bridge switching. X% fewer external components and PCB area than discrete designs, and standard QFN package enable shorter design-times and maximized chance of first-time-right.

Applications Overview

GaNFast half-bridge ICs enable high-frequency, soft-switching topologies such as active-clamp flyback (ACF), asymmetrical half-bridge (AHB), resonant LLC, totem-pole PFC (TTP) which are critical for highest efficiency, power density and system cost. Robust hard-switching performance and rich features increase switching frequency and efficiency in 3-phase motor-drive applications. Each topology has unique benefits and are selected per system requirements and desired power level, which should be well-defined, and the topology carefully selected before any design work is started.

This application note includes a detailed description of the IC features and functions, schematics and PCB layout guidelines, in-circuit examples and waveforms, and thermal management instructions. Electrical model simulation results are also included to help designers get their designs going quickly.



Power	ACF	AHB	LLC	T-P PFC	3-ph Motor
65 W	NV6245C (2x 275mΩ)				
100 W	NV6247 (2x 160mΩ)	NV6245C			
140 W		NV6247	NV6247	NV6247	
300 W					NV6247

Fig 1. GaNFast Half-Bridge IC companion topologies and power levels

Package & IC Connections

The IC integrates a complete half-bridge power-train together with level-shifting, bootstrap, two low-side GND-referenced PWM inputs, and low-side loss-less current-sensing. The IC pinout includes (see Fig. 2) high-voltage DC-bus input and high-side GaN power FET drain connection (V_{IN}), high-side GaN power FET source pad and low-side GaN power FET drain connection (V_{SW}), high-side I/O pins, low-side GaN power FET source pad (P_{GND}) and low-side I/O pins. High-side I/O pins include the high-side IC supply pins, and low-side I/O pins include PWM inputs, dV/dt turn-on control, and current-sensing output. The complementary switching currents of the external power-conversion circuit flow through the drain-to-source of both GaN power FETs. Heat generated from GaN power FETs is removed through both source cooling pads at the bottom side of QFN package to the PCB. Large PCB copper areas and thermal vias are then used to transfer the heat to the opposite side of the PCB and/or to inner layers that have large copper planes where it can then be spread and cooled. The low-side cooling pad is conveniently connected to P_{GND} to gain additional PCB thermal copper area. The low-side source pad and I/O pins are separated from the high-side source pad and I/O pins by a sufficient high-voltage creepage distance.

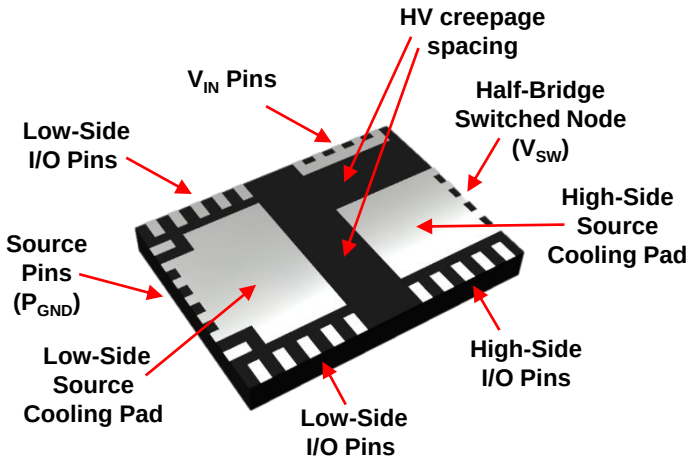


Fig 2. GaNFast half-bridge IC PQFN 6x8 package highlights (bottom view)

The typical connection diagram for this GaN Half-Bridge IC is shown in Figure 3. The IC pins include the drain of the high-side GaN power FET (V_{IN}), the half-bridge mid-point switched node (V_{SW}), the source of the low-side GaN power FET and IC GND (P_{GND}), low-side IC supply (V_{CC}), low-side gate drive supply (V_{DDL}), low-side turn-on dV/dt control (R_{DDL}), low-side 5V supply ($5V_L$), low-side referenced PWM inputs (IN_L, IN_H), low-side current sensing output (CS), auto-standby enable input ($\overline{STBY}$), high-side supply (V_B), high-side gate drive supply (V_{DDH}), and high-side 5V supply ($5V_H$). The external low-side components around the IC include V_{CC} supply capacitor (C_{VCC}) connected between V_{CC} pin and P_{GND}, V_{DDL} supply capacitor (C_{VDDL}) connected between V_{DDL} pin and P_{GND}, turn-on dV/dt set resistor (R_{DDL}) connected between V_{DDL} pin and R_{DDL} pin, current sense amplitude set resistor (R_{SET}) connected between CS pin and P_{GND}, 5V supply capacitor (C_{5VL}) connected between $5V_L$ pin and P_{GND}, and auto-standby enable pin ($\overline{STBY}$) connected to P_{GND} to enable auto-standby mode or connected to $5V_L$ to disable auto-standby mode. The external high-side components around the IC include V_B supply capacitor (C_{VB}) connected between V_B pin and V_{SW}, V_{DDH} supply capacitor (C_{VDDH}) connected between V_{DDH} pin and V_{SW}, and 5V supply capacitor (C_{5VH}) connected between $5V_H$ pin and V_{SW}. The high side V_B, $5V_H$ and V_{DDH} bypass capacitors must be chosen carefully to accommodate various system considerations such as high side wake up time, high side hold up time and standby power.

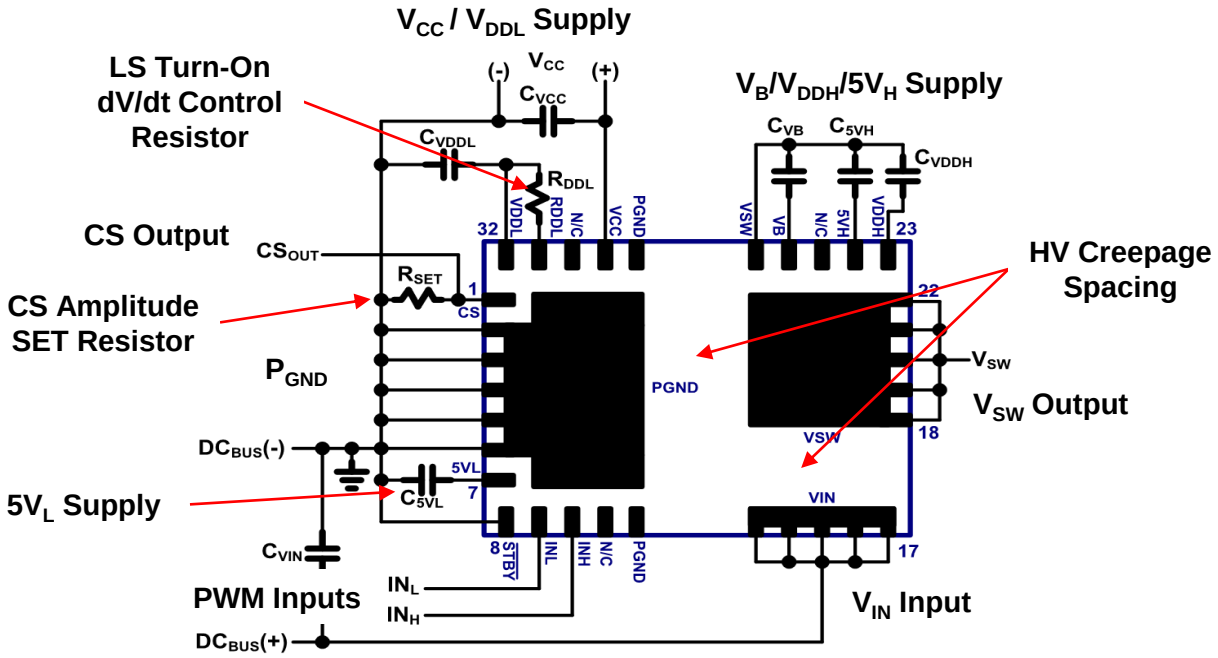


Fig 3. IC connection diagram

The following table (Table I) shows the recommended component values (typical only) for the external components connected to the pins of the IC. These components should be placed as close as possible to the IC. Please see PCB Layout Guidelines for more information.

SYM	DESCRIPTION	TYP	UNITS
C_{VCC}	V_{CC} low side IC supply capacitor	0.1	µF
C_{VDDL}	V_{DDL} low-side gate drive supply capacitor	0.01	µF
R_{DDL}	Gate drive turn-on current set resistor	50	Ω
R_{SET}	Current sense amplitude set resistor	Page 7, Equation 1	Ω
C_{5VL}	$5V_L$ supply capacitor	0.022	µF
C_{VB}	V_B high side IC supply capacitor	0.01	µF
C_{VDDH}	V_{DDH} high-side gate drive supply capacitor	0.01	µF
C_{5VH}	$5V_H$ supply capacitor	0.010	µF

Table I. Recommended component values (typical only)

Half-Bridge Daughter Card & Switching Waveforms

A multi-layer, half-bridge daughter card has been designed for bench testing purposes and to review the basic functionality and switching performance of the IC (Fig. 4). The daughtercard can be easily plugged into different application circuit motherboards, and includes the IC and all necessary external components. The external IC components have been placed and routed as close the IC as possible. Large copper planes and thermal vias have been placed on all layers at both source pads for good thermal management. See PCB layout guidelines (pages 13 & 14) for more information on proper PCB layout design.

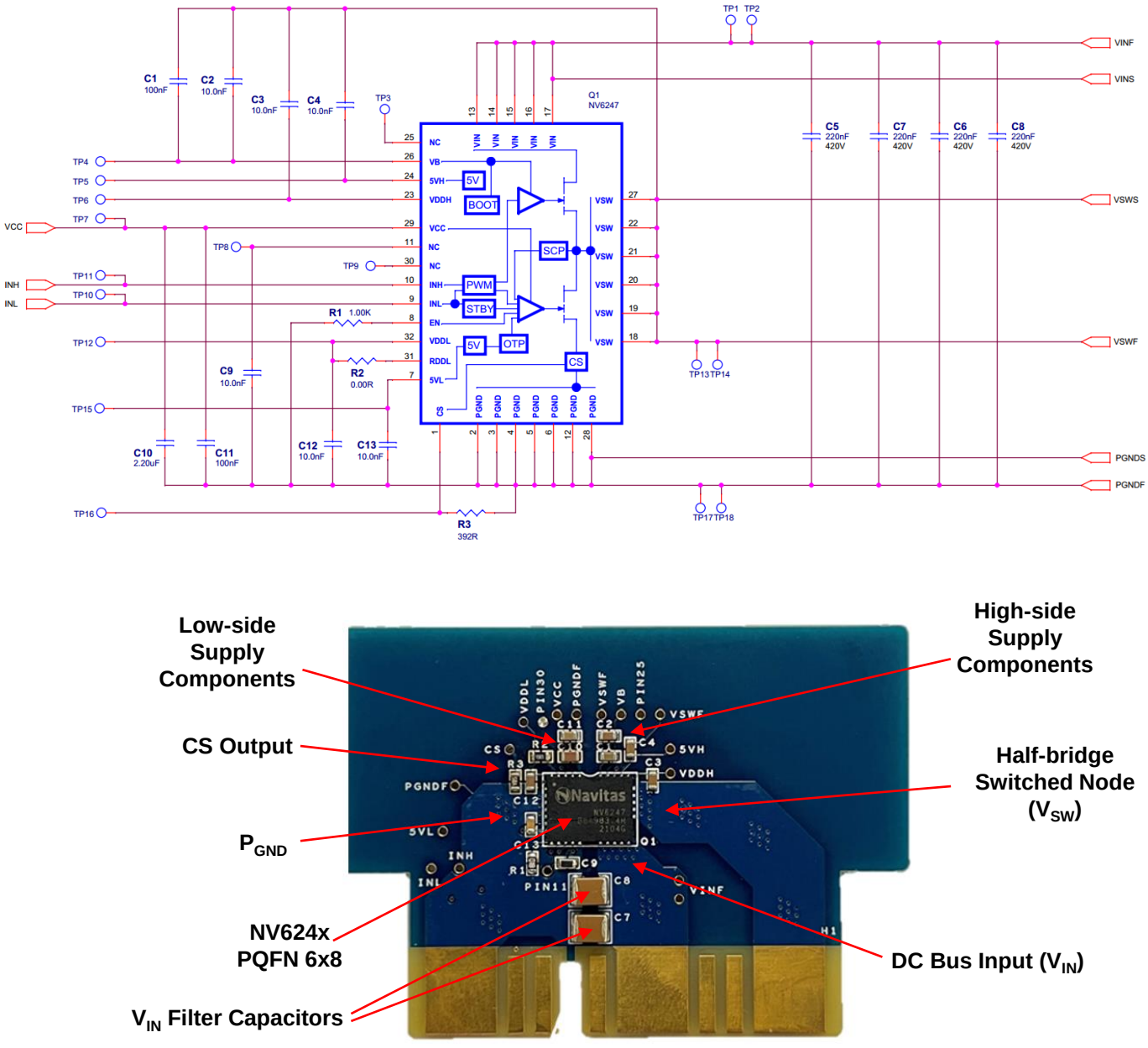


Fig 4. GaNFast Half-Bridge IC daughtercard schematics and assembled PCB

Half-Bridge Switching Waveforms (cont.)

The basic switching waveforms (Fig. 5) during resonant ZVS conditions (F_{SW} = 250 kHz, duty-cycle = 50%) include IN_L PWM input pulses, V_{SW} half-bridge switched node output, and output inductor current (I_L). The switching performance shows excellent on/off control of the integrated high- and low-side GaN power FETs. During the high-side on-time period (IN_H = high, IN_L = low), the high-side GaN power FET is turned on and the half-bridge switched node (V_{SW}) is held at the V_{IN} voltage level (DC bus voltage, 400 V). The output-inductor current ramps up to a positive peak level determined by one-half of the DC bus voltage level (+200 V), the inductor value, and the high-side GaN power FET on-time duration. When the high-side on-time period ends (IN_H = low, IN_L = low) the high-side GaN power FET turns off. During a short dead-time period, the inductor current slews the half-bridge switched-node down to P_{GND} at a dV/dt rate determined by the positive peak inductor current value and the output capacitance of the GaN power FETs. At the end of the dead-time period, IN_L then turns on (IN_H = low, IN_L = high) and the low-side GaN Power FET turns on and holds the half-bridge switched node (V_{SW}) at P_{GND}. The inductor current ramps down to a negative peak level determined by negative one-half of the DC bus voltage level (-200 V), the inductor value, and the low-side GaN power FET on-time duration. When the low-side on-time period ends (IN_H = low, IN_L = low) the low-side GaN power FET turns off. During another short dead-time period, the inductor current slews the half-bridge switched node up to the V_{IN} voltage level (400 V) at a dV/dt rate determined by the negative valley of the inductor current and the output capacitance of the GaN power FETs. The switching cycle then repeats and ZVS switching conditions are maintained each rising and falling edge of the half-bridge switched node (V_{SW}).

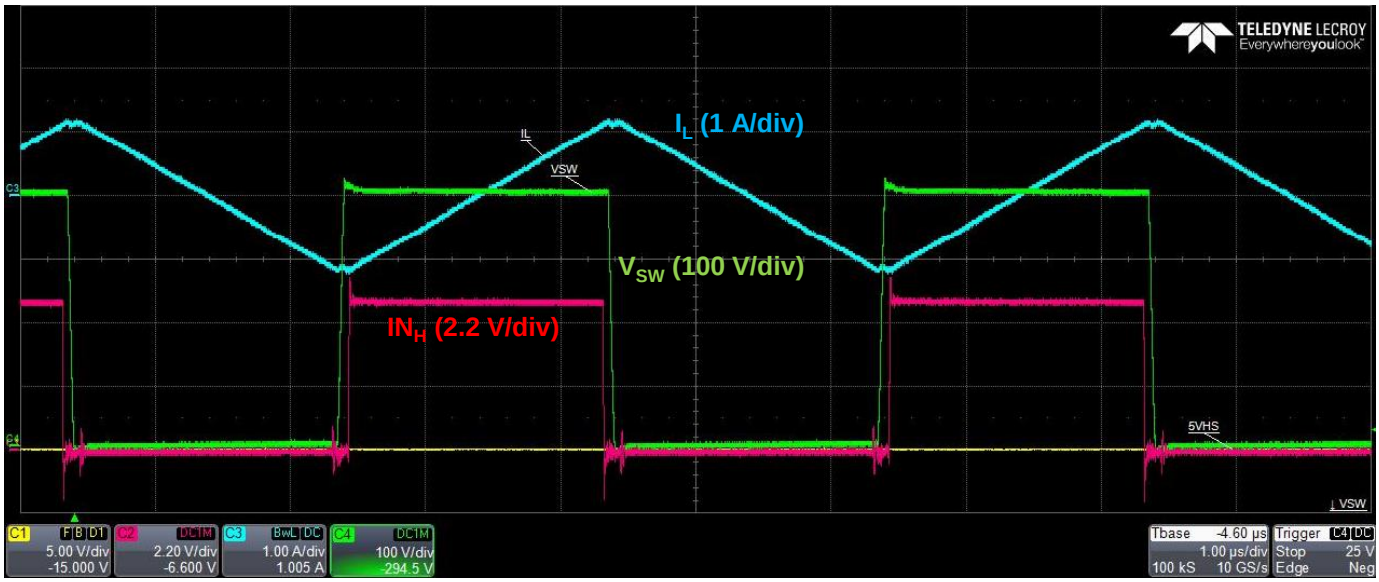


Fig 5. GaNFast Half-Bridge IC basic switching waveforms
(resonant ZVS mode, duty-cycle = 50%, F_{SW} = 250 kHz)

Loss-Less Current-Sensing

For many applications it is necessary to sense the cycle-by-cycle current flowing through the low-side GaN power FET. Existing current-sensing solutions include placing an external current-sensing resistor in between the source connection of the low-side power FET and P_{GND}. Using external current-sensing resistors increases system conduction power losses, creates a hot-spot on the PCB, and lowers overall system efficiency. To eliminate external resistors and hot-spot, and increase system efficiency, the IC integrates accurate and programmable loss-less current-sensing. The I_{DS} current flowing through the low-side GaN power FET is sensed internally (Fig. 6) and then amplified, trimmed and converted to a current at the current-sensing output pin (CS). An external resistor (R_{SET}) is connected from the CS pin to the P_{GND} pin and is used to set the amplitude of the CS pin voltage signal. This allows for the CS pin signal to be programmed to work with different controllers with different current-sensing input thresholds.

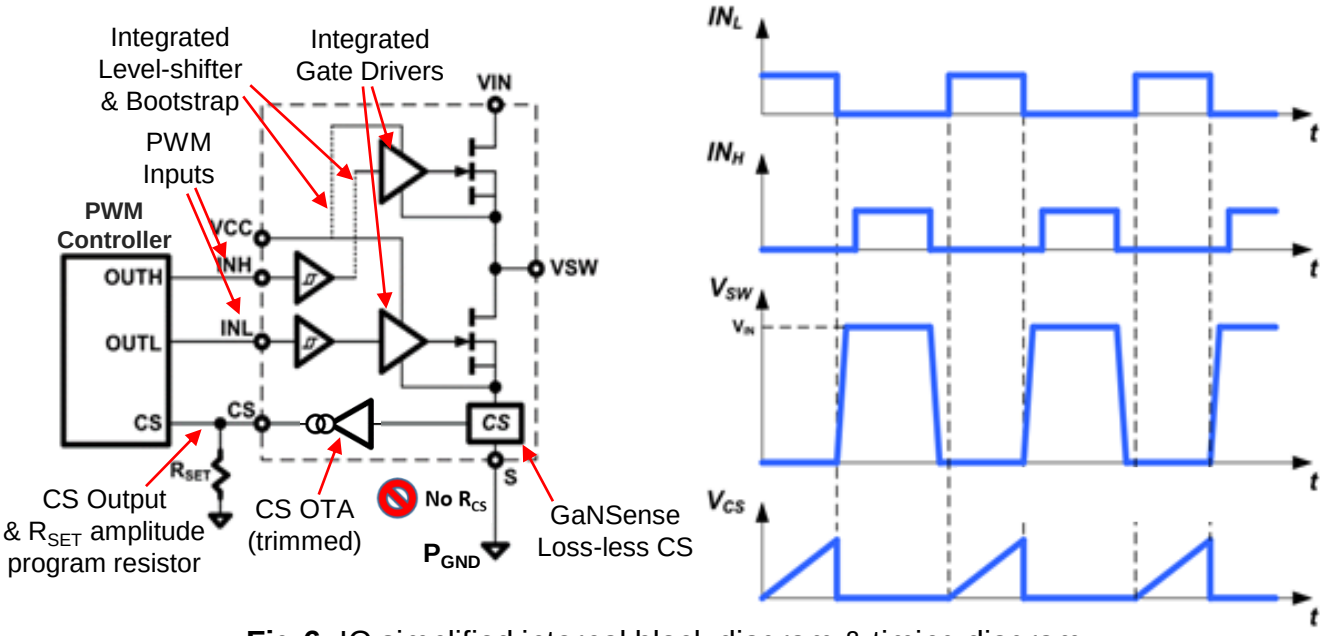


Fig 6. IC simplified internal block diagram & timing diagram

Due to careful design of internal current-sensing and amplifier circuits, plus accurate test and trim in production, the accuracy of the internal current-sensing circuit is very high (Fig. 7). The CS pin current versus temperature graph illustrates the normal positive temperature coefficient behavior of the internal circuit, with a +/- 4% tolerance from -40 to 125°C.

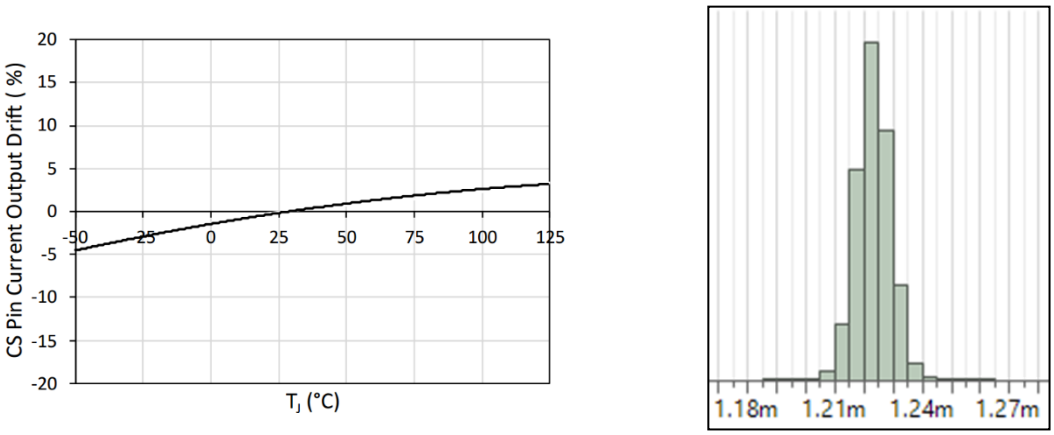


Fig 7. CS pin current vs T_{CASE} and post-trim production data (typical only)

Loss-Less Current Sensing (cont.)

When comparing GaNSense technology versus existing external current sensing resistor method (Fig. 8), the total ON-resistance, $R_{ON(TOT)}$, can be substantially reduced. For a 65 W, high-frequency ACF circuit, for example, $R_{ON(TOT)}$ is reduced from 320 mΩ to 160 mΩ. The power loss savings by eliminating the external resistor results in a +0.5% efficiency benefit for the overall system.

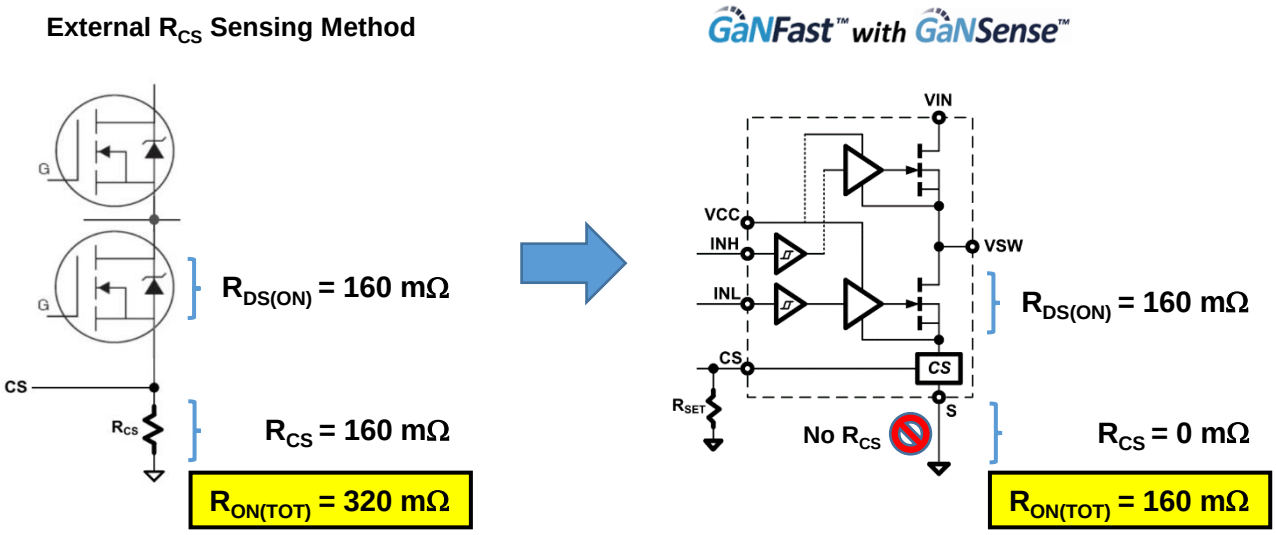


Fig 8. External resistor-sensing vs. GaNSense loss-less current sensing

To select the correct R_{SET} resistor value, the following equation (Equation 1) can be used. This equation uses the equivalent desired external current-sensing resistor value (R_{CS}), together with the gain of the internal sensing circuitry. This R_{SET} value will then give the correct voltage level at the CS pin to be compatible with the internal current sensing threshold of the system controller.

$$I_{OUT}\ Ratio = \frac{I_{DS}}{I_{CS}} = \frac{5A}{0.00125A} = 4000$$

$$R_{SET} = 4000 * R_{CS}$$

Equation 1. R_{SET} resistor value equation

Loss-Less Current-Sensing (cont.)

During bench testing, the switching waveforms (Fig. 9) show the CS pin tracking performance versus inductor current (I_L). The switching performance shows excellent V_{CS} and I_L real-time matching and tracking at 1 A peak current levels for 120 W asymmetrical half-bridge (AHB) application circuit during steady-state, full-load ZVS conditions. To show tracking accuracy, the CS pin voltage scale for all waveforms is based on R_{CS} gain calculation to match current probe scale.

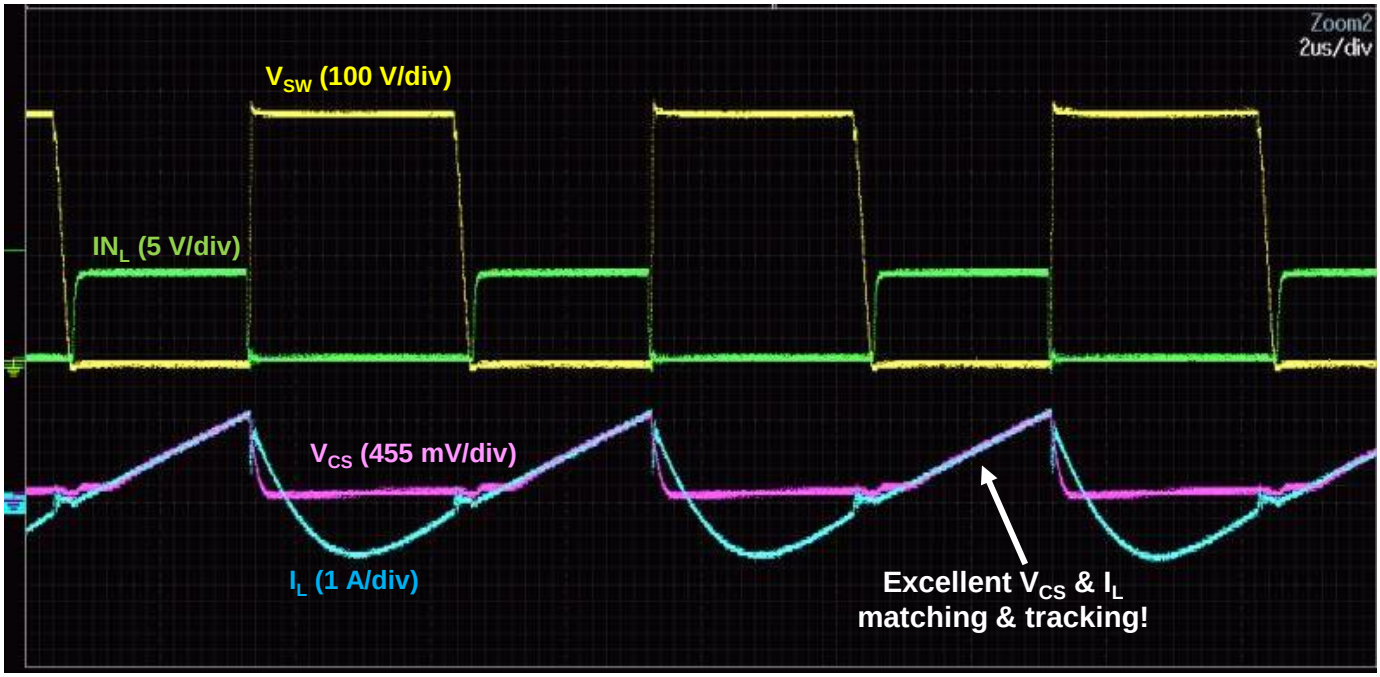


Fig 9. Loss-less current-sensing waveforms
(Asymmetrical half-bridge circuit, P_{OUT} = 120 W)

Over-Current Protection (OCP)

The IC includes cycle-by-cycle over-current detection and protection (OCP) circuitry to protect the low-side GaN power FET against high current levels. During the on-time of each low-side switching cycle (IN_H = low, IN_L = high), should the peak current exceed the internal OCP threshold (1.9 V, typical), then the internal low-side gate drive will turn the low-side GaN power FET off quickly and truncate the low-side on-time period to prevent damage from occurring to the IC. The IC will continue to function normally, and the high-side GaN power FET will then turn on at the next rising edge of the IN_H input pulse (Fig. 10) for the duration of the high-side on-time. After the high-side on-time period has ended, the low-side GaN power FET will turn on again at the rising edge of the next IN_L input pulse. Should the peak current exceed the OCP threshold again during the low-side on-time period, the OCP circuit will truncate the low-side on-time again. This cycle-by-cycle OCP protection feature will self-protect the IC each low-side switching period against fast peak over current events and greatly increase the robustness and reliability of the system. The OCP threshold equation (Equation 2) is a function of the internal current-sensing ratio and the external R_{SET} resistor and can be used to program the desired OCP current limit level (I_{OCP}). The internal OCP threshold (1.9 V, typical) is much higher than OCP thresholds of many popular PWM controllers. This ensures good compatibility of this IC with existing controllers without OCP threshold conflicts.

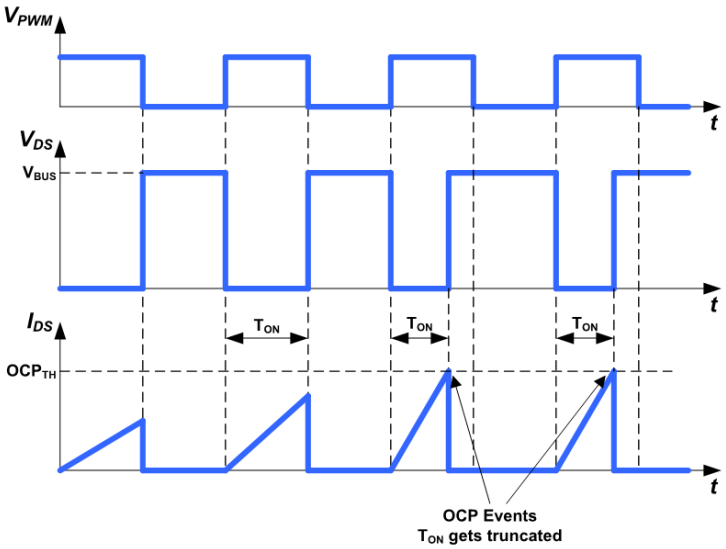


Fig 10. OCP timing diagram

$$I_{OCP} = \frac{[\,1.9\ \mathrm{V} \times 4000\,]}{R_{SET}}$$

Equation 2. OCP current limit threshold vs R_{SET}

Over-Temperature Protection (OTP)

The IC includes over-temperature detection and protection (OTP) circuitry to protect the IC against excessively high junction temperatures (T_J). High junction temperatures can occur due to overload, high ambient temperatures, and/or poor thermal management. Should T_J exceed the internal T_{OTP+} threshold (165℃, typical) then the IC will latch off safely (Fig. 11). When T_J decreases again and falls below the internal T_{OTP-} threshold (105℃, typical), then the OTP latch will be reset. Until then, internal OTP latch is guaranteed to remain in the correct state while V_{CC} is greater than 5 V. During an OTP event, the IC will latch off and the system V_{CC} supply voltage can decrease due to the loss of the aux winding supply. The system V_{CC} will fall below the lower UV- threshold of the system controller and the system high-voltage start-up circuit will turn-on and V_{CC} will increase again (Fig. 10). V_{CC} will increase above the rising UV+ threshold and the controller will turn on and deliver PWM pulses again, but the IC will remain off until T_J has decreased below T_{OTP-} and the OTP fault latch is reset. Once the fault latch is reset, the IC will start switching again at the next PWM pulses from the controller.

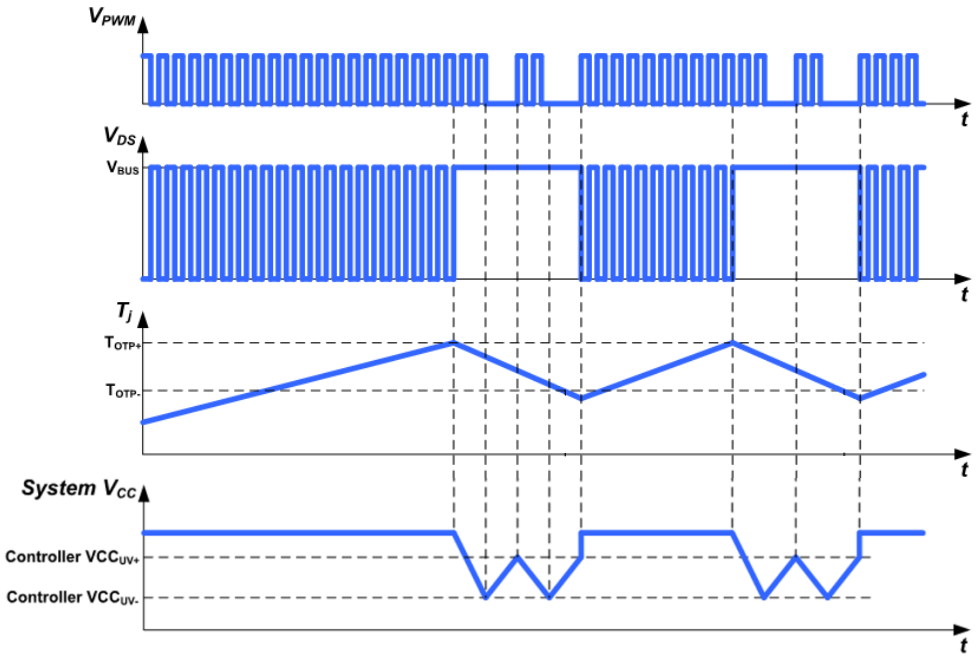


Fig 11. OTP timing diagram

Programmable Turn-on dV/dt Control

During first start-up pulses or during hard-switching conditions, it is desirable to limit the slew rate (dV/dt) of the drain of the low-side GaN power FET during turn-on. This is necessary to reduce EMI or reduce circuit switching noise. To program the turn-on dV/dt rate of the low-side GaN power FET, a resistor (R_{DDL}) is placed between the V_{DDL} pin 32 and the R_{DDL} pin 31 (see Fig. 3). This resistor (R_{DDL}) sets the turn-on current of the internal gate driver and therefore sets the turn-on falling edge dV/dt rate of the drain of the low-side GaN power FET (Fig. 12). The actual low-side V_{DS} turn-on dV/dt rates versus different R_{DDL} resistor values are also shown (Fig. 13).

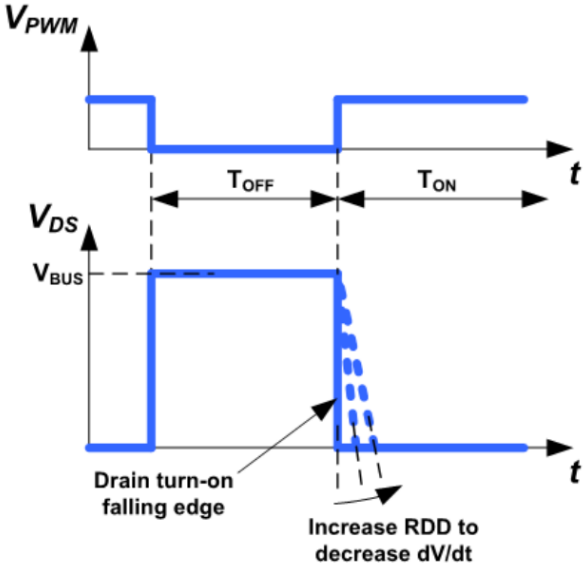


Fig 12. Turn-on dV/dt slew rate control simplified timing diagram

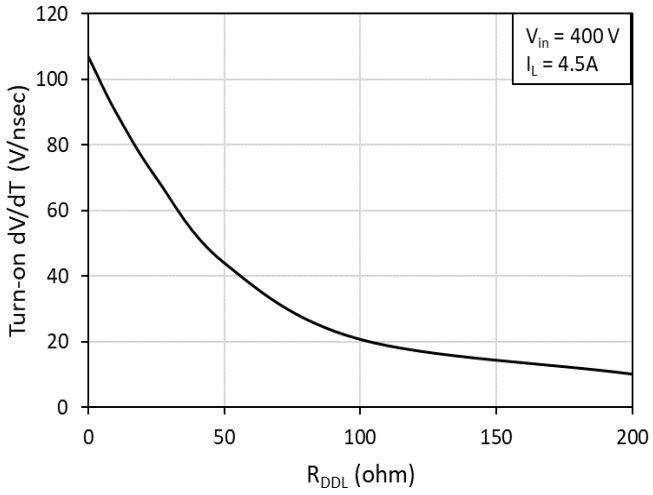


Fig 13. Low-side V_{DS} turn-on slew rate (dV/dt) vs R_{DDL} curve

Autonomous Low-Power Standby Mode

The IC includes an autonomous low-power standby mode for disabling the IC and reducing the V_{CC} current consumption. During normal operating mode, the PWM input signals at the IN_L and IN_H pins turn the gates of the internal high- and low-side GaN power FETs on and off at the desired duty-cycle, frequency, and dead-time. If the input pulses at the IN_L pin stop and stay below the lower V_{INL-} turn-off threshold (1.1 V, typical) for the duration of the internal timeout standby delay (t_{TO_STBY}, 90 us, typical), then the IC will automatically enter low-power standby mode (Fig. 14). This will disable the gate drive and other internal circuitry and reduce the V_{CC} supply current to a low level (265 uA, typical). When the IN_L pulses restart, the IC will wake up after a delay (typically around 450 ns) at the first rising edge of the IN_L input and enter normal operating mode again. To enable auto standby mode, the $\overline{STBY}$ pin 8 should be connected to source (set low). To disable auto standby mode, $\overline{STBY}$ pin should be connected to the $5V_L$ pin 7 (set high).

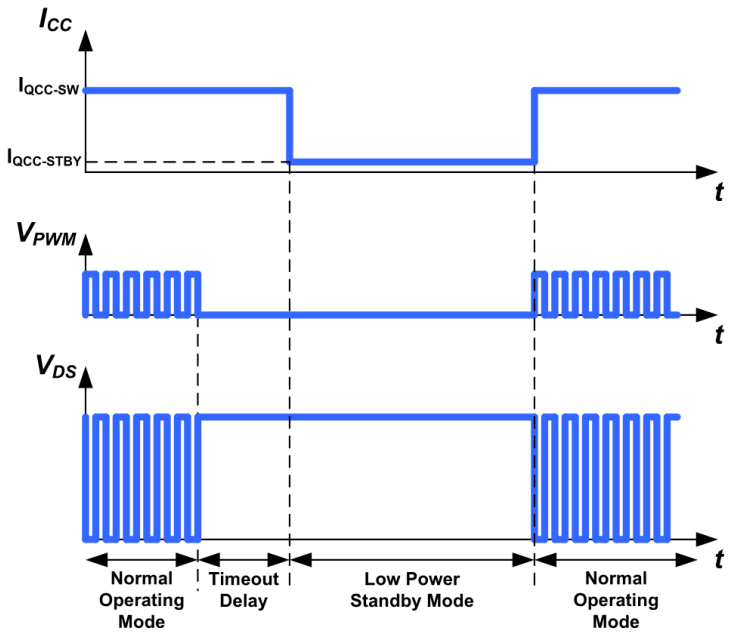
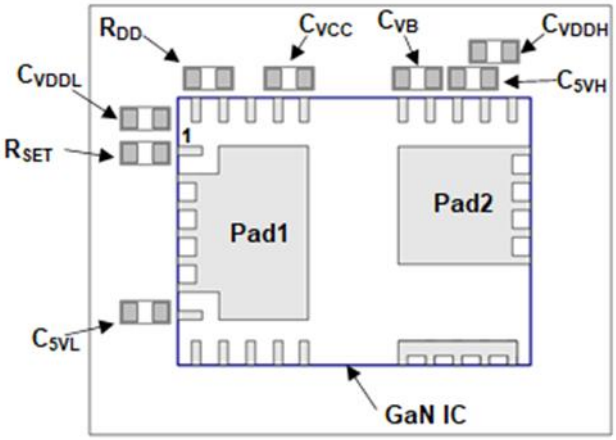


Fig 14. Autonomous low-power standby mode timing diagram

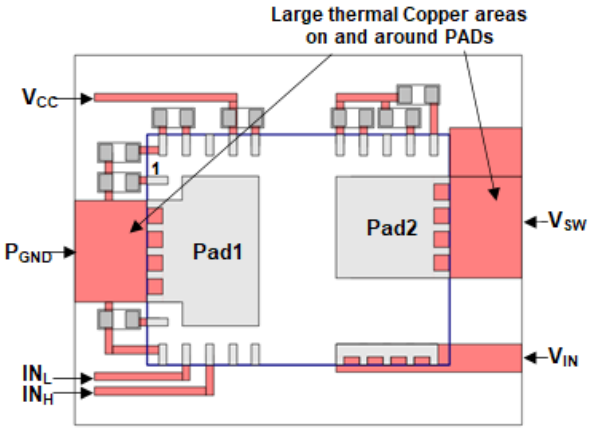
PCB Layout Guidelines (PQFN 6x8 mm)

For best electrical and thermal results, these PCB layout guidelines (and 4 steps below) must be followed:

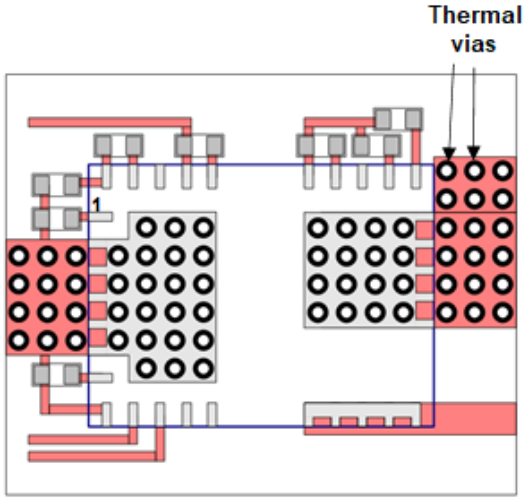
1) Place IC-related components as close as possible to the GaN IC. Place R_{SET} resistor directly next to CS pin to minimize high frequency switching noise.
2) Connect the ground of IC components to Source to minimize high frequency switching noise. Connect controller ground also to Source (P_{GND}).
3) Route all connections on single layer. This allows for large thermal copper areas on other layers.
4) Place large copper areas on and around Pad1 and Pad2.
5) Place many thermal vias inside Pad1 and Pad2 and inside Pad1 and Pad2 copper areas.
6) Place large possible copper areas on all other PCB layers (bottom, top, mid1, mid2).



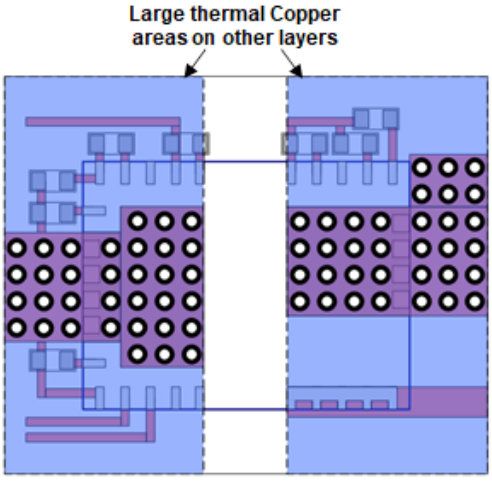
Step 1. Place GaN IC and components on PCB. Place components as close as possible to IC



Step 2. Route all connections on single layer. Make large copper areas on and around Source pad



Step 3. Place many thermal vias inside source pad and inside source copper areas.
(dia=0.65mm, hole=0.33mm, pitch=0.925mm, via wall=1mil)



Step 4. Place large copper areas on other layers. Make all thermal copper areas as large as possible!

Fig 15. PCB layout steps

NV6247 and NV6245C PCB Footprint Compatibility

The NV6247 and NV6245C have a slight difference in pin-out, as shown in Fig. 16. The NV6245C includes an additional R_{DDH} pin (pin 23) and additional R_{DDH} resistor placed between pins V_{DDH} and R_{DDH} (for programmable high-side turn-on dV/dt control). For compatibility, a dual-PCB can be designed, with an example shown in Fig. 17, and the high-side pinout differences and high-side component placement instructions for pins 23-27 are summarized in Table II.

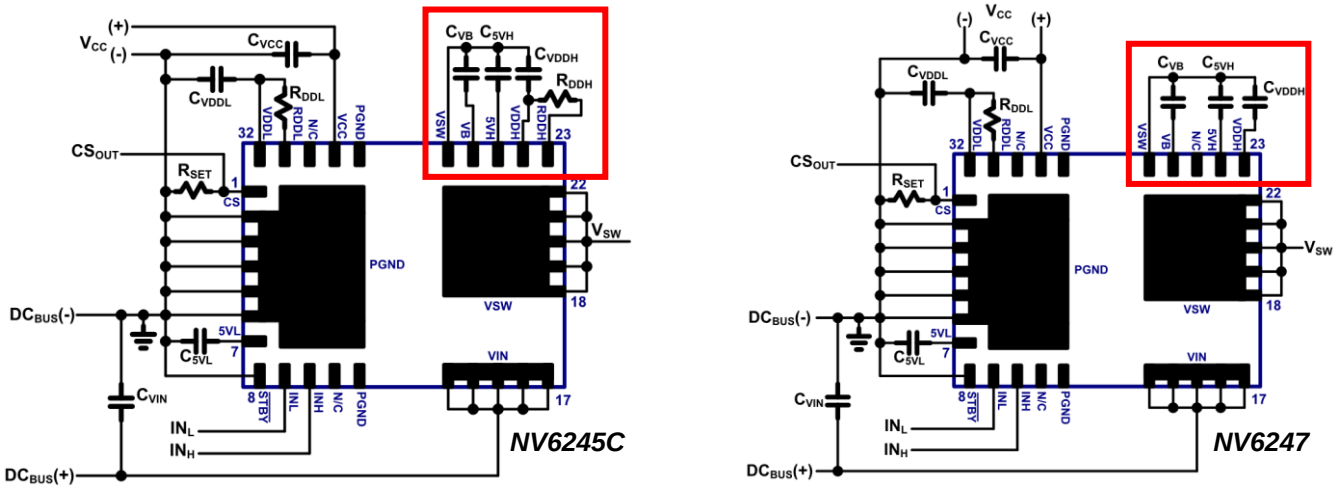


Fig 16. NV6245C and NV6247 IC connection diagrams

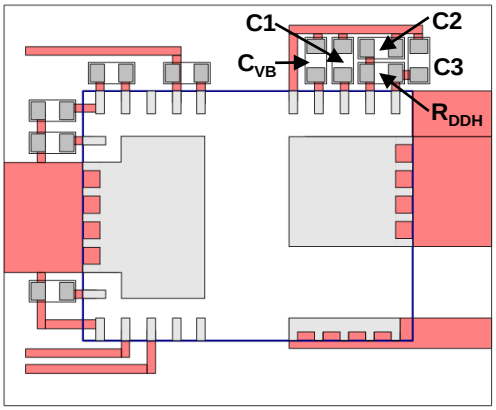


Fig 17. NV6245C and NV6247 dual-PCB footprint layout

Pin#	NV6245C Pin Name	NV6247 Pin Name	NV6245C Component	NV6247 Component
23	R_{DDH}	V_{DDH}	C3 = do not place	C3 = C_{VDDH}
24	V_{DDH}	$5V_H$	R_{DDH} = place, C2 = C_{VDDH}	R_{DDH} = do not place
25	$5V_H$	N/C	C1 = C_{5VH}	C1 = do not place, C2 = C_{5VH}
26	V_B	V_B	C_{VB}	C_{VB}
27	V_{SW}	V_{SW}	GND connection for C_{VB}, C_{5VH}, C_{VDDH}	GND connection for C_{VB}, C_{5VH}, C_{VDDH}

Table II. NV6245C and NV6247 pinout differences and component-placement instructions

Electrical-Simulation Model

PSPICE-based electrical simulation models have been developed for the NV624x product family. This models are compatible with SiMetrix, LTSPICE and PSPICE platforms and include all internal circuitry and logic, current-sensing, level-shifting and both high- and low-side GaN power FETs. A typical LTSPICE simulation circuit and steady-state waveforms are shown for a ZVS resonant application circuit (Fig. 18). Both PWM inputs (IN_H and IN_L) are shown together with the half-bridge switched node (V_{SW}) and output resonant inductor current (I_L).

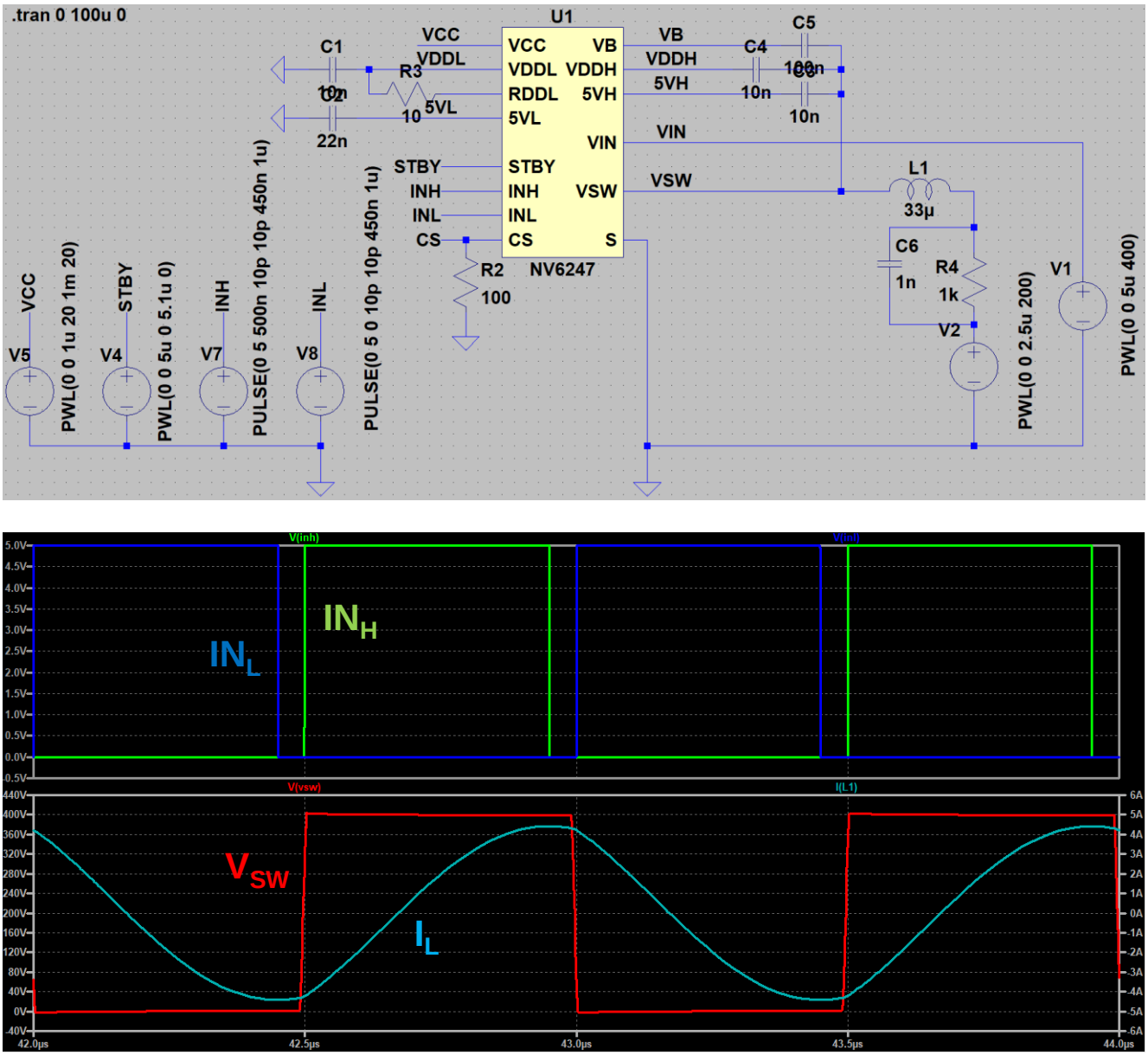


Fig 18. Electrical-simulation model & ZVS resonant circuit and simulation waveforms

3D Mechanical Model

A 3D mechanical model has been developed for this IC (Fig. 19). The NV6247.stp file is available and easily importable into many popular PCB design software platforms (such as Altium Designer). This model is useful for generating 3D renderings of assembled power supply designs to check for any design issues before releasing PCB gerber files for manufacturing.

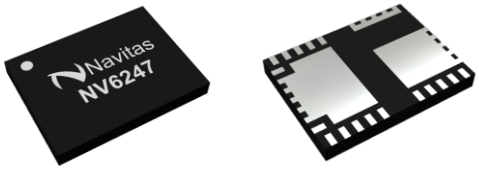


Fig 19. Top & bottom views of 3D mechanical model of NV624x (.stp file)

Thermal Management

The following thermal model (Fig. 20) is for a PCB daughtercard with the IC mounted on one side of the PCB. The heat from the IC flows through the package leadframe, to the PCB copper layers and thermal vias, through the thermal interface material (TIM) and laterally through the PCB to the sides. The TIM then goes to the safety insulating material (Mylar) and then to a Cu shield (used for heatsinking and EMI suppression). The thermal conductivity for these materials are listed in Table III. To represent the actual thermal conditions inside a 140 W charger running at full load, the Cu shield is held at 85°C, the T_{AMB} is set at 80°C, and P_{LOSS} for both GaN power FETs is set at 1 W total. From the thermal simulation (Fig. 21), the T_J of the high-side GaN FET = 97.5°C and Tj of the low-side GaN FET = 97.2°C. This result looks reasonable for the IC running during worst case line, load and ambient temperature conditions. Further improvement of the IC temperature is possible by using TIM with higher conductivity and by using thinner Mylar (if safety conditions allow).

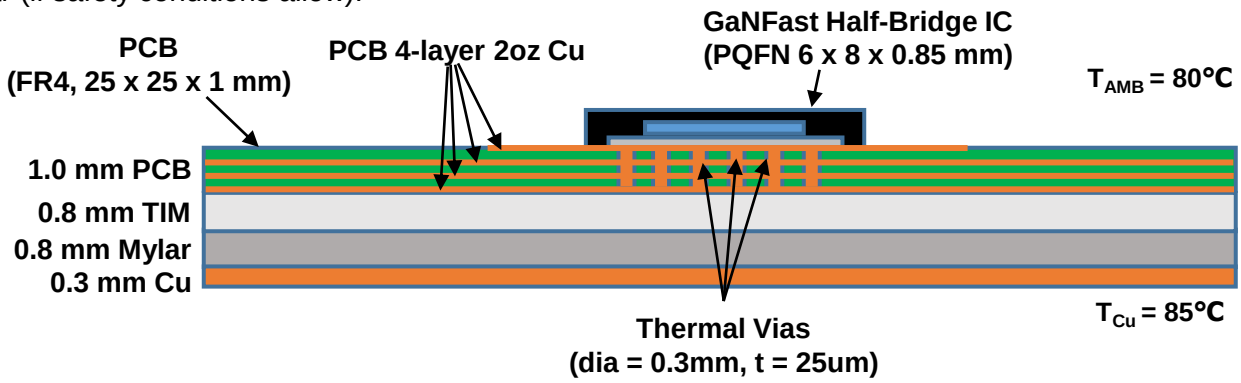


Fig 20. Bottom-cooled thermal-model stack-up diagram

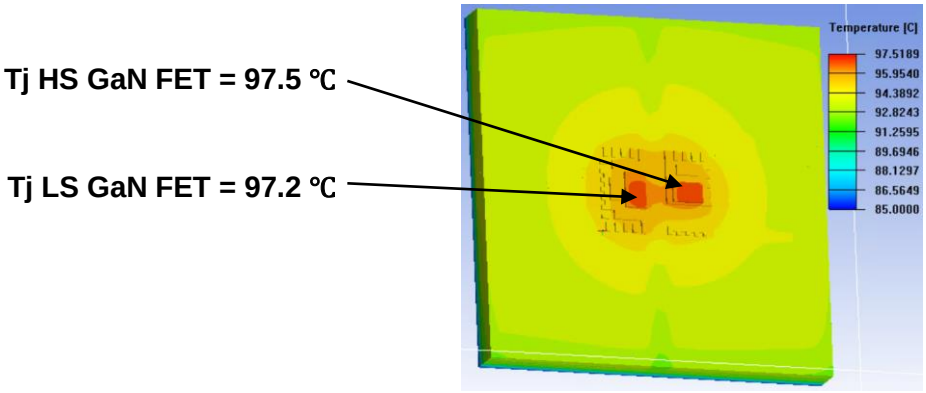


Fig 21. 3D thermal simulation results
($P_{LOSS\_HS\ GaN\ +\ LS\ GaN}$ = 1 W, T_{AMB} = 80°C)

Thermal Management (cont.)

Materials commonly used for shielding include copper or aluminum. Steel can be also be used for improved EMI shielding and is typically tin-plated to prevent rusting or corrosion. Some available thermal stack-up and shielding materials are summarized in the table below (Table III).

Thermal Interface (TIM)			
MATERIAL	MANUFACTURER	PART NUMBER	THERMAL CONDUCTIVITY
Thermal Pad	PMP	PMP-P-300	4.0 W/mK
Safety Isolation Material			
MATERIAL	MANUFACTURER	PART NUMBER	THERMAL CONDUCTIVITY
Mylar	Formex	PC-ITW N3-8	0.14 W/mK
Metal Shielding			
MATERIAL	MANUFACTURER	PART NUMBER	THERMAL CONDUCTIVITY
Copper	Various	Various	399 W/mK
Aluminum	Various	Various	235 W/mK
Steel	Various	Various	14 W/mK
Plastic Case			
MATERIAL	MANUFACTURER	PART NUMBER	THERMAL CONDUCTIVITY
Polycarbonate Resin	Sabic Plastics	PC Sabic 945	0.20 W/mK

Table III. Thermal stack-up and shielding-materials summary.

References (www.navitassemi.com)

1) GaNFast NV6247 datasheet, Navitas Semiconductor, 2022
2) New GaNFast Power ICs with GaNSense Technology Loss-Less Current Sensing & Autonomous Protection, AN015, Navitas Semiconductor, 2021
3) Thermal Management of GaNFast Power ICs, AN010, Navitas Semiconductor, 2019

Revision History

Date	Status	Notes
Aug 22	Released	

Additional Information

Contact: info@navitassemi.com