Advanced Power Modules for Telecom Applications

De-regulation and competition in wireline and wireless infrastructure telecommunications systems has accelerated the need for lower cost equipment solutions with ever-increasing bandwidth. Increasingly, designers are asked to provide more voltage rails for a variety of digital signal processors (DSP), field programmable gate array (FPGA), application Specific integrated circuit (ASIC) and microprocessors. In short, they are required to generate more voltages, at higher currents, more efficiently, with less noise, in a smaller space. And, if that wasn't challenge enough, the solution has to cost less, too! This article provides a brief understanding of the evolution of board-mounted power systems, and how the latest generation can achieve higher performance and lower cost – in a smaller footprint. **Brian Narveson and Adrian Harris, Texas Instruments Inc., USA**

Deploying access equipment closer to the subscriber requires smaller enclosures (pad and pole mounting) that must survive in a tougher environment. Infrastructure equipment is being designed for smaller footprints as central office space comes at a premium. Driving power management factors are size, thermal management, cost and electrical performance (regulation, transient response and noise generation).

Addressing various issues

The need to address size, efficiency and cost simultaneously has ignited a need to take another look at power architectures. The first generation of board-mounted power used a power architecture known as a distributed power architecture (DPA) (see Figure 1). This architecture used an isolated (brick) power module for every voltage rail. It worked well when there were limited rails, but cost and printed circuit board space increased significantly with each added voltage rail. Sequencing of the voltage rails was also difficult and required adding external circuitry which, in turn, added cost and board space.

To deal with the size and cost constraints of DPA, second generation systems moved to a fixed voltage intermediate bus architecture (IBA). An IBA (Figure 2) uses a single, isolated-brick power module and many non-isolated, point-of-load (POL) DC/DC converters. The POLs can be either power modules, such as TI PTH series, or discrete buck converters. The isolated converter works over the same input voltage range as the first generation, either 36 to 75V or 18 to 36V. It creates an intermediate bus that is regulated to 3.3, 5 or 12V. The voltage choice is up to the system designer. This design results in less board space, lower cost and easier sequencing of the voltages, due to features such as Auto Track. The only drawback of this architecture is reduced efficiency due to the double conversion required for each voltage.

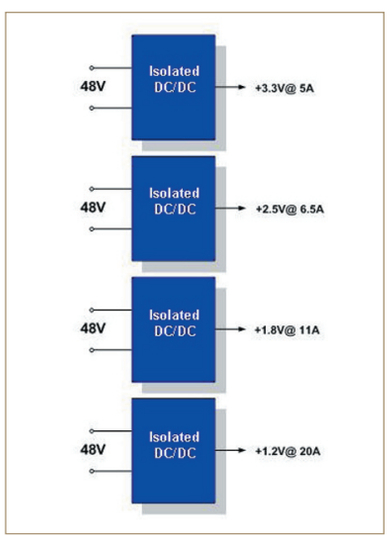
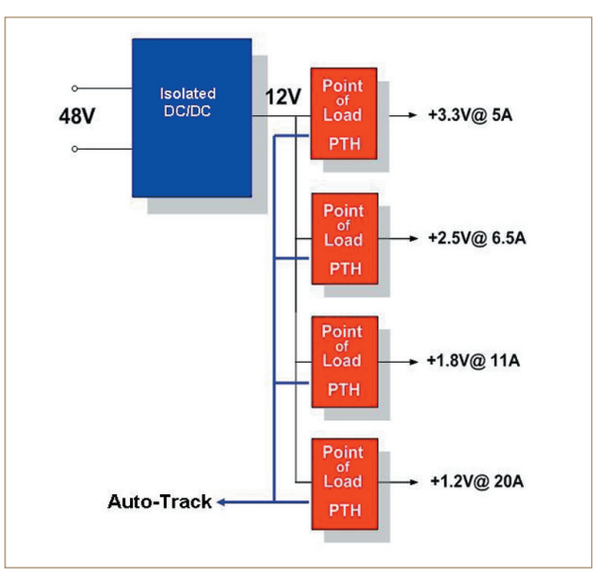


Figure 1: Typical DPA architecture

Today, most telecom systems use a fixed-voltage IBA. But, as small pad and pole-mounted access equipment designs evolve to sealed enclosures, with no forced

Figure 2: Fixed voltage IBA



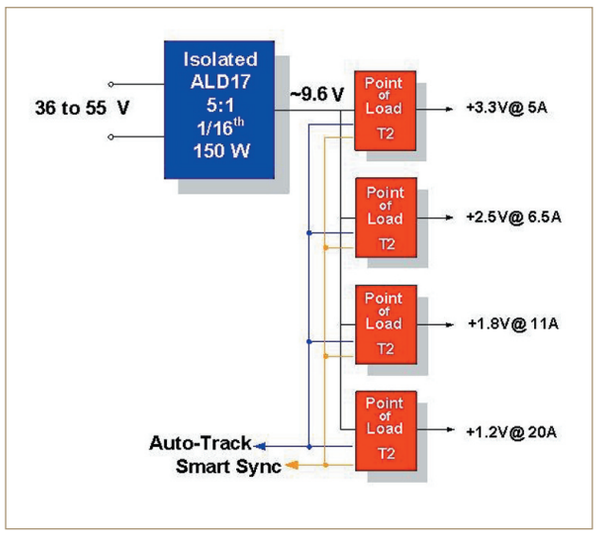


Figure 3: Unregulated IBA

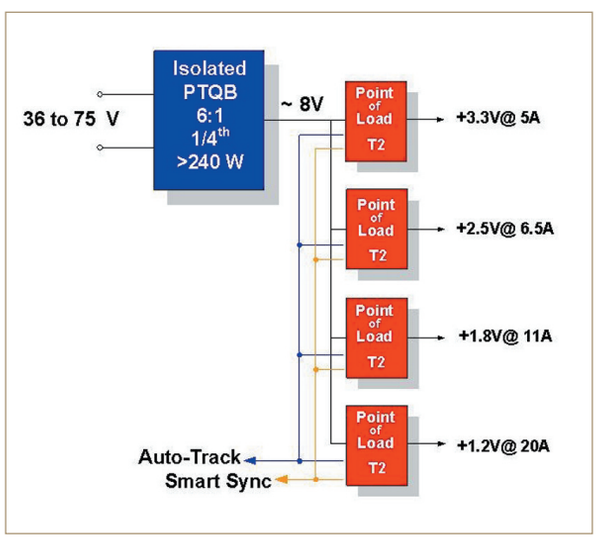


Figure 4: Quasi-regulated IBA

air cooling, it creates a need for a higher efficiency and smaller footprint solution. As every designer knows, the best way to get rid of heat in a system is not to create it. Since all of the power goes through the front-end isolated converter, it is the main focus when looking for efficiency improvement. The proven way to increase isolated converter efficiency is to run it at a fixed duty cycle and not regulate the output. That led to the unregulated intermediate bus architecture (Figure 3).

This architecture uses an unregulated bus converter where the output voltage is a ratio of the input voltage. In the example, an ALD17 5:1 converter creates an output voltage that is one-fifth of the input. This technique creates a design where a 150W system/board now can be designed with a one-sixteenth brick and achieve 96% efficiency for the first conversion stage. Unregulated voltage buses became possible when wide input (4.5 to 14V) PWMs and power modules such as TI's T2 products were introduced. This architecture is limited by the maximum input range of the bus converters, which is 36 to 55V. This is necessary to keep the input voltage to POLs less that 12V. The 12V maximum is necessary because for POLs to generate 1V or less output voltages, the input voltage cannot exceed 10 to 12 times the output. However, an increasing number of telecom OEMs are considering a move to this limited input range. That is due to the significant cost savings, size reduction and efficiency improvements obtained with this architecture.

Some telecom OEMs insist on maintaining the traditional wider input voltage specification of 36 to 75V with input transients to 100V. For these requirements, the power industry has responded with the quasi-regulated IBA (Figure 4). The main difference from this and the unregulated IBA is that if the input voltage exceeds 55 to 60V, the output voltage is regulated to around 10V. The drawback of this approach is that the isolated power module must increase in size to accommodate the regulation circuitry, and its efficiency is reduced above 55V. An example of this kind of product is the TI PTQB series.

To provide a meaningful comparison, the example in each figure has identical voltage and current requirements. It is based on a theoretical networking card utilising multiple high performance DSPs with associated analog and digital circuits. The output voltages are 3.3V at 5A, 2.5V at 6.5A, 1.8V at 11A and 1.2V at 20A. For a comparison of the architectures described above, see Figure 5. The graphs indicate that the ultimate dream is, indeed, possible. A quasi-regulated or unregulated power system can provide higher efficiency, in less space – and at lower cost. The most notable improvement from the second generation fixed-IBA to the quasi/unregulated-IBA is efficiency. As shown in Figure 5, power conversion efficiency increased almost 7%. This translates to a thermal load reduction of 14W for a 200W system.

We used power modules in these examples because they provide the greatest power density, and are the solution of choice at many telecom OEMs (pricing for POLs is based on 1K distributor quantities). OEM pricing would be less. Discrete POLs can be used in all systems, but the board space increases by at a factor of 2, although cost is reduced.

Electrical performance

The remaining challenge for the designer is to meet the increasing electrical demands at the heart of each system – high performance DSPs and ASICs. Primary performance issues are voltage regulation, current transient response and noise.

Regulation and current transient response are closely linked. In order to get higher performance, with lower power in a smaller size, digital semiconductors are fabricated with smaller geometry transistors that require ever decreasing voltages. Sub-1V core voltage requirements are now becoming the standard. Along with this low voltage have come increasingly tighter tolerances. It is now common practice to specify a total voltage tolerance of 3% including line (variations in input voltage), load (small deviation in load current), time, temperature and current transients. This leaves the power designer with only 30mV of head room to accommodate everything the digital world throw at him. About half of the tolerance budget (15mV) is usually absorbed for the DC parameters of line, load, time and temperature. The remaining 15mV is then available to deal with sudden (1 to 3 clock cycles) changes in current due to computational or data transmissions loads.

This creates power system design challenges to minimise voltage deviation in the presence of these current transients. If the core voltage (V_{cc}) exceeds the specified tolerance limits, the digital IC may initiate a reset or have logic errors. To prevent this

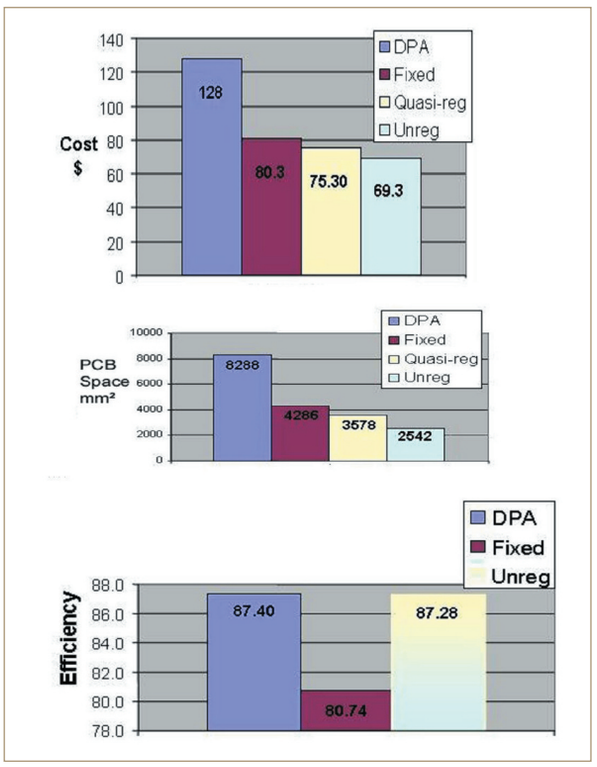


Figure 5: Comparison of architectures in terms of cost (upper), real estate (middle), and efficiency (lower)

occurrence, designers need to pay close attention to the transient performance of the POL modules being used. Digital loads, such as the latest Gigahertz DSPs, require extremely fast transient responses with very low voltage deviation. To achieve these targets, many additional output capacitors are usually added to the DC/DC converter to provide hold-up time until its feedback loop can respond. The power module, including this added capacitance to meet transient voltage tolerances, represents the complete power solution.

Capacitors have been evolving over the years, with volumetric efficiencies getting better all the time. Even with higher volumetric efficiency, the overall power solution can be over twice the size of the power module alone. This requires a large PCB allocation that is usually not available in today's physically smaller systems. What's more, the bill of material (BOM) costs of V_{CC} power can be more than double the cost of the power module when adding in the cost of capacitors.

With innovations in DC/DC power module technology, system designers are now able to achieve faster transient response and less voltage deviation using less output capacitance. An example is the T2 series next generation PTH modules (Figure 6). These devices incorporate a new feature called TurboTrans technology. This patented technology allows the designer to custom tune the module to meet a specific transient load requirement. Tuning is accomplished with a single external resistor.

TurboTrans can achieve up to an eight-times reduction in output capacitance. This feature saves the cost of capacitors and PCB space. Another benefit of this technology is enhanced stability with ultra-low equivalent series resistance (ESR) capacitors. Designers can use newer Oscon, polymer tantalums or all ceramic output capacitors without stability concerns. This allows the designer to use capacitor technologies capable of withstanding high temperature, lead-free solder profiles.

The final performance hurdle for isolated and POL converters is noise. When switching POLs run at different frequencies and share a common input bus, frequencies resulting from the sum and difference of those frequencies can create beat frequencies that make EMI filtering difficult. As an example, if a system has two POLs with one operating at 300kHz and a second at 301kHz, the beat frequency is 1kHz. This can require larger, more complex system filters. T2 power modules have a SmartSync feature that lets the designer synchronise the switching frequency of multiple T2 modules to a specific frequency. Synchronised modules eliminate beat frequencies and make EMI filtering easier. SmartSync can be used to set the frequency, so switching noise is out of a particular frequency band (i.e audio frequencies). TurboTrans and Smart Sync are standard features on T2 power modules that add no additional system cost to the systems described earlier.

Conclusion

A telecom system built with state-of-the-art power modules allows the system designer to reduce system size, decrease dissipated power, meet the power demands of high performance digital circuits and reduce the cost of power compared to regulated voltage IBA systems.

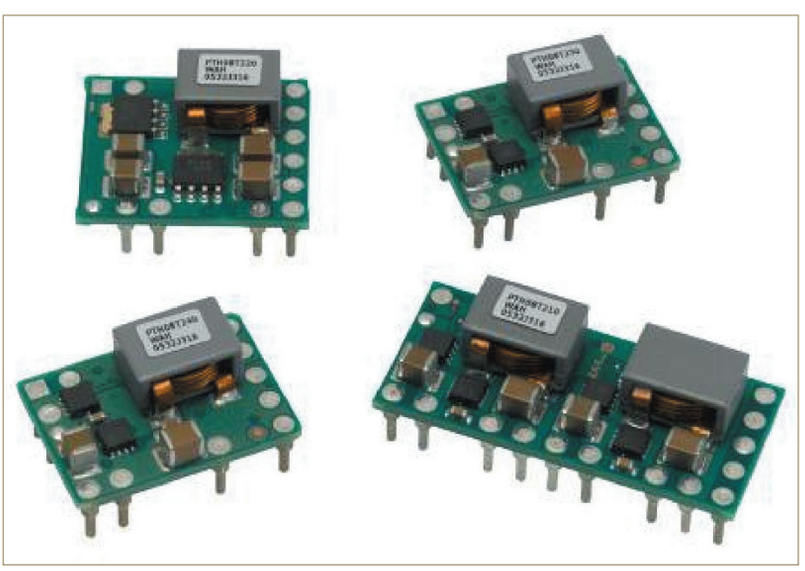


Figure 6: T2 Series Power Modules with TurboTrans