Techniques for Digital Power Conversion

High standards of performance, efficiency and power density are expected from today's digital power supplies. This article looks at practical ideas that designers can use to achieve these goals. It will show how digital signal controllers facilitate numerous digital power conversion topologies and control schemes. Pulse-width-modulation switching speeds, analogue-to-digital converter conversion rates, and analogue comparator capabilities will be discussed, and several switch-mode power supply topologies will be described. **Bill Hutchings, Microchip Technology, Chandler, Arizona, USA**

Traditional power-supply products, such as AC/DC and DC/DC switch-mode power supplies (SMPSs) have employed an analogue control loop for basic control of the pulse-width-modulation (PWM) module, integrated circuits and power devices. In these systems, additional digital control and communication, performed by a microcontroller, has been layered on top. In digital power supplies, the analogue control loop is replaced with a digital one, and the PWM module is typically integrated into the same microcontroller that is performing the high-level control and communication.

Digital loop control allows developers to realise many benefits. These are provided by the ability to perform power-conversion control via reprogrammable software, as well as the performance and features offered by digital signal controllers (DSC) solutions. Benefits can include: increased power density; faster time-to-market and ease of manufacturing; ease of adding additional features; improved reliability and greater protection of intellectual property.

Digital loop architecture

Many different power-conversion topologies can be implemented with digital loop control using modern DSC technology. Figure 1 shows a simplified example of a digital loop architecture for power conversion.

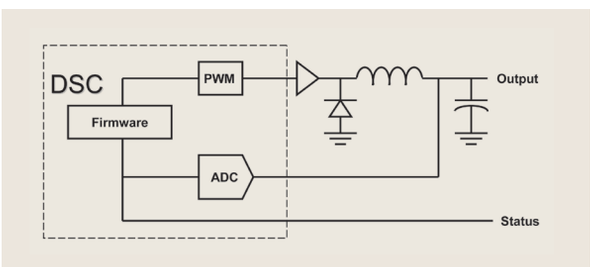

Figure 1: Example of a digital loop architecture

Everything inside the dotted line is internal to the DSC. To implement the digital loop, the analogue signals are first converted by an analogue-to-digital converter (ADC). The software running on the DSC then processes the samples to perform the voltage and current control loops necessary to control the supply. The results of these loops are then used to control the on-chip digital PWM module that directly controls the power devices. The basic digital control loop is now implemented in software, generally on the DSC in fixed-point maths. The DSC's internal architecture is a cross of both microcontroller and digital signal processor (DSP) capabilities. The DSP portion of the DSC performs the basic maths to implement the control algorithm in digital power conversion.

To achieve the goals of reliability, efficiency and power density, a DSC used for digital power conversion must be self-sufficient. This is critical because, if the digital power design implementation requires many external support chips, these three parameters will suffer.

Figure 2 shows a basic block diagram of a DSC equipped with the elements necessary for high-performance, reliable digital power conversion. The internal peripherals and features that help to reduce part count and increase power-supply reliability are: a high-speed digital PWM designed specifically for driving power-conversion bridges; a high-performance ADC that has special triggering and sample-and-hold capabilities; onboard analogue comparators to provide specific high-speed control algorithms, such as those for current limiting; a power-management subsystem to provide brownout reset, power-on reset and the

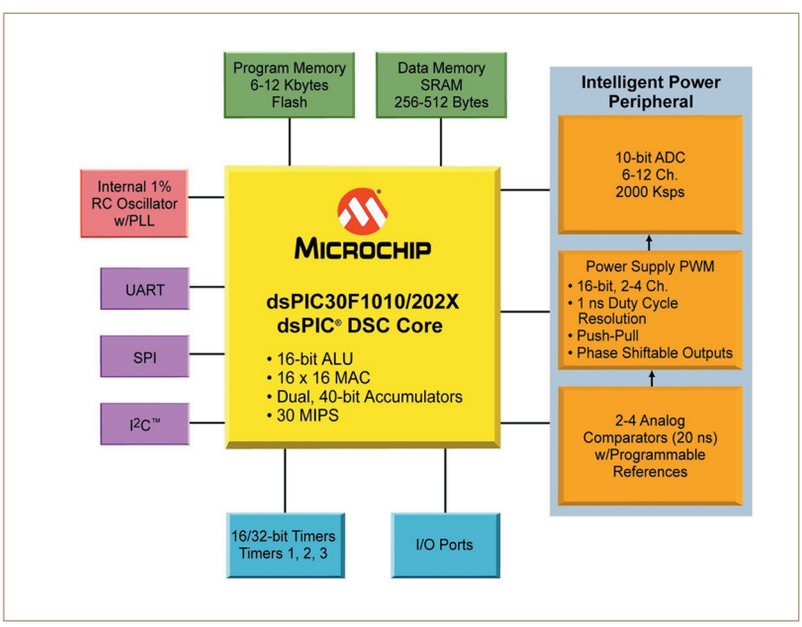

Figure 2: Example DSC for digital power conversion

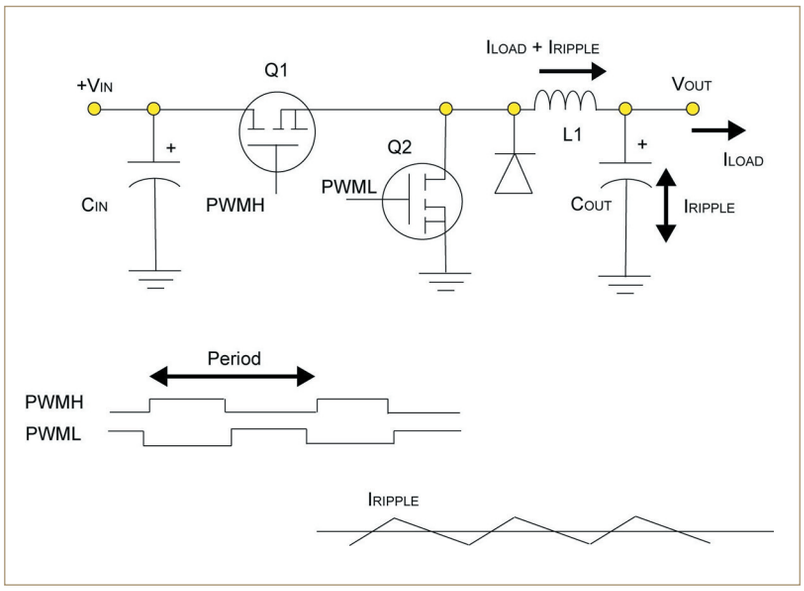

Figure 3: **Synchronous buck converter**

internal voltages required to provide a single-supply voltage to the DSC; a precision RC oscillator and internal PLL circuits to provide all clock signals required to drive the processor and high-speed peripherals; sufficient communications peripherals; flash memory and RAM; small size; and an extended temperature range.

Designers must also consider the auxiliary power required for the control circuits and the DSC. The DSC in Figure 2 supports a single input voltage and has the necessary power management capabilities to simplify the auxiliary power circuit, as well as improve reliability.

In some applications, such as AC/DC converters, the device can perform the conversion control, as well as features such as PFC. The digital PWM feature that supports the addition of functions is an independent time basis for the PWM complementary pairs. By using 'spare' PWM signals and the software running on the DSC, there is no need for an external PFC chip, which further increases the power supply's reliability.

Implementing the digital loop

An example digital control loop shows how the choice of DSC or other architecture affects the design. Figure 3 shows a synchronous buck converter, so called because transistor Q2 is switched on and off synchronously with the operation of the primary switch, Q1. The idea is that a MOSFET is used as a rectifier with very low forward-voltage drop. The converter's overall efficiency is improved when the diode's voltage drops; and the synchronous rectifier (MOSFET Q2) requires a second PWM signal complementary to the primary PWM signal. Q2 is now on when Q1 is off, and vice-versa. This is called 'Complementary PWM' mode.

Figure 4 shows a SMPS control loop. The most important fact to note is that there are delays associated with each block. The sample-and-hold circuit typically samples every 2 to 10 microseconds, and the ADC requires approximately 500 nanoseconds to convert the analogue feedback signal to a digital value.

The proportional, integral, and differential (PID) controller is a program that runs on the DSC with a computation delay of about 1 to 2 microseconds. The controller output is converted to a PWM signal, which drives the switching circuitry. The PWM generator can introduce significant delays if it cannot immediately update its output when given a new duty-cycle. Additionally, the transistor drivers and associated transistors introduce delays from 50 nanoseconds to about 1 microsecond, depending upon the devices used and the circuit's design. The output filter, typically implemented with an inductor and capacitor circuit, can also cause significant delays.

The delays associated with the conversion of the analogue feedback signal, the digital calculations by the processor and the output delays of the digital PWM to the power transistors are added to the sampling-rate delays. The effective sampling frequency of the primary control loop is the inverse of the controller and sampling delays. In this example, the control delay is 4.1 microseconds, resulting in a sampling rate of approximately 244kHz.

The controller bandwidth is the effective controller sample rate divided by the over-sampling ratio. In general, six to ten times over-sampling is required for loop stability. In this example, a six times over-sampling rate is needed to achieve the required performance of the loop. The estimated controller bandwidth is 40kHz. The addition of feed-forward terms to the control algorithm can increase the performance of the controller beyond the capabilities of a traditional PID controller with a 40kHz bandwidth.

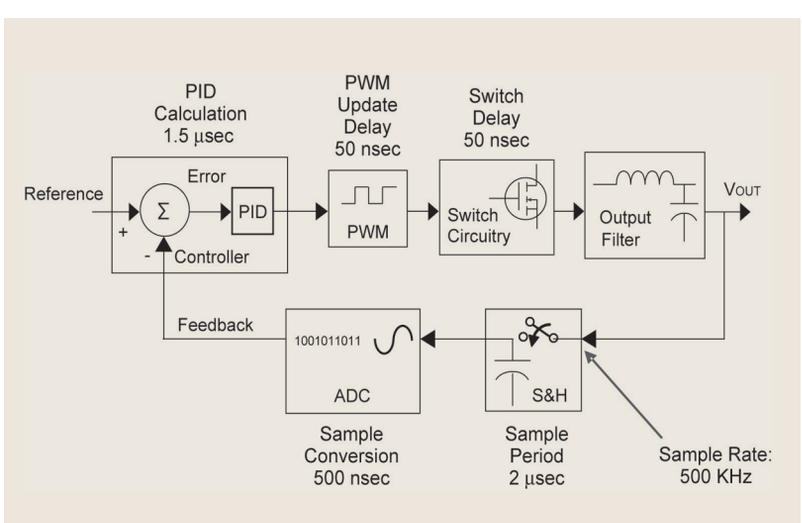

Figure 4: **Example SMPS control system**

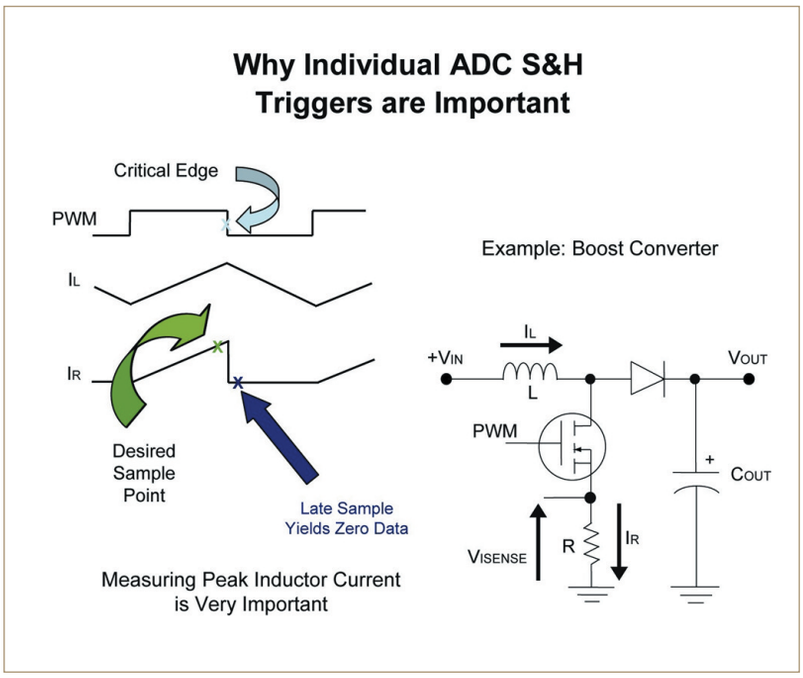

Figure 5: **Example of asynchronous ADC sampling**

PWM resolution

To prevent the PWM ripple from affecting the controller, the PWM reload frequency should be at least four or five times higher than the DSC's bandwidth. In this example, the ratio is 10 : 1, which sets the PWM frequency to 400kHz. Now that the PWM reload frequency has been set, the PWM's resolution can be determined.

Many vendors and customers are confused about the term 'PWM resolution'. This is not how wide a particular counter is, but rather how many counts (minimum possible PWM time slices) that can occur within a PWM-cycle period. In the power-supply, PWM resolution is specified by the smallest time increment achievable in the PWM duty cycle, typically in nanoseconds. If a DSC's digital PWM module does not have adequate resolution, the control system (hardware or software) will dither its outputs to achieve the desired average output. In power-supply applications, PWM dithering can create problems with ripple currents, and cause the control to enter an unfavourable mode of operation called 'limit cycling'.

PWM resolution = PWM counter frequency/PWM frequency! The chosen PWM frequency determines the necessary PWM resolution. This example requires approximately 11 bits of resolution, so the PWM clock must operate at around 1GHz.

The SMPS software implements the control algorithm, the central 'core' of which is the PID loop. The PID software is typically small – one or two pages of code – but its execution rate is very high – often hundreds of thousands of iterations per second! This rate requires the PID software routine to be as efficient as possible. An assembler offers a good method to ensure 'tight code'.

The execution time for the PID software determines two things: the PID iteration rate, which determines the amount of time between control-loop updates; and the PID execution time, which is in the critical path between the feedback sample and the PWM update.

The PID control loop is interrupt-driven by the ADC on a fixed-time basis. Any system function that can be executed in an "Idle Loop" should be executed outside the PID- control software loop. This includes voltage ramp up/down, error detection, feed-forward calculations and communication support routines. Any other interrupt-driven processes, such as communications, must occur at a lower priority than the PID loop.

Digital power conversion requires some unique ADC sampling capabilities, to achieve a practical implementation that does not require excessive processing power. The system implements a control loop where the DSC drives the signal sampled via the PWM state. The system has knowledge of when to sample the signal of interest, to provide the greatest information. Figure 5 shows the importance of this capability to trigger the

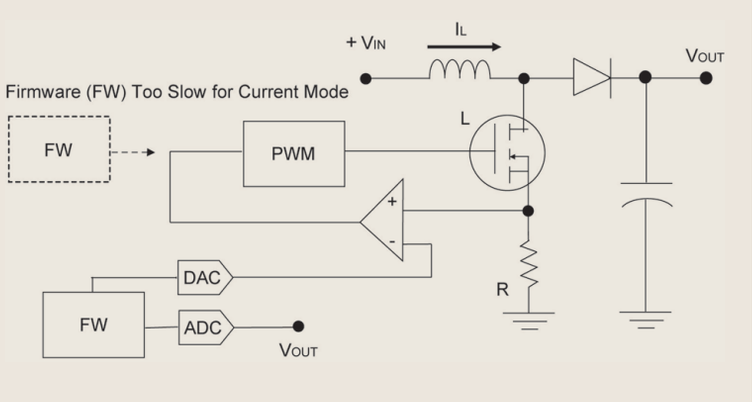

Figure 6: **Current limiting using analogue comparator**

ADC conversion at a precise point.

To minimise cost in power-converter applications, it is desirable to be able to measure voltages and/or currents at points that are near ground potential. This saves the cost and complexity of circuitry needed to handle the large common-mode voltages required to directly monitor the current through the inductor L.

In this example, the inductor current flows through the transistor when the transistor is turned on. It is desirable to measure the peak current, which occurs just as the transistor turns off. If the user cannot capture the current sample at the correct time (e.g. the sample is late), the transistor will be off and therefore no current will be measured.

As shown in Figure 5, the ability for asynchronous conversion, where the ADC is not limited to a periodic conversion rate, is critical in digital power-conversion applications. These applications require that the sample points be aligned at precise locations that are set in relation to the driving signal from the PWM. Multiple ADC sample-and-hold circuits are also important, as they can be flexibly triggered directly by the digital PWM peripheral. Triggering via software (versus triggering from the digital PWM) will not yield usable results, due to jitter introduced from the software. This will also introduce an unacceptable processing time for the software.

Analogue comparators provide additional benefits that are not practical or desirable to perform directly in the digital control loop. The reasons for this are:

- ADCs cannot monitor signals continuously.
- ADC monitoring is limited by the ADC's speed. If it spends all its time monitoring a specific signal, it cannot monitor anything else.
- ADC-based current monitoring increases latency between current measurement and PWM output (> 300ns).
- Analogue comparators enable latencies of approximately 25ns, from current measurement to PWM output.
- Analogue comparators provide processor-independent monitoring of over-voltage or over-current conditions.
- Analogue comparators can perform current mode control without loading the processor software or ADC.

In general, analogue comparators that are used to perform current limiting or fault shutdown of the digital PWM signals are critical to the implementation of digital power conversion. Figure 6 shows a system example of using analogue comparators to perform current limiting.

The ways in which analogue comparators are connected to digital power supplies are also important. For example, each analogue comparator should have its own 10bit DAC to enable the user to control the comparator's threshold. The reference must be accurate and stable, and the comparators must have fast response.

Typically, the time from when the analogue voltage is sensed to when the comparator modifies the PWM output should be about 20ns. It is during this time that current limiting control or fault response is performed. This response time is far faster than what is possible via software 'polling' techniques, which use the ADC and processor software to modify the PWM outputs in response to changing conditions.

Conclusion

Part of the value of using digital techniques in power supply products is the freedom that it affords designers in creating and protecting new intellectual property (IP). Designers using new, flexible DSCs for digital power conversion are finding that they can develop innovative topologies and algorithms. This new IP can be quickly and efficiently tested, as it is implemented in firmware rather than hardware.