Prospects of IGCT Technology

To improve performance, reduce the size and cost of power electronic systems and allow more flexibility in designing power electronic application, the development trend in high power semiconductors is toward higher current and voltage ratings. In this article, recent advances in Safe Operating Area (SOA) of a new range of High-Power Technology IGCTs are presented, with a glimpse of the future that these advances enable. **Tobias Wikström and Sven Klaka, ABB Switzerland Ltd, Semiconductors**

The Integrated Gate-Commutated Thyristor (IGCT) is a power semiconductor switch designed for use in power electronics applications at the very highest power levels. Thanks to its thyristor design inheritance, it has the necessary properties for switching large amounts of electric power in one component. The IGCT has been utilised in medium voltage drives, interties, STATCOMs, solid-state breakers and choppers. This article focuses on recent advances in IGCT technology, introduces the new 'High Power Technology' (HPT, Figure 1) and provide an overview of the future technology.

When the IGCT was introduced in the 1990's as a hard-driven GTO, its basic design still bore many resemblances to the standard GTO. The main difference was the switching mode – the hard drive: a means of turning the thyristor off exclusively in p-n-p transistor mode, like the IGBT. The advantages of p-n-p over n-p-n-p (GTO) turn-off are two-fold: the process is homogeneous, thus allowing a sound snubberless switching capability, and it allows more aggressive and low loss silicon designs. In the on state, it is a latched thyristor, which gives it very low on state losses and a wide design window for tuning its properties to fit the application.

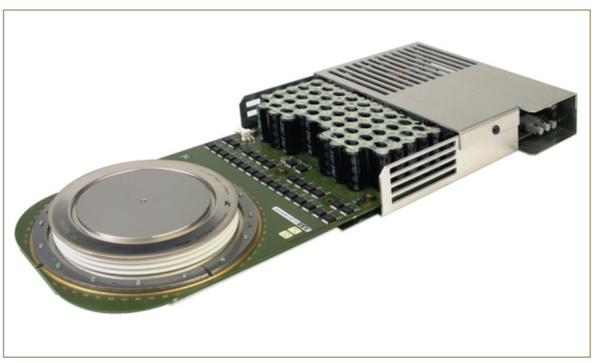


Figure 1: The new HPT IGCT appears in 4.5 and 6.5kV variants

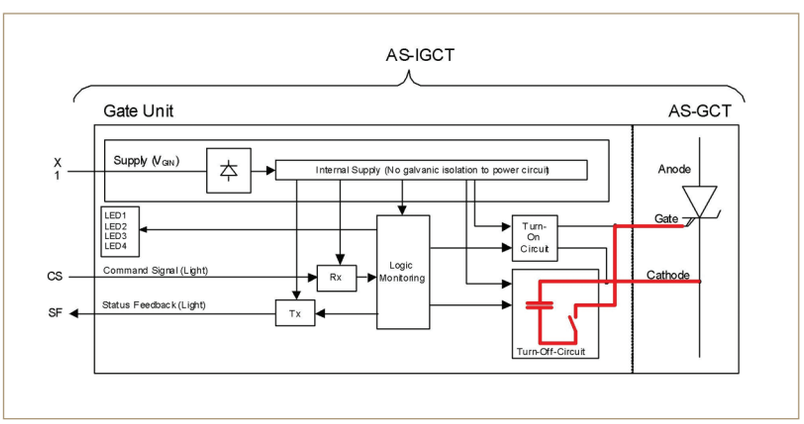


Figure 2: A schematic circuit diagram of the IGCT; left the gate unit with its outside connections on the left hand side. The GCT power semiconductor connecting to the main power circuit is situated to the right of the dashed line

SOA margins for the future

The challenge of IGCT technology has always been to scale up its turn-off capability (RBSOA). In small-area IGCTs, RBSOA has been shown to exceed 1MW/cm², well above the limit where other parameters, like losses and surge-current capability are more limiting. As shown further below, the larger the area, the lower the specific power handling capability. A reasonable approximation is that RBSOA scales with the square-root of the device area. The 4in diameter IGCT produced up to date (5SHY 35L4510) has been specified to 3500A @ 2.8kVDC. With the state-of-the-art HPT technology, the specified turn off capability for the same voltage rating will increase to 5.5kA. Even though today's IGCTs are mainly thermally limited, the user benefits are still two-fold: over-current trip levels can be set higher, and operation of the drive will become easier and more reliable.

In many applications there are requirements for short-term overload conditions. As long as the thermal mass of the heatsinks provides a slow enough temperature rise, these requirements can now be fulfilled.

Driving the IGCT

The reason for the sub-linear scaling of RBSOA lies in the details of how the IGCT is turned off. The gate unit controls the bias of the pn-junction between the cathode (n) and gate (p) contacts (Figures 2 and 3). It is also important to note that the term IGCT refers to the gate unit and the power semiconductor, which by itself is referred to as a GCT. In the on state, the gate unit provides a small forward current that keeps the thyristor latched. During turn off, the gate unit reverse-biases the pn-junction by activating its turn-off channel, marked in red in Figure 2.

The turn-off channel is a low-inductive voltage source biased just below the reverse blocking capability of the pn-junction. It forces the cathode current into the gate circuit at a rate governed by the stray impedance of the gate circuit (Figure 3, during t_{com}). The entire load current must be diverted from the cathode before the device functions as a p-n-p transistor. In addition to handling the full anode currents, it has to complete the commutation in much less than 1µs. Once

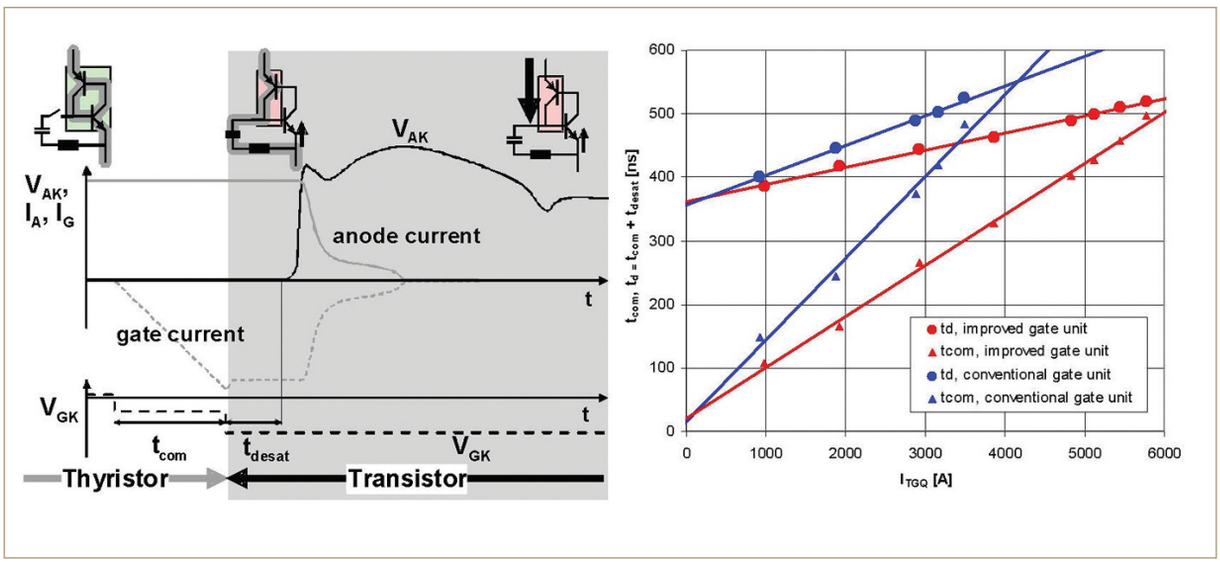


Figure 3: : IGCT turn off. On the top left, the current paths in an equivalent circuit consisting of the classical n-p-n + p-n-p transistor abstraction of the thyristor are shown. On the bottom, gate and cathode current waveforms are shown together with the anode voltage waveform. Right the current dependence of t_{com} and $t_{com}+t_{desat}$ shown for the improved HPT technology (red) and conventional technology (blue)

Figure 4: : 4in 5.5kA GCT wafer

this time has elapsed, the IGCT starts to build up voltage (after completion of tcom and tdesat in Figure 3) and it is an absolute necessity that the device now operates in p-n-p transistor mode.

Looking at the IGCT as a discrete power device, there is an apparent macroscopic speed condition that must be fulfilled for safe operation - the hard drive limit. It is the cross-over point in the graph to the right of Figure 3. It is a characteristic of the GCT wafer because different wafer designs react at different speeds ($t_{com}+t_{desat}$), as well as of the gate unit (t_{com}) because of its stray impedance. This is one of the reasons to why large-area devices are more challenging – the higher the current is, the harder the demands get regarding the gate circuit stray impedance.

To meet the increasing demands of power handling and the resulting need to lower stray inductance, the gate unit underwent a series of improvements: New capacitors with improved equivalent series capacitance; higher capacitance; gate unit assembled on a 6-layer PCB instead of 4 layers; optimised layout of the gate unit; and more MOSFET switches connecting the turn-off channel.

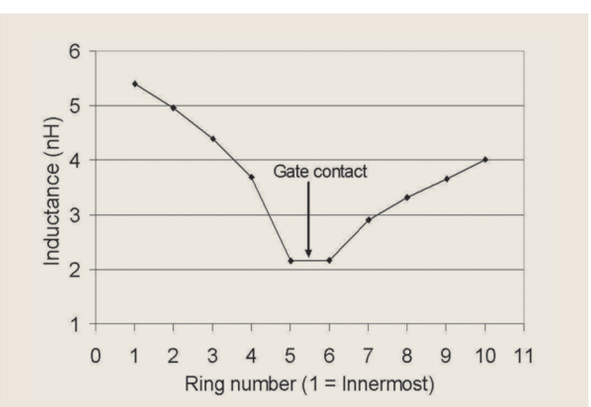
Making a more robust wafer

A more detailed model of the large-area GCT wafer (Figure 4) shows a parallel connection of thousands of GCT segments, all of which need to be operated synchronously to avoid current redistribution. The segments are arranged in ten segment rings on the wafer. The gate contact is ring-shaped and located between segment ring five and six. Unavoidably, these segment rings have a slightly different impedance to the gate unit.

A simulation of the wafer, housing and gate unit geometry reveals the different stray inductance load of individual segment rings dependent on the ring number (Figure 5). This imbalance results only from the constraints on how the current flows from the wafer to the gate unit. Considering that the active area of a segment ring increases with the square of the ring number, the impact of this imbalance is to be expected on the outermost ring. This is also confirmed by experiments; the outermost segment rings are in vast majority in RBSOA failures.

Apparently, the inductance imbalance is a fact of life. Today, it can only be

Figure 5: : The stray inductance as experienced by the individual segment rings on a GCT wafer as a function of its placement



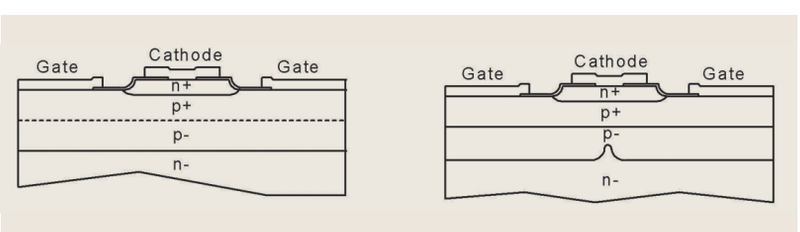


Figure 6: : Structure and doping design of a conventional GCT cell (left) and HPT technology with the corrugated p-base (right)

lowered with unrealistic effort because it is a result of mechanical constraints in the IGCT package assembly. Subsequently, the GCT device will inevitably be subject to some current redistribution as the gate signal propagates over the wafer. This is the second reason to why scaling up the area makes life tougher for the IGCT: the remotest cells get loaded with a higher stray inductance. And the only antidote from a silicon technology perspective is to make a wafer that shows less sensitivity to impedance imbalance.

With the HPT IGCT, ABB introduces a new design feature: the corrugated p-base. In Figure 6, the main characteristics of this technology are sketched: In conventional technology, the p-base diffusion is homogeneous over the whole wafer. In HPT technology, the deep p-diffusion is masked underneath the cathode fingers. As a result, the p-base has a corrugated appearance. Together with the new gate unit, it has a substantial impact on RBSOA.

The HPT technology is available in 4.5 and 6.5kV asymmetric IGCT versions. A conventional reference exists only for 4.5kV, which is why only these results are shown here. With HPT technology, the destruction limit of the IGCT has increased 40% at 125°C and by 80% at room temperature. The IGCT now demonstrates a negative temperature coefficient of maximum controllable current, illustrating that the device is now limited in the same way as IGBTs (Figure 7). With its new robustness, the HPT IGCT is also able to withstand SSCM (Switching Self-Clamping Mode), which is a harsh benchmark of ruggedness extensively described in connection with IGBTs over the last few years (Figure 8).

A technology that enables the future

Apart from the immediate benefits mentioned above, this novel technology allows future expansions of the IGCT range: Potential future 10kV IGCTs can now have competitive turn-off current ratings comparable with today's ratings of 6kV devices.

In principle, the technologies allow for better homogeneity of the turn-off process over the diameter of the wafer. A further increase of the wafer diameter appears feasible.

Combining these advantages, it is a safe bet that in near future we will see larger IGCTs capable of switching > 4kA against DC voltages of > 6kV enabling 3-level 20MW Medium Voltage Drives for 6kVAC motors without any need for series or parallel connection. On the other side of the application range, due to the enormous turn-off capability in combination with a potentially thyristor-like on state voltage drop, additional possibilities arise for the use IGCTs as wear-resistant static breakers.

Figure 7: : The maximum turn-off current of the HPT compared to the conventional IGCT specification

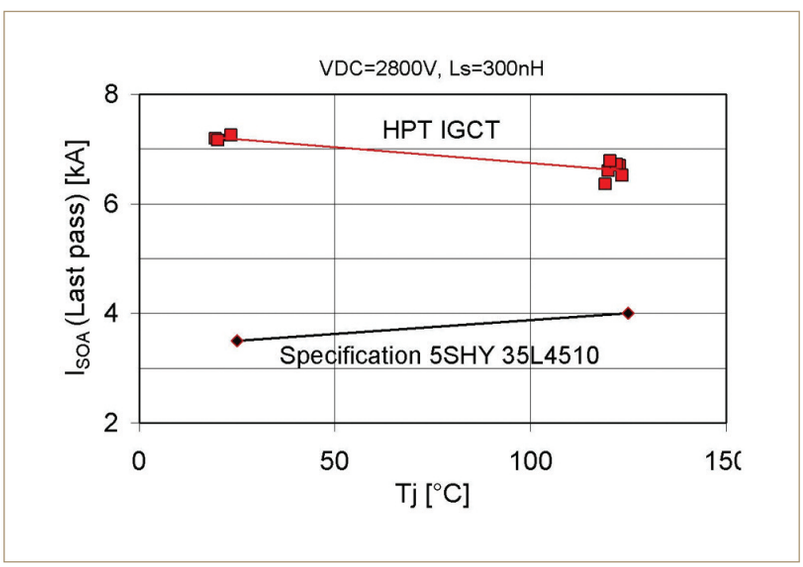


Figure 8: : An HPT IGCT performing turn-off under SSCM conditions