POL Step Down Regulators and How to Check for Stability

There are new 'point of load' step down regulators on the market that offer many features and are especially designed to be very easy to use. The new LM20 k family is an example of combining ease of use with many features required for challenging point of load designs. A new structural architecture is making all the features in combination with high output load current possible in a very small package. **Michele Sclocchi, Senior Principal Applications Engineer Power Management Europe, National Semiconductor, Milano, Italy**
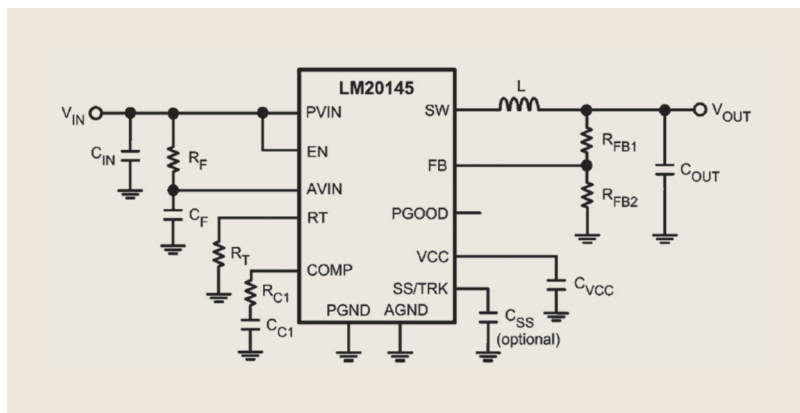
Even with easy to use devices, it is sometimes difficult to predict the stability of the control loop by calculations only. There is an easy way to determine the 0dB crossover frequency and phase margin of any switch mode power supply without needing an expensive network analyser to do so. In the following paragraphs, I will explain how to set up such a measurement circuit and how to get more knowledge about the control loop stability of one particular design besides load transient tests only.

What is special about point of load regulators?

For point of load regulation, usually low input voltages such as 5V are stepped down to lower output voltages such as 2.5, 1.8, 1.1V or even lower. Many applications requiring such low voltages tend to need high currents. Typical loads to power with point of load regulators are FPGAs and ASICs which have a very special power management need.

High performance FPGAs especially require multiple power rails. Two power rails for core and IO are quite common. Some FPGAs however, need even more supply rails. The actual current

requirement is highly dependent on the actual usage of the FPGA. Other concerns of some FPGAs are monotonic start-up of its supply voltages, as well as power sequencing of the different rails.

All the requirements mentioned above make it difficult for just any power management IC to be used as point of load supplies for FPGAs or similar loads. The new LM20000 family of ICs offers a whole family of point of load regulators which can easily be interchanged once a design has started. If final code in an FPGA is changed over a development cycle and happens to require more current, the LM20000 family member with a higher current rating can be employed without losing much design time since all members of the family are very similar to each other.

Multiple point of load regulators can be synchronised to each other to avoid frequency problems, such as the beat phenomenon which can occur if different switching frequencies are used in one system. The parts will start-up into a pre-biased load with a monotonic ramp to prevent any latch up or similar behaviour on some FPGAs or ASICs. With a soft-start and tracking feature, the start-up can be closely controlled to

align with the requirement of each individual FPGA or ASIC type. Figure 1 shows a typical example of a high current point of load power supply. Since the high side and low side power transistors are both included in the power management IC, only very little external component selection and optimisation is necessary.

A solution is not an IC by itself

Engineers who are not mainly power management designers especially need some support to optimise a power supply design. Simulation tools can help to show behaviour in the real world. Even more important to design support than simulation capability is having a tool that helps to select the right external components in the first place. Simulation tools usually do not directly give the trade-offs between one component selection versus another component selection. The LM20000 family of regulators offers an Excel design guide that helps quickly to select the optimised external components and even calculates the predicted stability. Figure 2 shows the main view of the straight forward design spreadsheet offered for free on the National Semiconductor webpage.

High Power Density and Self-Synchronisation

National Semiconductor Corp. has introduced a new line of buck switching regulators that are the first in the industry to feature self-synchronisation. Part of its PowerWise energyefficient product family, the regulators feature a variety of input voltages and output currents, and offer a combination of power sequencing, adjustable switching frequency and clock synchronisation options.

The new line of LM201xx and LM202xx synchronous buck regulators includes 2, 3, 4 and 5A output current devices with an input voltage range from 2.95 to 5.5V. Each regulator integrates two switching MOSFETs and utilises an externally compensated peakcurrent-mode control loop, providing superior load transient response in low duty cycle applications. The external compensation allows the performance to be optimised for the output capacitor and inductor. With current-mode control, two external components are needed for compensation. The ability of the 3 and 4A clock synchronisation devices to self-synchronise when in out-of-phase operation reduces input capacitance and voltage ripple in power supply designs.

Each buck regulator has a precise internal voltage of 1.5% accuracy from -40 to 125°C. They include a precision enable pin that allows accurate setting of the turn-on threshold and sequencing of the turn-on of multiple devices, eliminating the need for an external voltage supervisor chip. Also included is a power good indicator that regulates the output voltage within tolerance and can sequence loads that have an enable input. A tracking and soft-start feature allows to set the output to accurately track an external supply, as well as provide a controlled voltage ramp to protect loads against in-rush current that could cause latch-up. The monotonic start-up into pre-biased load feature prevents the possibility of latch-up in field programmable gate array (FPGA) and

application-specific integrated circuit (ASIC) applications. Over-voltage and under-voltage events are monitored at the output voltage.

The low-voltage LM20123, LM20124 and LM20125 buck regulators feature fixed frequencies of 1.5MHz at 3A, 1MHz at 4A or 500kHz at 5A for enabling the smallest solution size. The low-voltage LM20143, LM20144 and LM20145 buck regulators feature adjustable frequencies for maximum design flexibility. The low-voltage LM20133 and LM20134 buck regulators provide clock synchronisation for synchronisation to an external clock source. The low-voltage LM20154 buck regulator features out-of-phase clock output for current sharing or out-of-phase operation. The high-voltage LM20242 buck regulator, offered in a 20pin TSSOP package with exposed pad, operates with an input voltage range from 4.5 to 36V and delivers up to 2A of continuous output current. The LM20242 features adjustable frequency from 250kHz to 1MHz.

Evaluation boards are available for most of the types. The M20145 demonstration board has been designed to balance overall solution size with the efficiency of the regulator. It measures just 1.0 x 1.0in on a two layer PCB, with all components placed on the top layer. The power stage and compensation components have been optimised for an input voltage of 5V, but for testing purposes, the input can be varied across the entire operating range. The output voltage is nominally 2.5V. The control loop compensation has been designed to provide a stable solution over the entire input and output voltage range with a reasonable transient response.

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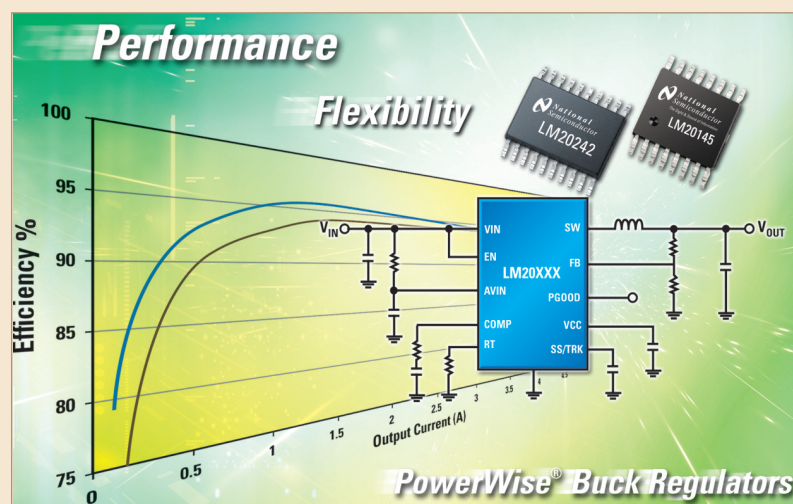
National's new line of LM201xx and LM202xx synchronous buck regulators includes 2, 3, 4 and 5A output current devices

Using a mathematical spreadsheet approach to find out the stability of a switch mode power supply is easy and convenient. Especially if tools such as described in the previous paragraph exist. However, how can a design engineer be sure that the real hardware has enough stability margin? Spreadsheets will only give the result of input variables that the user enters. When looking at output capacitor's equivalent series resistance (ESR), it is difficult to get an exact value

from a manufacturer and when multiple capacitors with different or the same ESR are put in parallel. What will the total output capacitor ESR look like for the control loop?

A very good way to check for the stability in a power design is to just measure it in real life. This can be done by measuring the 0dB crossover frequency of the regulation loop transfer function, as well as the phase margin at the frequency of the 0dB crossover using an ordinary

signal generator and an oscilloscope. Figure 3 shows the set-up for the measurement.

Checking stability with only a scope and a signal generator

The first step for the measurement set-up is to add a small signal injection point. This can be done by putting a 20Ω resistor into the feedback path between the output voltage and the high side connection of the high side feedback resistor.
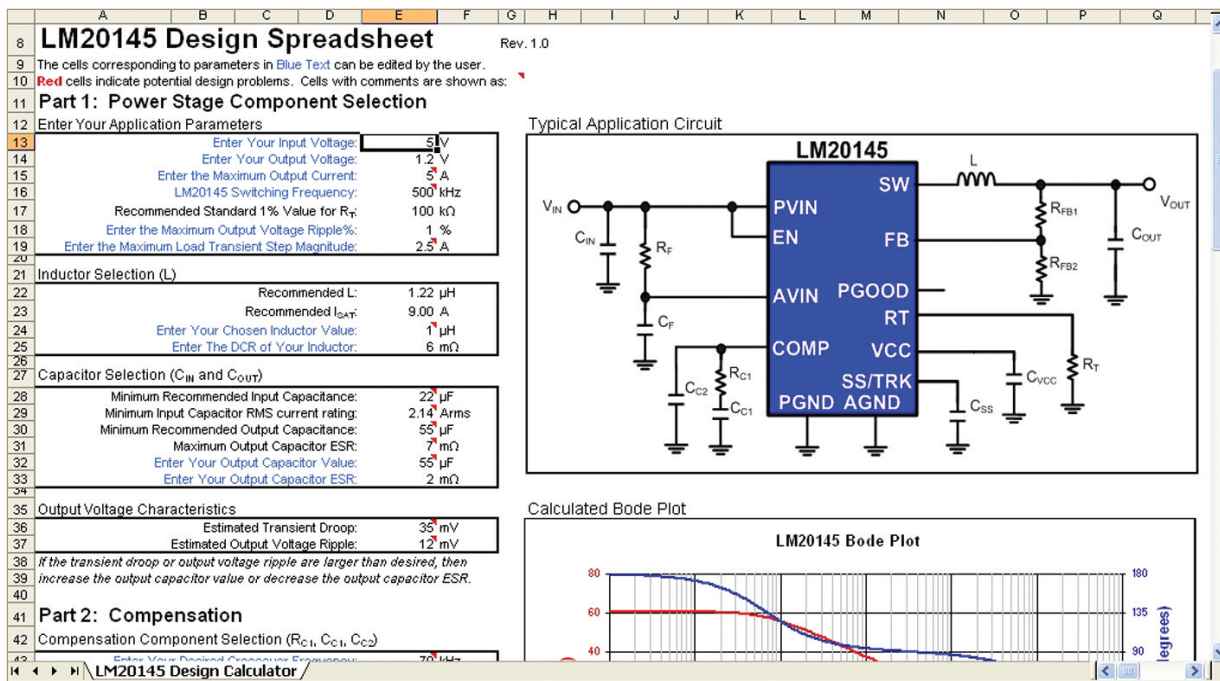
Figure 2: **Design spreadsheet to help optimise the design of point of load power management solutions**

Next step is to set up a signal generator with a transformer on the output to prevent any DC currents to flow from the circuit under test to the signal generator. The transformer T1 is not very critical. A simple offline 220 to 12V transformer will work fine. Other simple transformers will also do the job.

Set the signal generator to a frequency below the switching frequency of the power supply circuit. Waveform should be set to sine wave and the amplitude should be set so that behind the transformer T1 (at points A and B) the amplitude of the sine wave is between approximately 30 to 100mV.

Set up an oscilloscope with one channel attached to point A and the other channel to point B. Set the oscilloscope to bandwidth limiting to avoid switching noise from shadowing the sensitive measurement. Set the oscilloscope to the lowest range possible such as 10 or 20mV per division.

Power up the LM20145 or other power management circuit and watch the

oscilloscope screen. There should be one sine wave visible on one channel and probably one line on the other channel. When sweeping the frequency of the signal generator across the range from a few hertz up to half the switching frequency of the power supply. Depending on the transformer T1 used, the amplitude of the sine wave might change a bit, since the gain of the transformer might change over frequency. It might be necessary to adjust the amplitude of the signal generator when sweeping its frequency to keep the amplitude of the injected signal in the range of 30 to 100mV.

When sweeping the signal generator frequency, there should be one point where channel A and channel B on the scope both show a sine wave with the same amplitude. This is the frequency when the gain of the power supply control loop is 1 or 0dB. This point gives the bandwidth of the power supply system. At this frequency a phase shift between channel A and channel B can

be seen. Take a one shot plot with the scope and put one time marker on the peak of the one channel sine wave and the other time marker on the peak of the other channel sine wave. The measured phase difference in degrees is the phase margin of the power converter transfer function.

Conclusion

Modern point of load regulators offer many great features to build a power supply for FPGAs and ASICs. Thanks to a family of parts, a basic power management design is easily scalable without having to redesign the whole circuit. Spreadsheets offer good design assistance in selecting the external components. For finding out how stable the real design actually is, an easy test procedure with low cost standard equipment was shown.

So, all that is needed to start having fun in the lab is the bosses' request to design a power supply for an FPGA or ASIC.

Figure 3: **Set-up to measure 0dB crossover and phase margin of a power supply with an oscilloscope and a signal generator**