Super Junction MOSFET with Robust Body Diode

Switch mode power supplies, ballast and white good applications need MOSFETs with good body diode characteristics. If the body diode reverse recovery characteristics are poor, it increases the turn-on loss of the MOSFET. Also, the body diode should be able to handle high di/dt and dv/dt. Hence, MOSFETS with good, rugged body diodes are needed for these applications. Fairchild has used numerical simulations in mixed mode circuit and device conditions to analyse what is happening inside the device during the reverse recovery transient. This has helped to understand the reasons behind the failure and to design a rugged SuperFET device. **Praveen M. Shenoy, Sampat Shekhawat and Bob Brockway, Fairchild Semiconductor, Mountaintop, USA**

Super junction (SJ) charge balance concept devices [1, 2] have gained market acceptance as they have much lower R_{dson} compared to regular MOSFETs. Devices were introduced in to the market in the late '90s. These devices are very attractive for high voltage as the R_{dson} is proportional to BV, unlike conventional devices where R_{dson} is proportional to $BV^{2.5}$. Hence, SJ devices have much lower R_{dson} compared to regular MOSFETs, particularly at higher voltage ratings.

However, one drawback of SJ devices has been the poor body diode reverse recovery characteristics. In SJ devices, P-N pillar structures are used to obtain charge balance. This results in two issues for body diode, 1) much larger PN junction area which increases I_{rrm} and Q_{rr} due to higher injection and 2) high dv/dt due to quick depletion in the pillars which can cause snap-back/turn-on of the parasitic NPN transistor.

Early generation SJ devices had high reverse recovery current and failed during some reverse recovery events [3]. Even though the body diode characteristics have improved over time, some SJ MOSFET body diodes are still not as rugged as conventional MOSFET body diodes. Reverse recovery measurements show that SJ MOSFET body diodes fail at a di/dt of just 100A/µs, whereas SuperFET devices are virtually indestructible, surviving >1000A/µs. Fairchild has also introduced rugged SuperFET devices with fast recovery body diodes which have low T_{rr} and Q_{rr}.

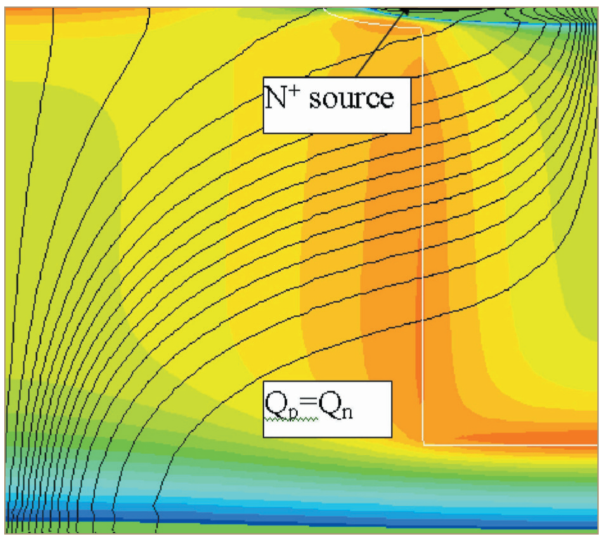


Figure 1: Mix mode simulation results for the balanced case ($Q_p = Q_n$) showing electric field and current flow lines during 25% I_{rrm} of reverse recovery (conditions: 20A, 400V, 25°C, 275A/µs). Majority of the current flows directly in to the P+ body contact with remaining current flowing under the source

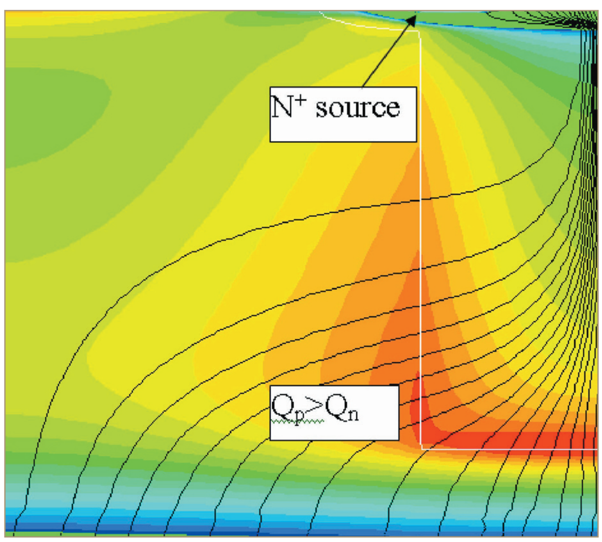


Figure 2: Mix mode simulation results for $Q_p < Q_n$ case showing electric field and current flow lines under conditions of Figure 1. Majority of the current flows under the source which could lead to parasitic bipolar transistor turn-on

Experimental results and simulation

The reverse recovery characteristics of super junction MOSFETs were measured and compared at a di/dt of 100A/µs. Most SJ MOSFET body diodes failed while SuperFET devices passed; this type of failure was observed on many devices and hence, is not an isolated case. The failing devices destroy themselves during the phase where the voltage is high and current and di/dt is still high. Two dimensional numerical device physics simulations in mixed mode were performed to understand what happens inside the device during reverse recovery. The full reverse recovery circuit is simulated with physics based SJ-MOSFET for

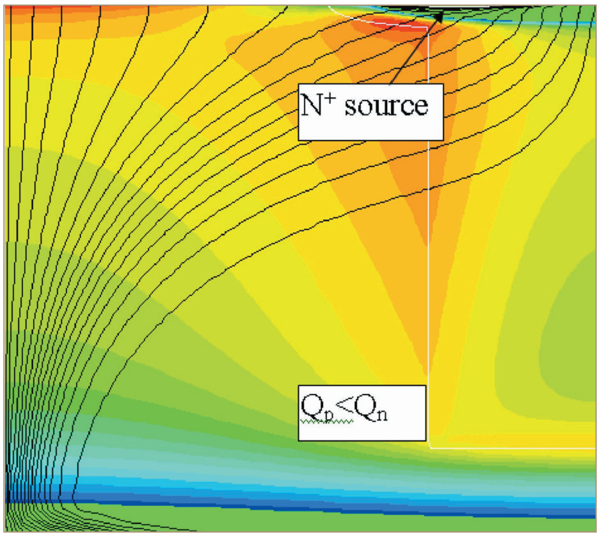


Figure 3: Mix mode simulation results for $Q_P > Q_n$ case showing electric field and current flow lines under conditions of Figure 1. All the current flows directly in to the P+ body contact and therefore there is no risk of parasitic bipolar transistor turn-on

switching and another physics based SJ-MOSFET with gate shorted to source for body diode. The parasitic inductances and capacitances are also put in to the circuit. The current flow contours during this critical phase were analysed closely to understand the diode failure mechanisms.

In a super junction device, perfect charge balance between the N and P pillars is not always possible due to processing variations. The effect of charge imbalance on the device characteristics has been discussed in literature [4]. For the reverse recovery context, three cases were analysed: perfectly balanced case ($Q_P = Q_n$), P pillar charge less than N pillar charge ($Q_P < Q_n$) and P pillar charge greater than N pillar charge ($Q_P > Q_n$).The electric field and current flow lines during t_b phase at 25% I_{rrm} were analysed as the failure on other devices was at around 25% I_{rrm}. These plots are shown in Figures 1 - 3.

In the balanced case (Figure 1), the peak electric field is at the pillar PN junction at about half the pillar depth and most of the current flows straight in to the P+ body contact and remaining current flows under the N+ source. For the $Q_P < Q_n$ case (10% imbalance), the peak electric field is at the top P-well junction and most of the current flows under the N+ source as seen in Figure 2. The high current flow under the source can lead to the parasitic NPN transistor turn on. The high electric field and current flow under the source causes localised heating in that area. This further accentuates the parasitic bipolar turn-on problem as with temperature, R_{bb} increases and V_{be} decreases. Hence, the $Q_P < Q_n$ case is prone to parasitic bipolar turn-on and failure during high current or high di/dt reverse recovery.

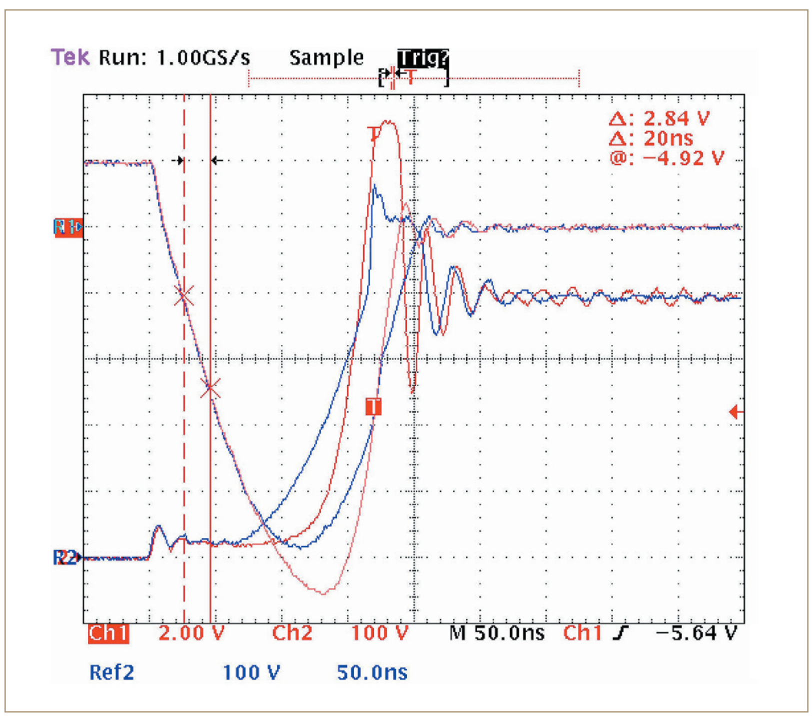
When $Q_P > Q_n$ (10% imbalance), the peak electric field is at the bottom of the pillar and all the current flows directly into the P+ body contact, as shown in Figure 3. There is no current flow under the source and heat generation spot is at the bottom, far away from the source region. So this design is immune to parasitic bipolar issue and more rugged for reverse recovery and UIS. Hence, it is desirable to design with $Q_P > Q_n$ so that even with process variations, it rarely goes in to the $Q_P < Q_n$ space. There is a very slight R_{sp} penalty (< 2%) with this type of a design and it could be offset with slightly higher starting Q_n.

Simulation for design

Based on the in depth analysis of the physics of the reverse recovery in SJ devices, Fairchild designed the SuperFET devices to have excellent dv/dt and di/dt ruggedness. Care was also taken in the layout to make sure all the hole current is collected with good body contacts. Figure 4 shows the reverse recovery waveforms of SuperFET (SJ) and KMOS (conventional MOSFET) at very high di/dt conditions. It can be clearly seen that both devices survive this extreme test. This shows that SuperFETs have very rugged body diodes, as good as or better than conventional MOSFET body diodes.

Some applications like asymmetric half bridge ballast circuits require low I_{rrm} and Q_{rr}. For those, fast body diode MOSFETs utilising minority carrier life time control are recommended. Lifetime killing using irradiation or heavy metal diffusion further reduces Q_{rr} and T_{rr} and increases dv/dt ruggedness. The above-mentioned conventional lifetime control techniques

Figure 4: Measured reverse recovery waveforms comparing Fairchild's FCH20N60 SuperFET device and conventional FCH27N50 device at very high di/dt conditions



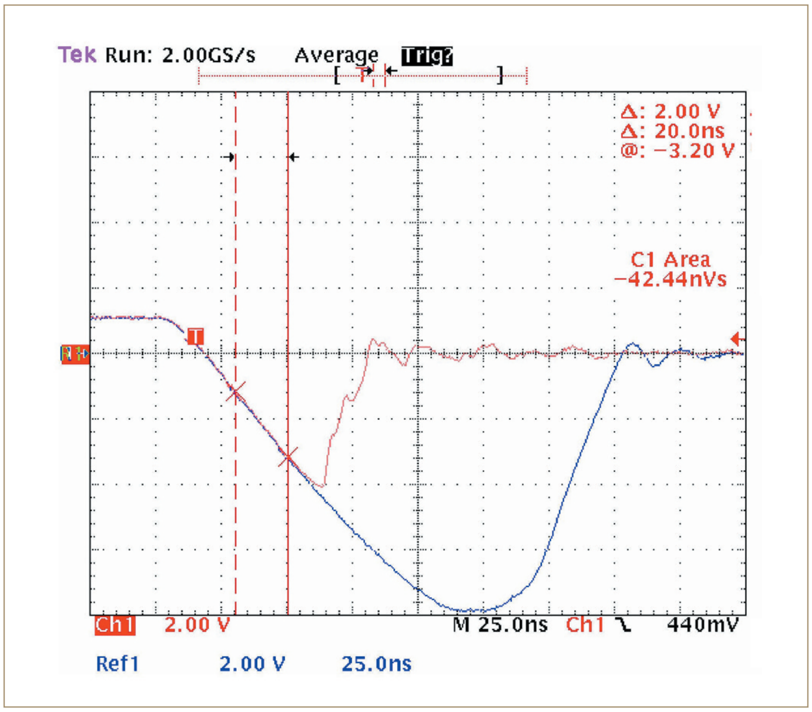


Figure 5: **Measured reverse recovery waveforms comparing Fairchild's FCP11N60 and FCP11N60F SuperFET devices at a high di/dt of 1000 A/µs. As expected, the fast recovery device has very low T_{rr}, Q_{rr} and I_{rrm} compared to the standard device**

can be used for super junction devices also to get fast body diodes. Fairchild has recently released a fast recovery version of SuperFET devices having very low T_{rr} and Q_{rr} and which are, at the same time, quite rugged at high di/dt and dv/dt.

Figure 5 shows the measured waveform comparing FCP11N60 and FCP11N60F (fast recovery version). It can be clearly seen that the fast recovery device has much lower Q_{rr} (6x), I_{rrm} (2x) and a low T_{rr}. The two parts were compared at different di/dt's ranging from 100A/µs to >1000A/µs and similar characteristics were seen. Also note that both devices are designed with ruggedness and do not fail under the extreme di/dt or dv/dt conditions.

Literature

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