Thermal Behaviour of Three-Level Trench Gate IGBT Modules in PFC and PV Operation

The control of the power semiconductors in a three-level NPC topology employs a set of 12 control signals in total. A back-to-back two-level/three-level inverter has been built to circulate power performing arbitrary load conditions to analyse the thermal dissipation of the power semiconductors. This thermal analysis utilises an IR camera to perform an in-situ measurement and allows precise modelling of thermal and electrical parameters. Once this experimental platform has been calibrated, the loss on each semiconductor chip can be acquired and compared with the simulated results. Hence, tuning of the model parameters becomes possible. **Marco Honsberg and Thomas Radke, Mitsubishi Electric Europe, Germany**

The continuously growing consciousness towards energy saving needs have led to intense research towards highly efficient power conversion methods. Online Uninterruptible Power Supplies (UPS) being connected and loaded 24 hours and 7 days, as well as photovoltaic (PV) inverters, are dedicated applications with a high potential in energy saving by an increase of the total system's efficiency. Besides the continuous improvement of the power device's inherent loss performance and the outlook to have Silicon Carbide (SiC) based switching devices and their optimised packaging technology widely available in a few years, three-level technology has been found efficient in decreasing a system's power loss.

Three-level IGBT modules, with their comparatively complex structure in terms of chip layout and their thermal performance under varying load conditions, are essential to fabricate a compact and reliable three-level inverter. Figure 1 shows a view into an opened three-level 13in one IGBT module. In addition to the pure NPC three-level structure, there is a 1200V-class IGBT to perform a braking operation in conjunction with the employed free-wheeling diode (FWD). Such a braking operation can become necessary in case a regenerative load is connected to the UPS. The circuitry of the module is shown in Figure 2.

All chips forming a P-side and, respectively, an N-side functional group, e.g T 1, T 2 and their FWDs and Clamp diodes (CLDs) and T 3, T 4, their FWDs and the CLDs, respectively, for the N-side are located on one AlN ceramic substrate for

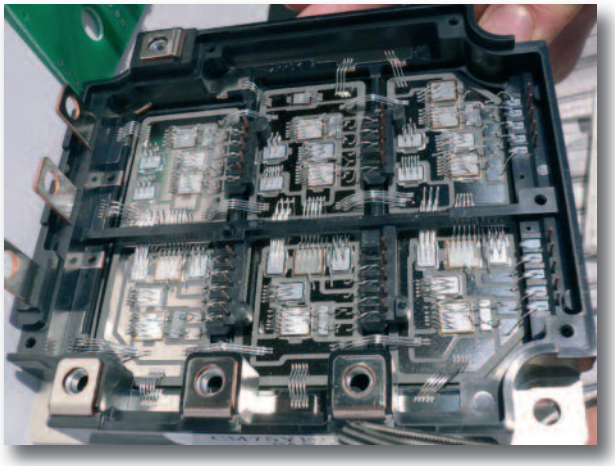


Figure 1: **Opened three-level IGBT module**

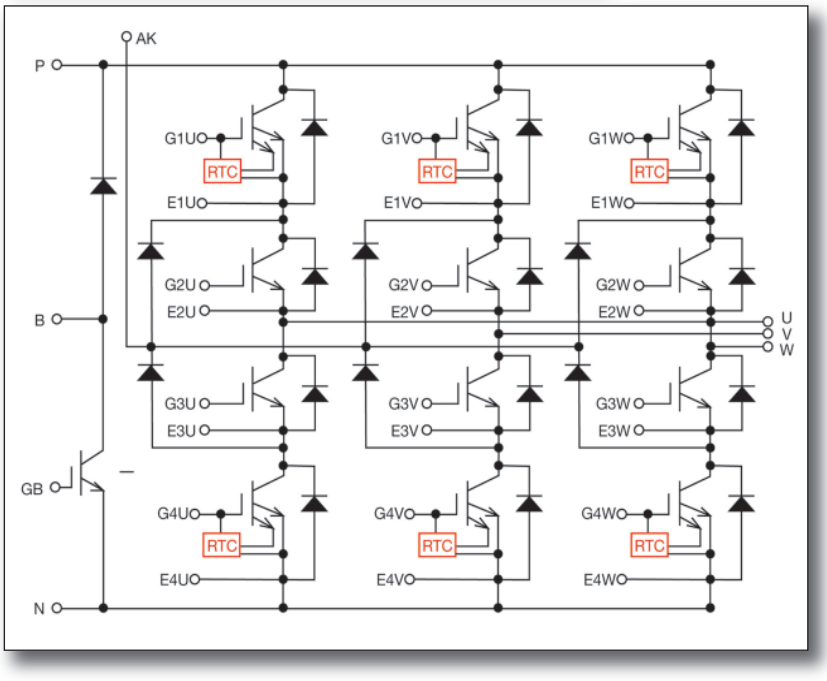


Figure 2: **Three-level IGBT module topology including circuitry**

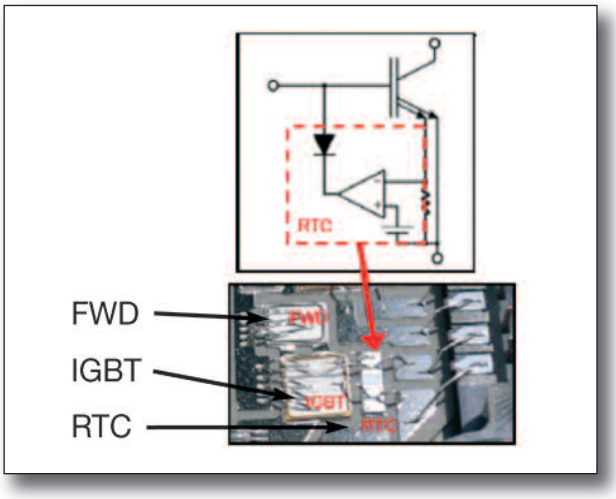


Figure 3: **RTC operation and chip**

best thermal conduction. The internal layout, power chips and the thermal profile in a sample module has been analysed by thermograph and baseplate temperature sensors under varying load.

Three-level NPC topology and short circuit detection

The outer switches (IGBT 1 and IGBT 4) are equipped with a real-time current controller (RTC), a unique technology utilising a fraction of the collector current to detect an over-current situation and to force the IGBT into a current controlled desaturation. The principle of the RTC and its location on the substrate is shown in Figure 3. Basically, the aforementioned fraction of the collector current is flowing through the shunt resistor (inside the red dashed line of Figure 3) and creates a voltage drop accordingly. The following comparator pulls down the Gate Emitter voltage (V_{ge}) when the reference voltage level (V_{ref}) is exceeded by shunt voltage drop.

A similar circuit has been used in previous generations of Intelligent Power Modules (IPM) for more than 10 years to control the desaturation current level precisely, and has been adopted here for an IGBT module the first time. As a result, the comparatively low current level reduces the stress on the IGBT during a short-circuit situation. Such a stress reduction improves the reliability of key applications like PV inverter and UPS. The increase of MTBF is a key objective for UPS applications where power quality and availability, as well as a long lifetime, is a main target for PV inverter. The inner IGBTs (2 and 3) are lacking this RTC, leading to a higher desaturation current. Hence, the module provides an essential feature to efficiently protect a three-level inverter system in short-circuit situations, as the described deliberate implementation of RTCs at IGBT 1 and IGBT 4 ensure that inner IGBTs (IGBT 2 and IGBT 3) would never desaturate before the outer ones. This feature of the three-level IGBT modules is simplifying the gate driver and the connected fault detection logic usually being implemented into a programmable logic device.

Power loss calculation approach

The thermal evaluation has been done by the modelling of the device and the characterisation of loss parameters like switching and conduction losses as a function of their influencing parameter. With this device data and the knowledge about the commutation in a real inverter operation, it becomes possible to perform a loss simulation for the specific operation conditions which are considered typical for PV-inverter or UPS operation.

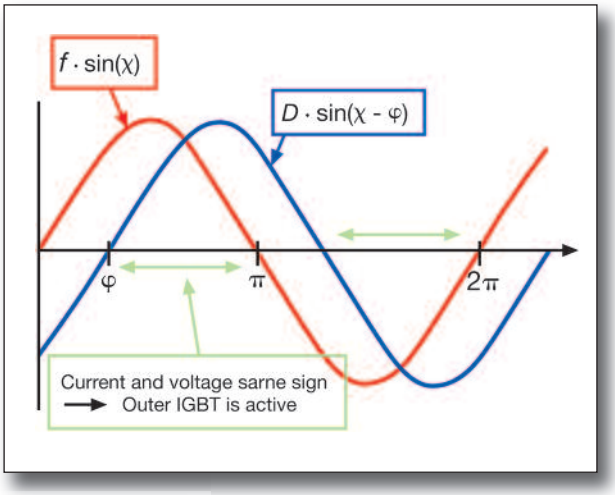
In three-level NPC configuration, the number of commutation paths is substantially higher and leads to a more complex way of calculating loss for the individual FWD/CLD or IGBT chip. The value and the direction of the current, in conjunction with the output voltage represented by a pulse width modulated (PWM) signal and their phase angle in between, are the input parameters of the loss calculation approach. Additionally, the chip inherent loss dependencies:

- $V_{ce(sat)} = f(I_c, T_j)$,
- $V_F = f(I_E, T_j)$,
- $E_{on}, E_{off}, E_{rr} = f(I_c, R_G, V_{cc}, T_j)$

have to be taken into account, where $V_{ce(sat)}$ is the saturation voltage, I_c is the collector current, T_j is the junction temperature of the chip and E_{on}, E_{off} are the switching energies to turn on or off the device and E_{rr} to recover the incorporated diodes respectively.

R_G represents the connected gate resistance and V_{cc} is the DC-link voltage. An arbitrary combination of voltage and current and their phase angle between them needs to be considered when performing the loss calculation (Figure 4). In the example during the interval where current and output voltage are having equal polarity, the 'outer' IGBT (IGBT 1 or IGBT 4 respectively) together with their corresponding clamp diodes are switching/recovering while the inner IGBTs (IGBT 2 and IGBT 3 respectively) are only having conduction losses as a function of the

Figure 4: **Arbitrary combination of voltage and current**



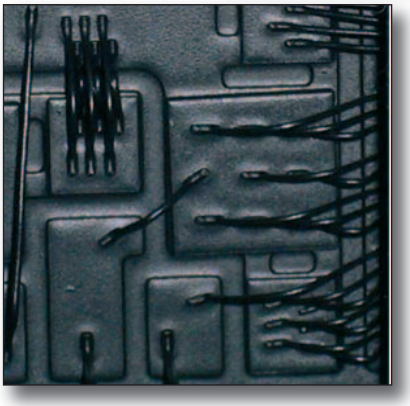


Figure 5: **Black painted chips**

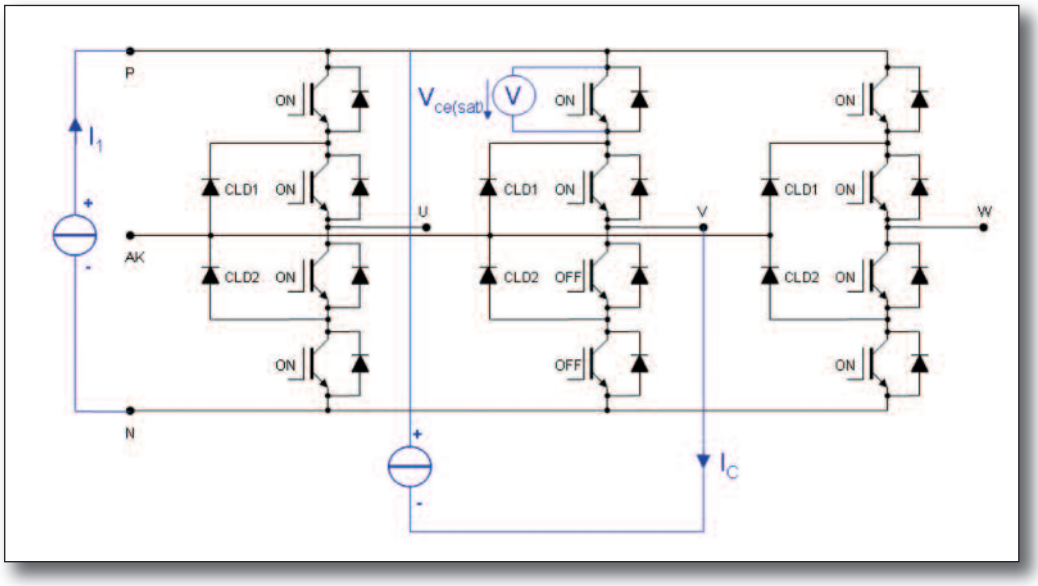


Figure 6: Test set-up to determine the thermal resistance of the DUT

actual output current polarity. In the same way, the active components and their individually imposed loss must be identified in the remaining intervals to perform a calculation over one cycle and hence getting an image of the total loss inside the module.

In reality, the voltage waveform is usually established by a PWM signal, which is adjusting the (fixed) DC-link voltage to the mean output voltage value of the switching instance by the applied duty cycle 'D'. If the thermal simulation is done in this precise way, pulse by pulse, the calculation of total loss becomes simple by summarising the loss per switching instant or pulse 'p'.

With t1=φ and t2=π , this specific calculation for T1 can be performed according to equations 1 - 5 considering P_{SS} steady state or conduction loss and P_{SW} switching loss.

1) $p = pulse$

2) $P_{T1}(p) = P_{SS\_T1}(p) + P_{SW\_T1}(p)$

3) $P_{SS\_T1}(p) = \bar{i}(p) \cdot V_{CE\_sat}(\bar{i}(p), Tj(p-1)) \cdot D(p)$

4) $P_{SW\_T1}(p) = E_{SW}(i(p), V_{cc}, R_G, Tj(p-1)) \cdot fc$

5) $\overline{P_{T1}} = \frac{1}{T}\int_{t1}^{t2} P_{T1} \cdot dt = \sum_{p(t1)}^{p(t2)} P_{T1}(p) \cdot \frac{1}{T}$

Loss calculation in PV-inverter and UPS especially for the front end portion of the UPS (3~ PFC) are quite simple because of a simplification of the interval situation. Assuming sinusoidal shape of current waveforms, the calculation can be performed according to the aforementioned equations. The correctness and the precision of such a loss calculation is checked to allow a tuning of parameters to reach a good matching between simulation and reality. Hence, a precise measurement instead of simulation of loss under realistic conditions provides the required precision for a simulation tool. For this purpose, a back-to-back configuration of inverters has been developed that is able to perform a circulation of power. Hence, the specific conditions found in PV-inverter operation and 3~ PFC operation can be created easily, helping to investigate on the thermal behaviour and evaluate the performance of two- and three-level IGBT modules.

Load generation test set-up

Before applying the realistic application conditions the setup consisting of the IGBT module and the heatsink was prepared and calibrated. For this purpose the device under test (DUT), a 75A three-level IGBT module CM75YE13-12F, has been equipped with various thermocouples mounted into the baseplate just under the specific IGBT or diode chip. Moreover, the gel has been removed from the module and the bare chips have been coated by a black varnish with known emission coefficient. Figure 5 shows the result after the coating.

In order to acquire the thermal resistance from junction to the baseplate for each chip precisely a DC current test has been performed, which is powering all available IGBTs by one current source and the DUT by a separate current source to create realistic temperature gradients in the module's baseplate. As a result of the chosen set-up, two entire legs are powered by one current source and the positive/ negative part of the leg where the DUT is located is powered separately. At the DUT, along with the precise DC current measurement, a $V_{ce(sat)}$ measurement is performed on chip level (Figure 6).

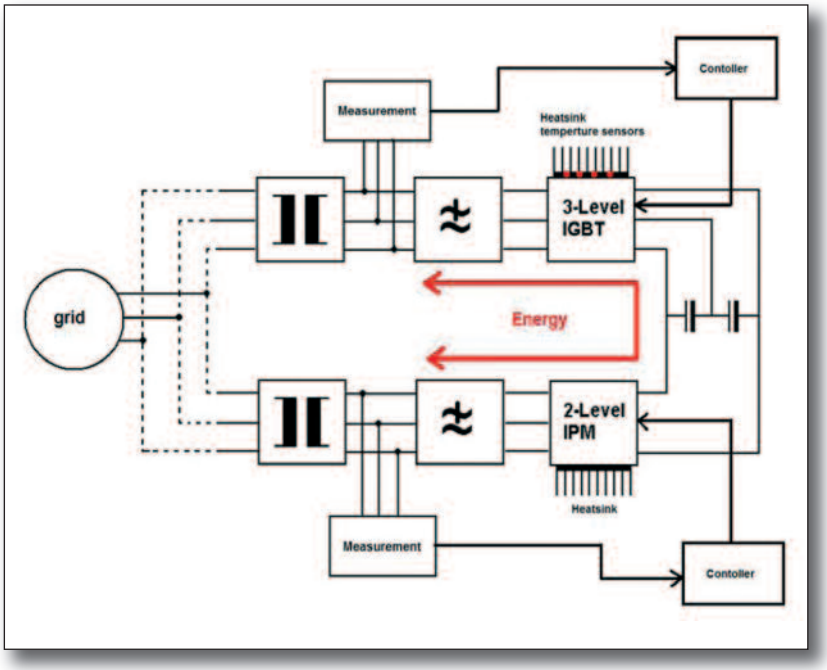


Figure 7: Thermal investigation by a set of two inverters which are circulating the power

The thermocouple touching the baseplate just under the chip and the infrared camera is observing the black painted surface of the IGBT/FwDi chip. The DC-loss of this selected operation point is well-known and the thermal resistance can be determined by linking power loss and temperature rise by means of the thermal resistance, according to the well known equation 6:

$$6)\quad P = \frac{T_j - T_c}{R_{th(j-c)}}$$

The thermal investigation has been performed by a set of two inverters which are circulating the power. Figure 7 reveals the configuration of the experimental test-bench which allows the setting up of arbitrary operation conditions for the power stage by a digital control of DC-link voltage, switching frequency load currents, PFC/ inverter mode and current phase angle. Hence, the loss distribution inside the IGBT module can be shifted and the corresponding individual chip temperature observed accordingly.

Application conditions for PV-inverters

IR images of typical operation conditions for PV- inverter, e.g. cos(φ) =1 and modulation index variation of 0.5 to 1.0, PFC operation and also mixed conditions with highly capacitive or inductive load have been tested. The case presented below shows the typical operation under PV conditions operating at the following application parameters:

- V_{CC} = 750V
- Î = 50A
- modulation ratio = 69%
- cos(φ) = 1
- f_c = 10kHz
- f_o = 50Hz
- T_f = 65°C

By the interpretation of the thermal image and considering the corresponding baseplate temperature of the chip, the power loss can be calculated according to equation 6.

From the IR image (Figure 8), the absolute temperatures can be easily read out and it becomes clear that in this operation, as already described in the power loss calculation approach, thermally the outer IGBT T1 is the bottleneck. The FWDs are not taking over any load as theoretically already understood. Hence, the colour of the IR image indicates a substrate temperature accordingly. It is remarkable that, in this operation, the clamp diode (clamp) is thermally only slightly loaded despite the small modulation index of only 0.69. With respect to PV-applications, it is an indication of a conservatively selected chip size inside this three-level IGBT module.

Furthermore, a qualitative result on the junction temperature change as a function of varying phase angle between current and voltage explains that the set-up of chip sizes inside a module can be optimised for certain operation conditions. The shift of load reflected in the thermal dissipation as a function of the cos(φ) is indicated in the IR images shown in Figure 9. For all of these tests, the amplitude of the current and the modulation index have been kept constant, but they are different compared with the previously measurement results. Referencing to the naming convention, according to Figure 2, all measurements have been taken out of leg V and D1 is the FWD to T1 and Dc1 is the CLD of the positive part of the leg.

From these images, it can be understood that the lower the cos(φ) is the lower the power loss in T1 gets. T2 shows a quite stable dissipation under all these changing conditions. However, the origin of this power loss is changing: While in the case of cos(φ) = 1 T2 is mainly heated by conduction loss, the situation at PFC operation (cos(φ) = -1) is changed to a mixture of (less) conduction loss but more switching loss.

The differences indicated as ERROR between real measurement and simulated results are very small. The results presented in Table 1 show a good match.

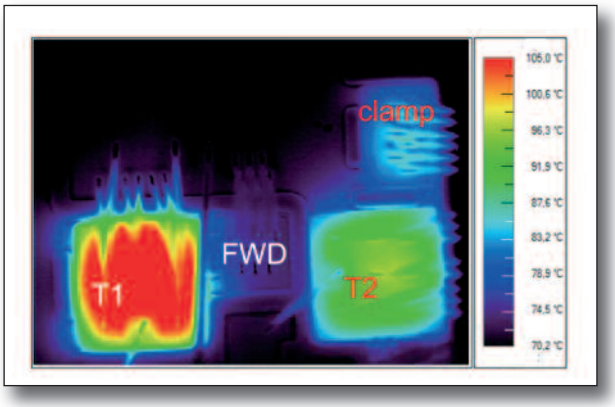


Figure 8: **IR image indicating the absolute chip temperatures**

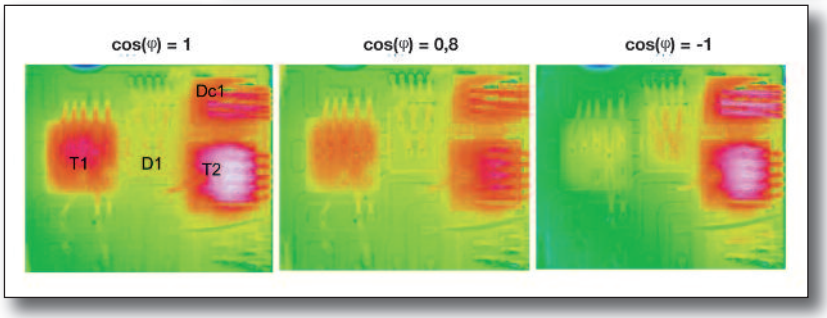


Figure 9: **Chip temperatures at cos(φ) variation**

Conclusion

The inverter and the control structure according to Figure 2 has been calibrated and successfully commissioned to generate realistic test conditions for the optimisation of two- and three-level IGBT modules. IR images and the analysis of the corresponding loss information has led to the conclusions regarding the suitability of the chip set-up of the suggested three-level IGBT module under PFC and PV-inverter operation with varying power factor. The results show the potential hotspots inside a three-level IGBT module depending on the actual load conditions and allow for optimising a loss simulation tool.

	calc.ΔT(j-c)	meas.ΔT(j-c)	Error
IGBT T1	34.4K	34.7K	0.3K
IGBT T3	20.2K	20.1K	-0.1K
FWD D4	0K	-0.4K	-0.4K
Diode CIDi	13.2K	13.0K	-0.2K

Table 1: **Temperature rise ΔT(j-c) results calculated versus measured results**

Literature

'Three-level Trench Gate IGBT modules with IGBT and their thermal analysis in UPS, PFC and PV operation modes', published at EPE 2009 - European Conference on Power Electronics and Applications, Barcelona, 8-10 September 2009