Next Generation High Performance BIGT HiPak Modules

The practical realization of the Bimode Insulated Gate Transistor (BIGT) will provide a potential solution for future high voltage applications demanding compact systems with higher power levels. In this article, we give an outlook into the new technology and the basic performance levels which could be achieved as the BIGT progresses towards the product development stage, **Arnost Kopta, Munaf Rahimo and Raffael Schnell, ABB Switzerland Ltd. Semiconductors**

The BIGT is an advanced reverse conducting IGBT device concept which mainly targets an increase in the power density levels of high voltage IGBTs for next generation power electronics systems. The new device can operate in both freewheeling diode mode and (IGBT) transistor mode by utilizing the same available silicon volume in both modes. Therefore, the BIGT targets to fully replace the state-of-the-art two-chip IGBT/diode approach with a single BIGT chip. This is achieved while also being capable of improving on the overall performance especially under hard switching conditions with low losses, soft switching characteristics and high safe operating area (SOA).

The BIGT development has resulted in a clear breakthrough in device performance by adopting an advanced shorted collector backside layout design, optimum doping profiles and controlled lifetime reduction for enabling best possible operation in both IGBT- and diode mode. In this article, we present the latest electrical and reliability results achieved by demonstrating the 3.3kV BIGT in two HiPak module footprints up to Tj=150°C.

The BIGT concept

The BIGT consists of a hybrid structure integrating an IGBT and an RC-IGBT into a single chip as shown in Figure 1. The main target of this combination is to eliminate snap-back behavior at low temperatures in the BIGT transistor on-state mode by ensuring that hole injection occurs at low voltages and currents from the P+ collector region in the IGBT section of the BIGT. The BIGT concept provides an optimum solution especially for thin devices with punch-through type buffer designs where the snapback phenomenon is pronounced in standard RC-IGBTs.

The backside layout design and dimensioning of the IGBT region is optimized to provide smooth transition into full chip conduction as the RC-IGBT section will also provide holes at higher currents maximize the RC-IGBT area for diode conduction and minimize any current non-uniformities especially during switching due to the integrated structure. Furthermore, the introduction of the IGBT will enable the RC-IGBT part layout design to be independently optimized for maximizing the diode area and ensuring that the BIGT utilizes the whole chip during transistor conduction for providing the same technology curve as for a state-of-the-art IGBT chip. The BIGT concept has resulted in a better trade-off between the above mentioned parameters compared to the standard RC-IGBT design. On the other hand, to optimize the BIGT for low dynamic and switching losses, the main challenge was to enable low diode mode recovery losses while not having a considerable effect on the transistor mode on-state losses.

A three step approach is utilized to achieve this target. The first step is the fine control of the doping profiles of the emitter P-well cells and collector P+/N+ regions. As shown in Figure 1, the Enhanced-Planar (EP) cell technology does not include any highly doped P+ well regions and also exhibits a compensation effect due to the N-enhancement layer. These two features provide the BIGT with a fine pattern P-well profile for obtaining low injection efficiency for a better diode performance while maintaining the typical low IGBT losses associated with EP designs. The second optimization step employs a Local P-well Lifetime (LpL) control technique (see Figure 1 top) utilizing a well-defined

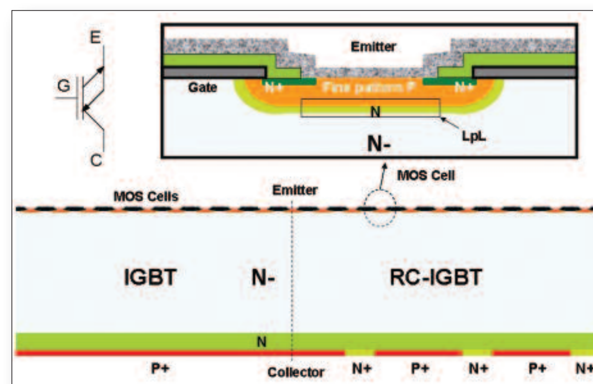

Figure 1: BIGT cross-section

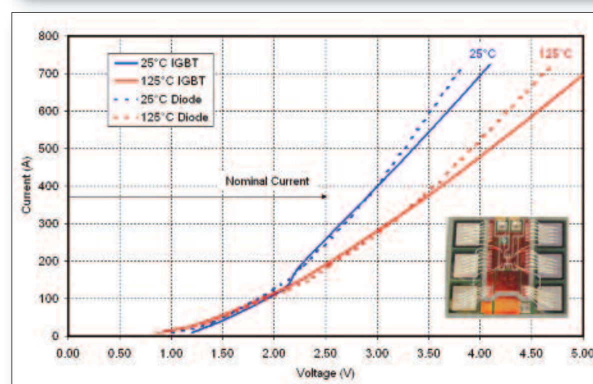

Figure 2: On-state characteristics of the 3.3kV BIGT substrate

particle implantation which further reduces the diode recovery without degrading the transistor losses and blocking characteristics. A further reduction in the reverse recovery losses is achieved with a uniform local lifetime control employing proton irradiation.

Characteristics of the 3.3kV BIGT

The BIGT technology has mainly been developed for high voltage devices. The work presented here was carried out on a 3300V/62.5A BIGT chip with an active area of approximately 1cm². High current 3.3kV HiPak1 (140 x 130mm) and HiPak2 (140 x 190mm) BIGT modules were fabricated and tested under conditions similar to those applied to state-of-the-art IGBT modules.

The BIGT advantage is demonstrated since the HiPak1 module containing 4 BIGT substrates for a total of 24 BIGT chips can practically replace the larger 1500A HiPak2 SPT+ IGBT module which normally contains 6 substrates having a total of 24 IGBTs and 12 diodes. The larger standard IGBT module has the further disadvantage of employing much less diode area which is normally a limiting factor in rectifier mode of operation and for the surge current capability. On the other hand, the larger HiPak2 BIGT module employs a total of 36 BIGT chips and its rating can potentially exceed 2000A.

Electrical characterization of the 3.3kV BIGT HiPak modules was carried out and is presented below, including static and dynamic measurements under nominal and SOA conditions. For the dynamic measurements at nominal conditions the DC-link voltage was set to 1800 V, while for SOA characterization it was increased to 2400 V. The R_{Gon} and R_{Goff} values were fixed for all dynamic tests at 1.0Ω and 1.5Ω respectively. Also, a 220nF gate-emitter

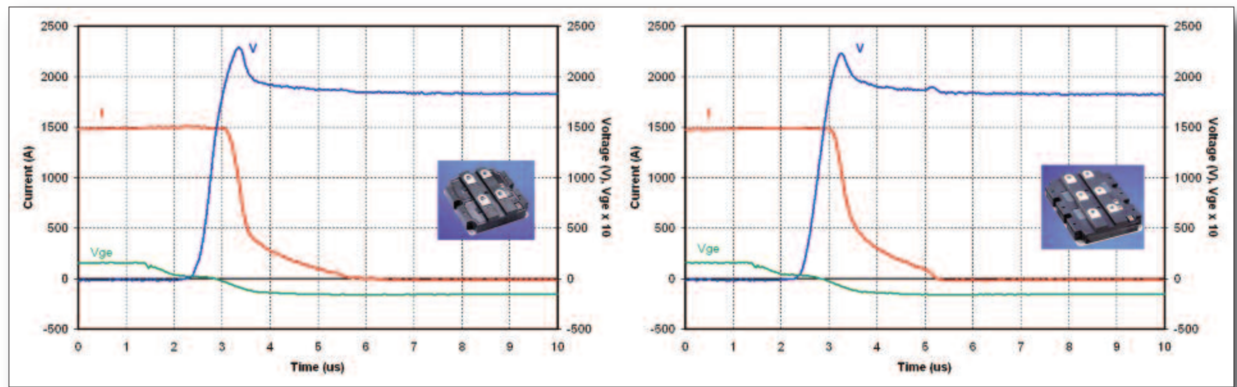

Figure 3: 3.3kV BIGT HiPak1 (left: E_{off} =2.8J) and SPT+ IGBT HiPak2 (right: E_{off} =2.7J) turn-off nominal waveforms

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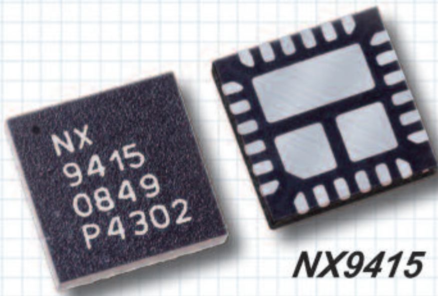

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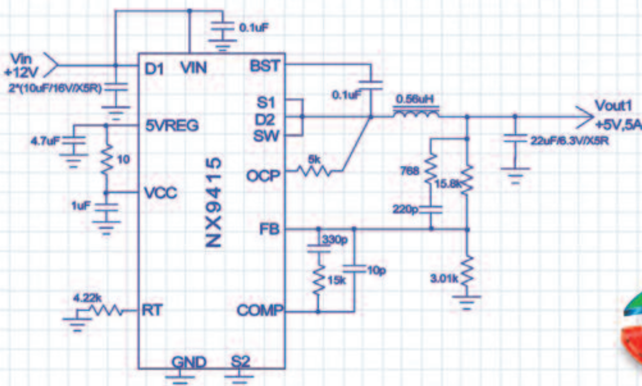

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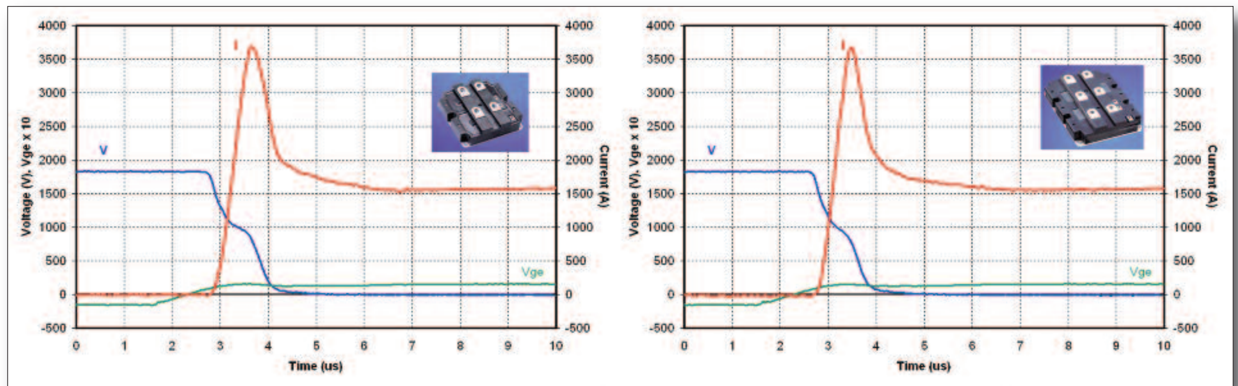

Figure 4: 3.3kV BIGT HiPak1 (left: E_{on} =2.2J/ E_{rec} =2.3J) and SPT^+ IGBT HiPak2 (right: E_{on} =1.9J E_{rec} =2.2J) turn-on nominal waveforms

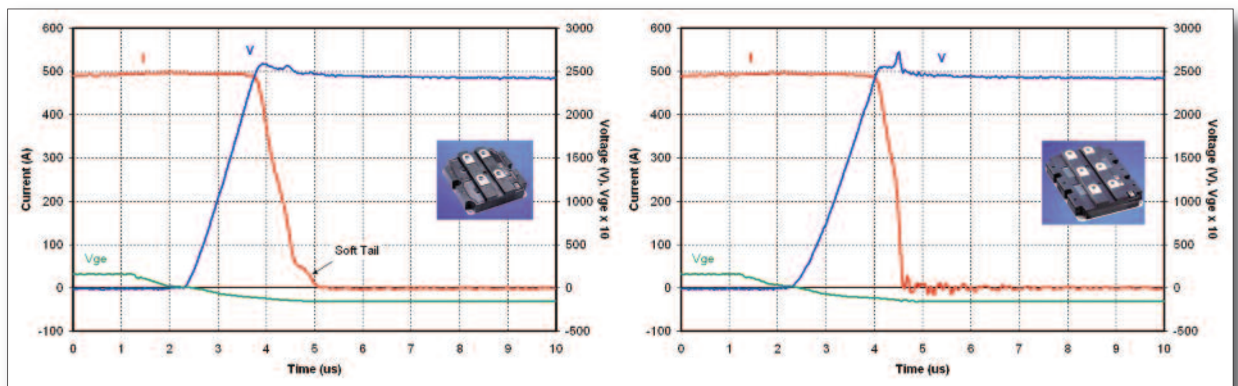

Figure 5: 3.3kV BIGT HiPak1 (left) and SPT^+ IGBT HiPak2 (right) turn-off softness

capacitance C_{ge} was employed.

The on-state characteristics of the BIGT in IGBT and diode modes are shown in Figure 2 at 25°C and 125°C. The results were obtained from the HiPak substrate test with a nominal current of 375A. For both IGBT and diode modes, an on-state of 3.5V at 125°C is shown at the nominal current. For safe paralleling of chips, the curves show a strong positive temperature coefficient even at very low currents in both modes of operation due to the optimum emitter injection efficiency and lifetime control employed in the BIGT structure.

Figures 3 and 4 show the 3.3kV HiPak1 BIGT and HiPak2 SPT^+ IGBT turn-off and turn-on waveforms respectively measured under nominal conditions (V_{DC}=1800 V, I_C=1500 A, T_j=125°C). The respective module switching losses are also indicated. The waveforms demonstrate the normal BIGT switching behavior in both IGBT and diode modes when compared to a state-of-the-art device. A similar comparison is shown for the nominal reverse recovery performance as shown in Figure 5. The di/dt during switching exceeds 6kA/μs for all tests.

Softness performance

The new BIGT technology has inherently extremely soft switching behavior in both IGBT and diode mode of operation. The optimized collector P+ doping profiles will ensure that during the turn-off tail in both modes, the passing electrons towards the N+ regions will induce a large potential across the PN junction forcing a controlled level of Charge Extraction (or hole injection) into the base.

Figure 5 demonstrates this softness during turn-off for both the BIGT HiPak1 and the SPT^+ IGBT HiPak2 modules at 500A and V_{DC}=2400V and T_j=125°C. The reverse recovery softness performance of the BIGT is also demonstrated in Figure 6 at a very low current of 50A and V_{DC}=2400V and T_j=125°C.

This feature is of particular importance for the realization of the BIGT technology since it overcomes the expected trend of reduced softness due to the non-

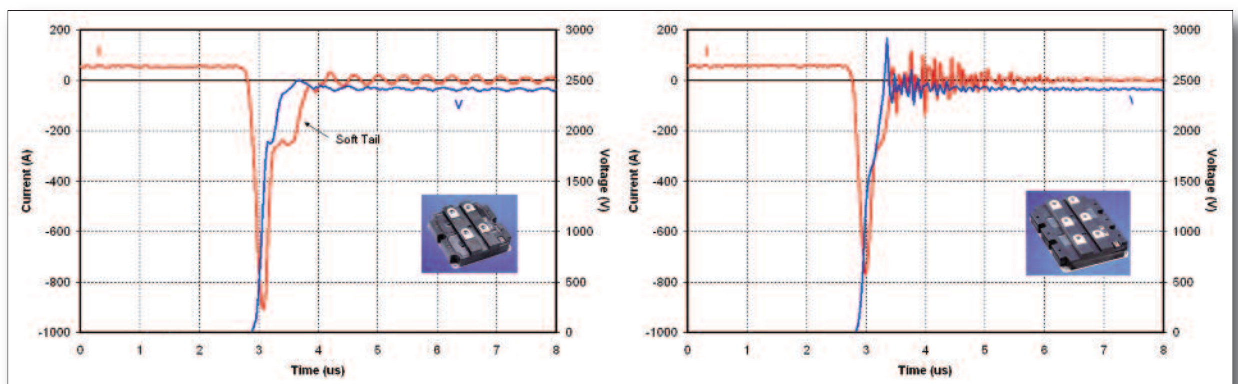

Figure 6: 3.3kV BIGT HiPak1 (Left) and SPT^+ IGBT HiPak2 (Right) reverse recovery softness

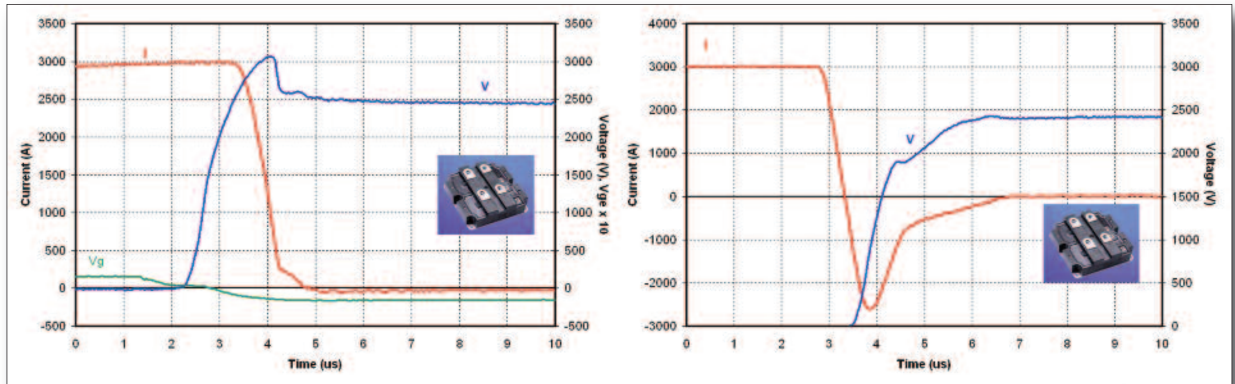

Figure 7: 3.3kV BIGT HiPak1 turn-off (left) and reverse recovery (right) SOA at 150°C (peak power = 7.9MW and 3.5MW respectively)

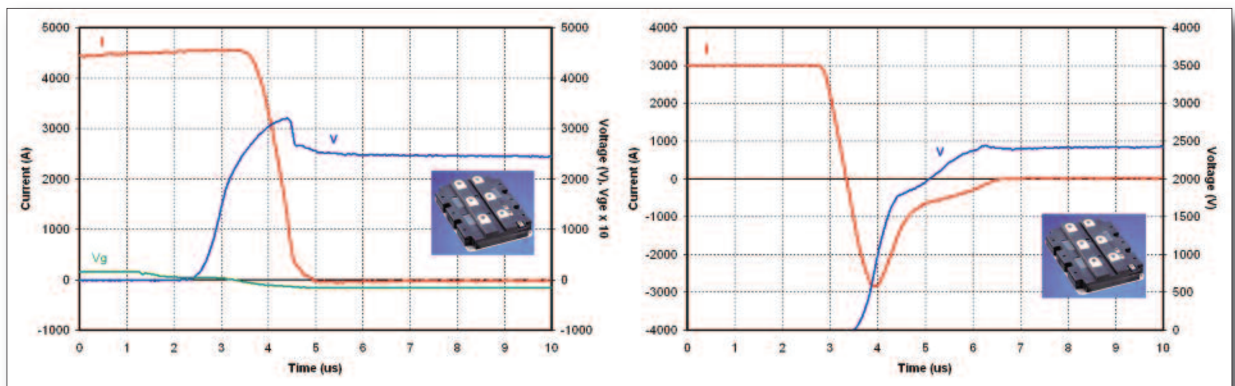

Figure 8: 3.3kV BIGT HiPak2 turn-off (left) and reverse recovery (right) SOA at 150°C (peak power = 12MW and 4.2MW respectively)

optimum silicon design of the BIGT for diode mode operation and the increase diode area provided with the new concept.

SOA performance

The SOA switching performance will be presented here at T_j=150°C to demonstrate the robustness of the BIGT modules. Figure 7 shows the turn-off waveforms at 3000A and V_{DC}= 2400V in both IGBT and diode modes.

Similar SOA tests were carried out for the larger HiPak 2 module at 4500A, V_{DC}= 2400V and 150°C as shown in Figure 8. The BIGT also shows rugged short circuit performance with an average short circuit current of 6500A when measured under these conditions.

Frequency operation and reliability testing

3.3kV HiPak1 BIGT modules were subjected for the first time to a PWM frequency test in an H-bridge configuration. The test was carried out at a maximum junction temperature of 120°C for approximately 30 minutes at three operational frequencies (500Hz, 1000Hz and 1500Hz). At a DC link voltage of 2.1kV, peak currents up to 800A were achieved during the tests. The frequency test results provide a first insight into the feasibility of a single chip operating in both IGBT and freewheeling diode modes under hard-switching conditions.

Reliability measurements were also carried out on BIGT chips. The BIGTs successfully passed the standard verification High Temperature Reverse Bias (HTRB) stress test at 2640V both at 125°C for 168 hours followed by a second run for the same chips at 150°C for a further 168 hours. In addition, the BIGT successfully passed the High Temperature Gate Bias (HTGB) test at V_{ge} = 25V at 150°C for 168 hours and a humidity (HAST) test at 125°C, V_{ge} = 25V, and V_{ce} = 80V with 85% humidity for 168 hours.

Figure 9 shows the expected output current performance for the BIGT HiPak2 module compared to today`s SPT^+ IGBT equivalent module at 125°C in both Inverter and Rectifier modes. It was assumed that an optimized chip/package layout design and loss trade-offs were employed in a fully developed BIGT module. The curves show that the diode performance is a limiting factor for the standard module approach while for the BIGT module the transistor mode defines the limit. The curves show that with BIGT technology a 25% and 38% increase in inverter and rectifier output current capability is achieved respectively. Furthermore, the BIGT technology will pave the way for future generations of IGBT based designs to provide higher power densities without any limitations imposed by the diode performance.

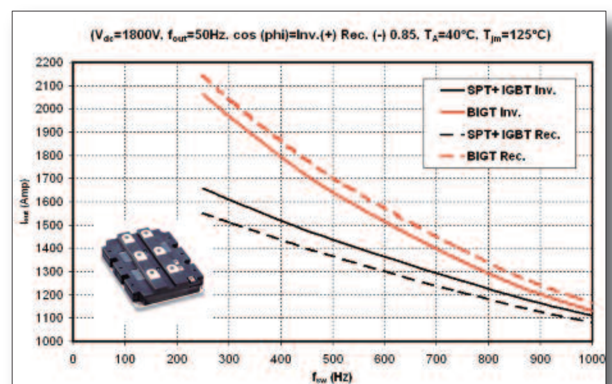

Figure 9: Output power capability of the 3.3kV SPT+ IGBT against the BIGT Hipak2 modules in both inverter and rectifier modes