Integrated FETs for Power over Ethernet

Power over Ethernet (PoE) Power Sourcing Equipment (PSE) controllers use high-voltage, high-current FETs for connecting the power source to the load. Integrating the FET reduces the space required to implement the PSE subsystem and also reduces component count. This article explains the precautions that must be taken with integrated FETs using the recently introduced Silicon Labs Si3452 PoE controller as an example.

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This controller supports four independent PoE (IEEE 802.3af) and PoE+ (IEEE 802.3at) PSE ports, offers real-time power measurement capabilities, energy-efficient powered device (PD) detection and disconnect algorithms, and low on-resistance power FETs and sense resistors. These features enable smaller, highly energy-efficient and lower-cost PoE/PoE+ Ethernet switches and midspans designed to power multi-radio wireless access points, industrial automation systems, VoIP phones, and building security and surveillance systems.

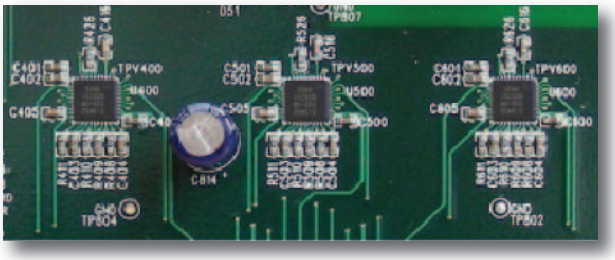

Figure 1: 12 PoE Ports with Si3452 (no backside components)

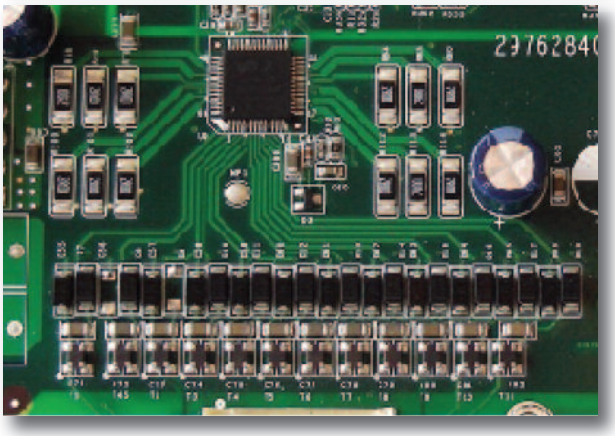

Figure 2: Representative layout of 12 ports without integrated FETs (FETs are on the backside, photo is to same scale as Figure 1)

FET current carrying requirements

With a standard TO-223 FET package and two 0805 resistors for current sensing, the external FETs use about 50mm^2 of package area per port. When the controller size is added, the package area per port is approximately 70mm^2 compared to less than 20mm^2 for a typical PoE controller with integrated FETs. Figures 1 and 2 show representative layouts for 12 port comparing the Si3452 with integrated FETs to a 12 port solution without the integrated FETs.

Some other advantages of FET integration are higher reliability due to lower component count and interconnections and guaranteed coordination with the PoE controller fault protection and current limit. When the FET is integrated, the current sense resistor is also typically integrated, which reduces noise and offset effects and typically allows the use of smaller sense resistors for less current sensing power loss. While the advantages of using the integrated FET are compelling, the reduced size means more care must be taken to avoid heating in both normal and transient conditions.

Until recently, the required power level for PoE PSE was 15.4 W. The recently adopted 802.3at amendment to the IEEE standard increases the power level to 30W for "Type 2 circuits" (cat 5E or better cable). The requirements for DC and transient current limit performance as well as typical current limits are shown in Table 1.

As can be seen, the FET must be capable of handing high DC current and high transient power conditions. These are addressed below.

DC current levels

When using integrated FETs, some care is required because, typically, four or more ports can be supported on one IC; so, I^2R losses from all ports combine.

For example, the Si3452 4 port PoE controller has a maximum combined FET and current sense resistance of 0.6Ω. In a worst-case situation, with all four ports carrying 600mA, the power dissipated is 1.2W (including V_{dd} and V_{ee} consumption). The Si3452 is packaged in a 6x6 mm QFN

Port	Power level	Voltage	Maximum DC current	Minimum current limit	Minimum current limit time	Typical current limit	Typical current limit time
Type 2	30W	50-57V	600mA	686mA	10ms	800mA	15ms
Type 1	15.4W	44-57V	350mA	400mA	50ms	425mA	60ms

Table 1: FET current carrying requirements

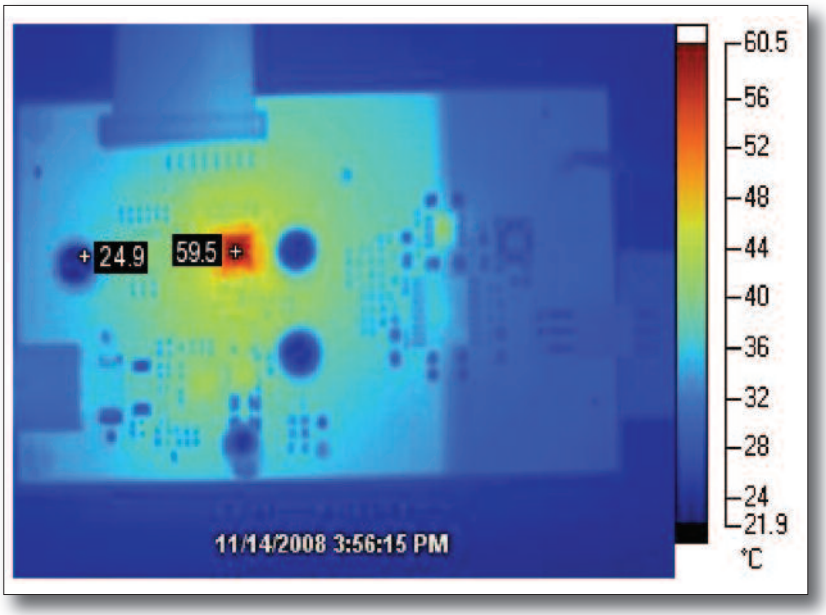

Figure 3: **Measured thermal rise of Si3452 with four ports carrying 600mA**

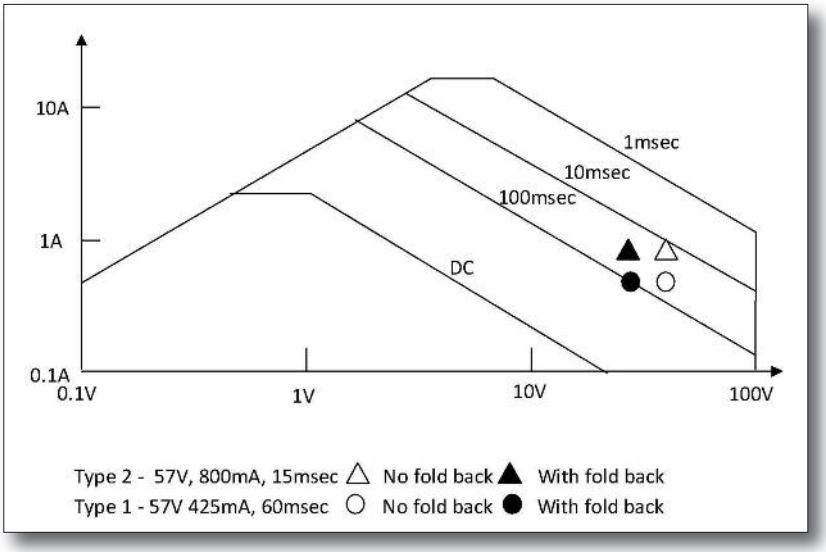

Figure 4: **Typical FET SOA curves**

with exposed pad. To dissipate this amount of heat, it is recommended that the exposed pad be connected by 25 vias to a heat spreading layer on the back of the PCB with at least 1inch^2 of copper per IC. With the recommended layout, the thermal impedance is 32°C/W with no airflow, and the worst case rise is less than 40°C. The Si3452 is rated for a junction temperature of 125°C; so, operation of 85°C is possible even without forced air cooling. Figure 3 shows the measured 34.6°C thermal rise of a Si3452 with four ports carrying the worst-case 600mA.

Transient conditions

The FET must be protected against faults and start-up transient conditions. Normally, the FET source is connected by a current sense resistor to a V_{ee} supply of as much as -57V, and the drain is clamped to ground; so, the worst case fault causes 57V of drain voltage on the FET while it is in the on state.

When using an external FET, is it not practical for the controller IC to measure the FET temperature for protection; so, the FET current limit and overload timing (TICUT) must be adjusted to fall within the safe operating area (SOA) of the FET (see Figure 4).

As can be seen, the required current limit and time is very close to the transistor SOA; so, a special technique, referred to as foldback current limiting, is employed. With the fold back current limit approach, the current limit is reduced as the FET drain voltage increases above a certain level (typically 25 V).

With the integrated FETs, it is possible to put thermal sensors close to the FET. The circuitry is arranged to turn off the FET if the thermal sensors activate, providing an additional level of safety against FET damage from fault conditions. Typically, these techniques are combined, resulting in the integrated FET being better protected against fault conditions despite the small size.

A concern with this approach is that a fault on one port might cause a thermal overload indication on another port. This is avoided by having the thermal sensors near each FET so that severe overloads are detected on a per-port basis. Overloads that are not as severe are protected by monitoring port current and shutting the port off after the required time. Combining these approaches prevents a fault on one port from affecting other ports.

Conclusion

Table 2 summarizes the issues with integrating FETs in PoE PSE controllers and the techniques for dealing with these issues in integrated FET controllers. By using the techniques described above, FETs can be safely integrated into PoE PSE controllers allowing significant savings in cost, component count and required PCB area.

Issue	Technique required
I^2R heating due to DC current on multiple ports	Use exposed pad package with multiple vias to a heat spreading plane
High current transients	Voltage foldback of current limit and thermal sensors for added safety
Faults on one port might affect another port	Place thermal sensors near FET. Monitor port current and shut port down if it is overloaded

Table 2: **Summary of issues with integrating FETs in PoE PSE controllers**