Power Module with Additional Low Inductive Current Path

Parasitic inductances are a major problem with power modules, in particular in fast switching applications. The parasitic inductance of the component interconnections causes an over-voltage condition and increases the switch-off losses in the semiconductor. Many initiatives have been investigated to reduce the parasitic inductance in power modules utilizing a complex mechanical construction of overlapping internal bus bars forming the DC path. An alternative to this approach, which is outlined within this article, is a concept using today's standard power module construction but providing an additional ultra low inductive path for the transient current. **Michael Frisch and Temesi Ernö, Vincotech Germany and Hungary**

Switching-off the IGBT results in a current change which causes an over voltage spike by the current change in the parasitic inductances according to $V_{CE(peak)} = V_{CE} + L \times di/dt$ [1]. This voltage peak at switch-off endangers the semiconductor itself which than requires a higher voltage rating of the component. Additional increased switch-off losses will be generated in the transistor according to $E_{Off} = \int V_{CE}(t) * I_C(t) * dt$. Both, the increased voltage rating and the losses will lead to higher costs for the application.

The parasitic inductance limits the maximum switching frequency at an acceptable efficiency. The voltage overshot is not only linear with the inductance but also with the switched current. This leads to the requirement of ultra low inductive designs of high power modules. For a low power application, e.g. 100A/700V (1200V component rating), an inductive loop with 10nH is acceptable. To achieve the same switching condition in a high power application, e.g. 500A/700V (1200V component rating), would require a 2nH target for the stray inductance. In contradiction to these requirements are the needs for low resistive tracks, which cause additional stray inductance by the increased mechanical dimensions of bus bars and screw contacts. As a consequence the turn-off speed for high power modules has to be reduced. This reduces the di/dt and the voltage overshot, but in consequence the switching losses are higher and the maximum PWM frequency is limited due to the losses.

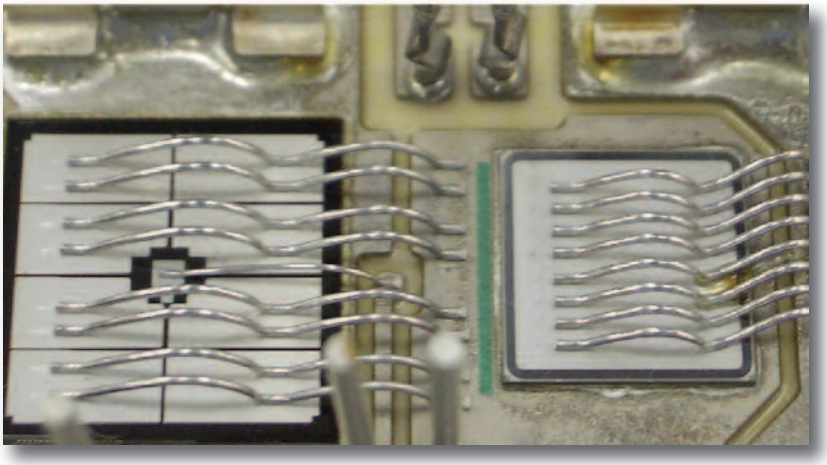


Figure 2: **Wire bonds as a source of stray inductance**

Paralleling of IGBTs

The paralleling of IGBTs is another critical issue for the design of high power modules. The largest die size of 1200V IGBTs is rated for a nominal current of 150 - 200A. For higher current rating a paralleling of the chips is necessary which produces additional challenges into the module design such as:

- Symmetrical gate drive signal
- Symmetrical static power sharing
- Symmetrical dynamical paralleling

The paralleling during switch-on and off is influenced by the chip tolerances as well as the module inductance. While the semiconductors are switching in a linear mode were the spread in the chip characteristics can cause large asymmetry of the current, this will cause of one of the IGBTs to exceed the RBSOA (Reverse biased safe operating area)[2]. The RBSOA defines the maximum current which can be switched off safely without slowing down the semiconductor or using special circuits such as active clamping, soft turn-off.

The asymmetry in the stray inductance and tolerances of the chip parameters makes it difficult to predict the current sharing during switching, so that a safe turn-off operation becomes to be a complex mission. The higher the switched current the more likely is one of the

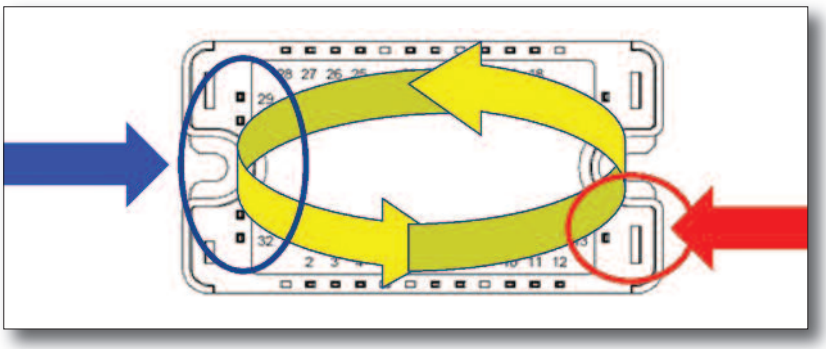


Figure 1: **Inductive loop in power modules**

individual IGBT chips be overloaded at turn-off.

Sources of parasitic inductance

Parasitic inductance appears when current encircles an area (see Figure 1). In power modules are sources which significantly effect parasitic inductance [3]:

- Wire bond: The loop of the bond wires are add to the inductance (Figure 2). A flat and short bond wire design and the paralleling of wires will reduce the negative influence of this section. A wire bond connection from the substrate to external contacts will increase the problem.
- Substrate: The power tracks on the DBC (direct bonded copper substrate) will also encircle an area but the inductance is not as high as expected. The reason for this is that the back sides of the substrates are usually covered with solid copper of the substrate and the base plate. The inductive loop will now build a transformer which is shorted on the output. The inducted eddy-current in the secondary will compensate the inductance of the primary. The remaining inductance is not that significant.
- Connection elements inside the module: Modules with multiple substrates have the need of bridges to connect the power tracks between the DBCs. The reduction of the inductance of these elements can be achieved with flat construction or with an overlapped sandwich of DC+ and DC- (see Figure 3).

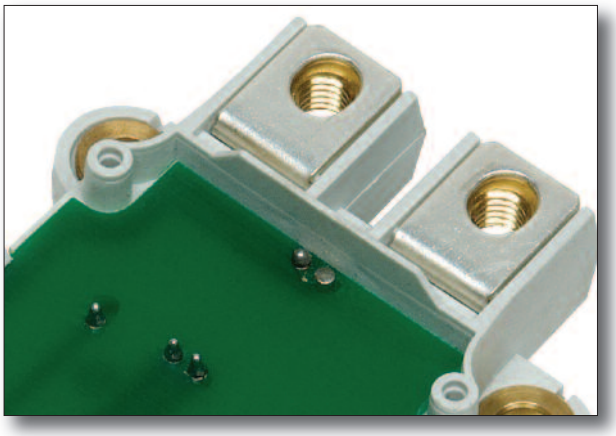


Figure 4: Power module with screw contacts

- External connection: The external connection with screw contacts (Figure 4) has some limitations. The screw system has large dimensions and it is necessary to keep certain distances between the voltage potentials to prevent sparking. With this condition the external DC interconnections have to be as close to each other as possible while still fulfilling the isolation requirements. Additional external effects might be compensated by external capacitors direct assembled on the DC-screw contacts.

The implementation of all the before mentioned actions will lead to an inductive loop between 12nH and 25nH; which is far above the required 2nH target for real fast switching.

Reduction of the switching frequency

As a consequence of this circumstances with a relative high inductive loop, is to forcing a lower switching speed. The insertion of an increased gate resistor value is the obvious method to slow down the IGBT. But the turn-off characteristic of some IGBT technologies is nearly independent from the gate resistor. The suppliers of IGBTs are answering this problem with special high power components, were the turn-off is slowed down [4]. An additional method to reduce the switching speed is the connection of a negative feedback in the gate drive circuit. The parasitic inductance of the bond wires is used to reduce the effective gate emitter voltage change at the chip (see Figure 5).

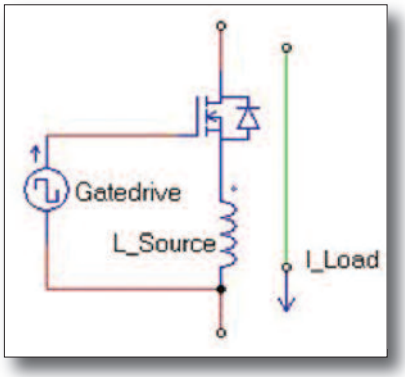
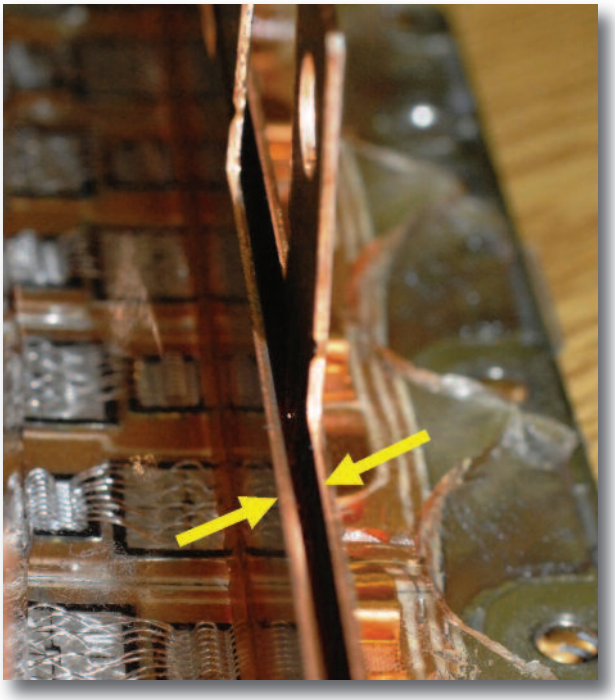


Figure 5: Parasitic inductance as a negative feedback for the gate control

Figure 3: High power module with parallel DC-bus bar



For high power applications this parasitic effect is utilized to slow down the IGBT in order to reduce the overshoot and RBSOA problem. For fast switching applications a Kelvin emitter is used (see Figure 6) to

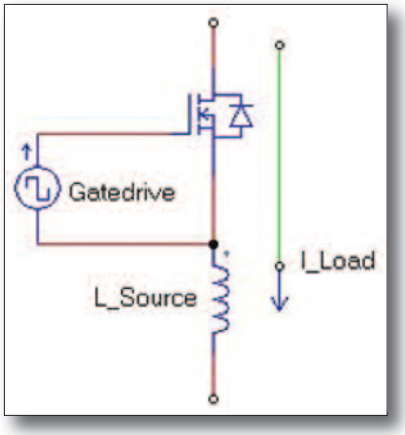


Figure 6: Gate control with current-less Kelvin contact for fast switching applications

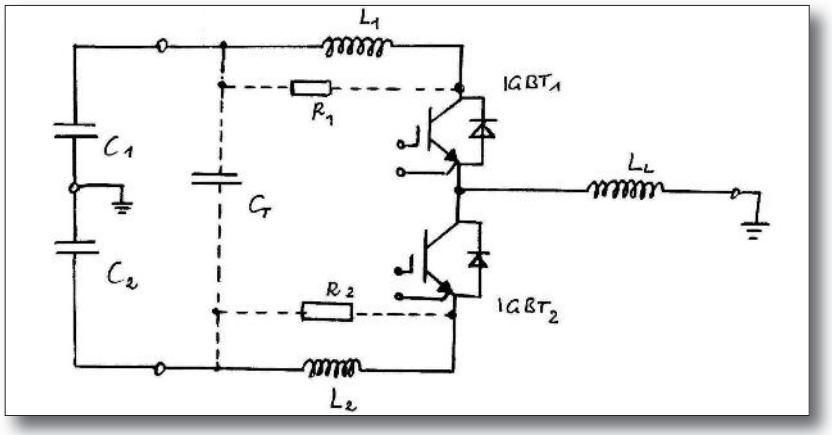


Figure 7: Concept of a power module with separated current path for continuous current (solid) and transient current (dashed)

eliminate this effect and to reduce the switching losses but here the parasitic inductance helps to keep the IGBT inside its specified conditions.

This component will additionally reduce the overshoot problem, but this in consequence leads to high switching losses because of the increased turn-off energy (E_{OFF}).

Low inductive solution for high power modules

The idea is to provide a low inductive path for the transient current during switching, while having a low resistive path for the continuous current. (see Figure 7).

The electrical connections in high power modules have to be designed for the conduction losses of the RMS current. This requirement increases the effort for a low inductive routing of the DC current, as solid copper bars have to be used to avoid over-heating. Unlike the requirements for the continuous current, the transient current path is only active during switching when di/dt is high. This is only for some hundreds of nanoseconds. Thermal issues are a minor problem for the tracks which are used only for the transient current.

The consequence is now to design a new ultra low inductive path for the transient current and use the already existing low resistive path for the continuous current. There are two directions to reduce the inductance in the transient path:

- An ultra low inductive path with overlapped tracks (e.g. on PCB, capacitor foil etc.).
- Paralleling of many connections to achieve the low inductance as a result of a conclusive paralleling (best is a pinning with alternating DC voltage polarity close to each other).

A module concept is developed based on a standard flowSCREW package. The transient current path is defined as PCB-bridges between the DCB-substrates (see Figures 8 and 9).

The DC-tracks in the transient path are routed totally overlapped. This means every DC+ voltage track is overlaid with a DC- track on a second layer. The small adapter PCBs are soldered into the main PCB with PCB fingers into complementary holes. Here, a certain distance is required to keep the clearance and creepage distances between DC+ and DC- fingers. Such a distance would cause parasitic inductance if no action is taken for

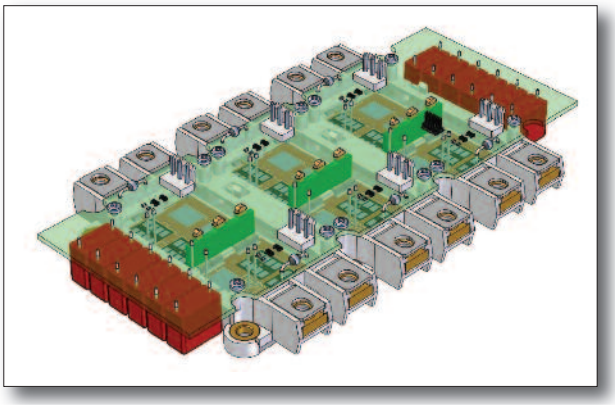
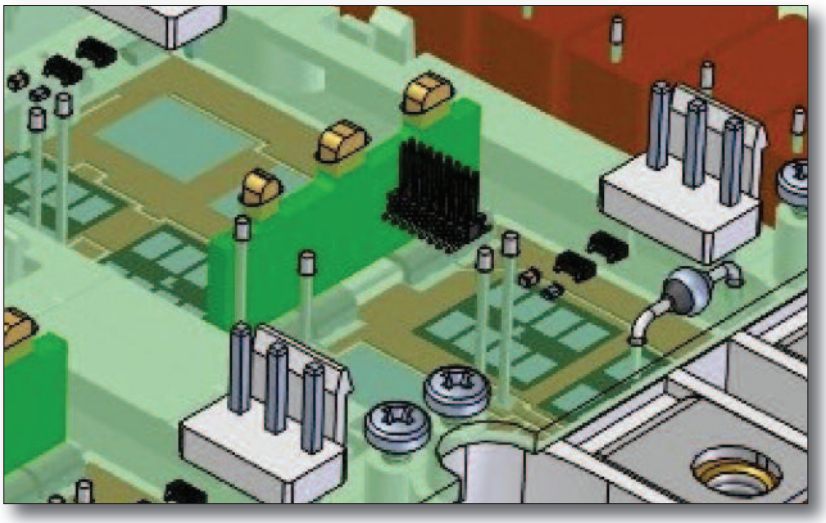


Figure 8: **Module concept based on the flowSCREW2 package with low inductive PCB bridges**

BELOW Figure 9: **PCB bridge in detail**



compensation. The current will take a separate path in the finger, making it impossible to compensate the magnetic field with the working current. But inside of the finger the opposite voltage potential is routed (in the DC- finger there are inside DC+ layers) which ensures the system to store a smaller electrical energy in the connection stray inductances. The transient DC path is routed to foil capacitors with total 1,2_F on the main PCB. For a better utilization of the capacitors all three half bridges are connected to the same DC capacitors.

Measurement and simulation

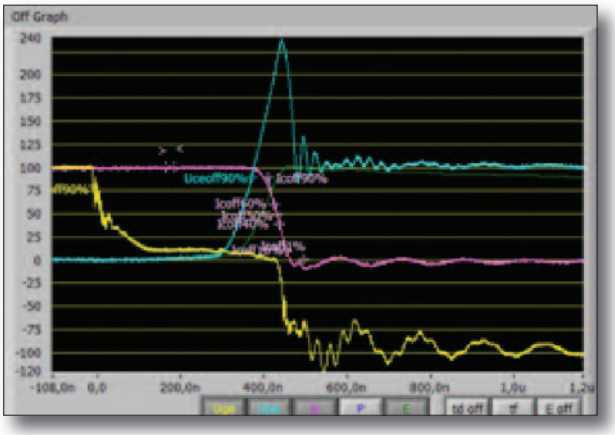
The investigation starts with the analysis of the performance of actual power modules. It is important to find out how the inductance of the package is limiting the usage of fast components in high power applications. As an example the voltage overshoot of a 600V trench field-stop IGBT in a flowSCREW2 package is shown here (see Figure 10). In this module are two 600V/200A IGBTs paralleled to a 400A half bridge topology.

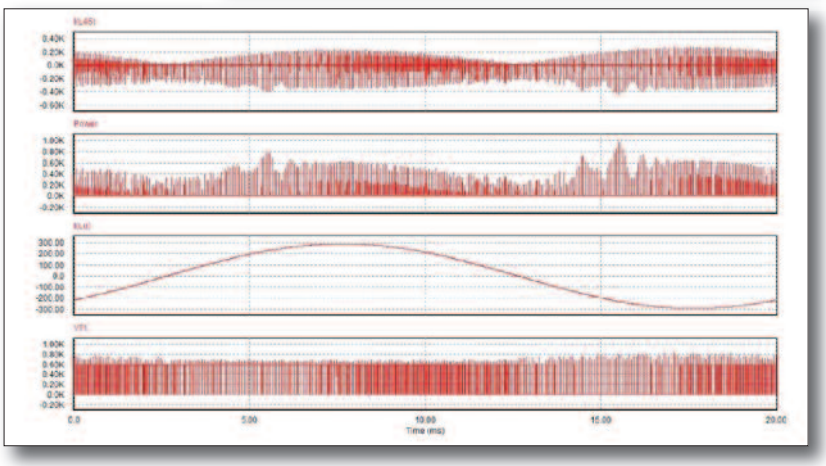
The parasitic inductance results to ca. 22nH. In this value the external DC-bus connection is included. The inductance causes at 700A (25°C) an overshot of already 370V. The DC-voltage in this test was reduced to 300V but it still exceeded the maximum voltage rating of the IGBT.

The next step is a model with the parasitic inductance of the module (too complex to show here).

Figure 10: **Turn-off characteristics of a fast switching IGBT in the flowSCREW2 package without low inductive feature**

BELOW Figure 11: **Simulation result - module with transient current path**





For a prediction of the improvement of a transient current path we add this design concept feature to the model and perform a simulation of the current, voltage and power values at the semiconductor (Figure 11).

Verification of low inductive current path

Samples of power modules are built (Figure 12) and equipped with the low inductive PCB bridges. The modules are tested in order to verify the expected behavior with an inductance measurement and the detection of the voltage overshoot of fast switching IGBTs.

The comparison with the standard module will show the effectiveness of the new module concept. Two different tests are defined to verify the effectiveness of the new solution:

- The module with low inductive current path is connected to the DC-link with ca. 9nH inductance in the DC-bus.
- The on-board capacitors on the PCB board are connected to the module.

The IGBT were switched off with 350V and a current of 720A (25°C). The voltage overshoot is 250V. The inductance of the transient current path is 16nH. In this value the 9nH of the external DC-bus connection have been included, the high frequency on-board

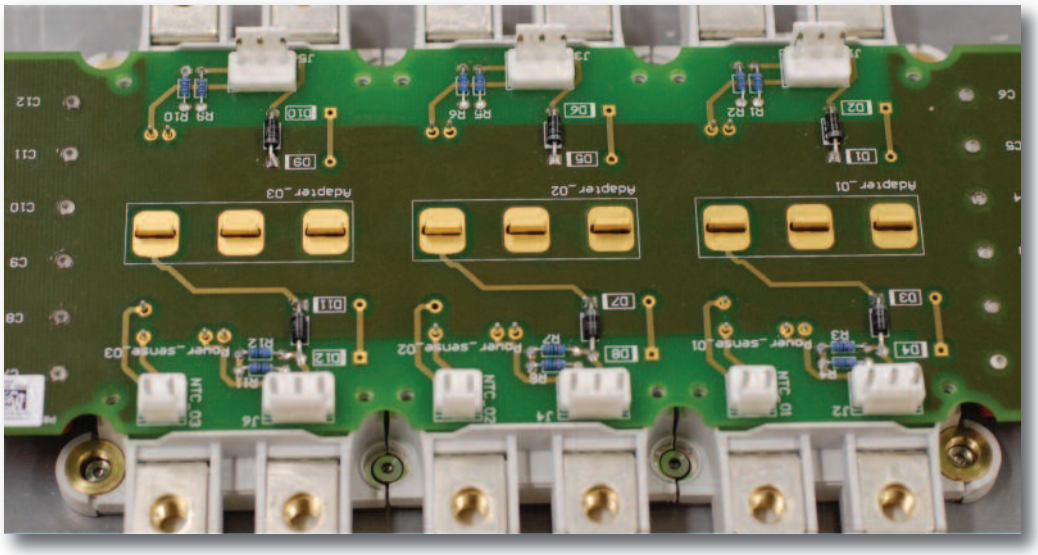


Figure 12: **Three halfbridges are low inductive connected to high frequency DC-capacitors in this test sample**

capacitors were not connected in this test. The comparison between the standard and the new solution are confirming the expectation into the new approach. The low inductive solution reduces the voltage overshoot from 350V (at 700A) to 250V (at 720A). This opens the opportunity to increase the DC-link voltage up to 350V.

With the on-board capacitors implemented, the inductance of the transient path is reduced to 7nH, which does not include the internal inductance of the on-board capacitors. The voltage overshot results to 190V at 720A (25°C) which lead to a maximum DC voltage of >400V (Figure 13). It is possible to reduce the inductance to ca 5nH, when the screw contacts are also connected to fast capacitors in parallel.

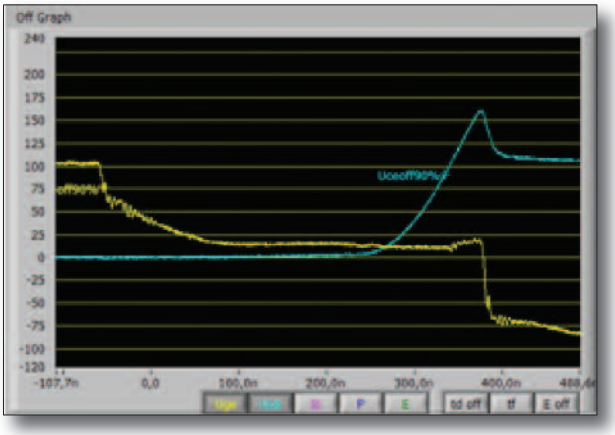


Figure 13: **Turn-off characteristics of a IGBT in the flowSCREW2 package with low inductive current and on-board capacitors**

The next approach is the paralleling of low inductive paths for the transient current. With this technique it is possible to reduce the inductance to a minimum and it offers the possibility to create low inductive paths for each individual IGBT chip. In this case, the current sharing during turn-off is closed to the static value of the paralleled components. This will open the door for new fast switching high-power applications.

Possible solutions with low inductive current path

The separation of the current paths for a low resistive and low inductive path opens the field for new fast high power module topologies:

- Fast switching high power applications: An increased switching frequency for high power applications is the key for size and weight reduction of such systems.
- High power NPC inverter [5]: The new low inductive approach might be a valuable strategy for neutral point clamped inverters (NPC-Inverters). NPC- or 3-level inverters have three DC voltage potentials. In such applications a low inductance between all DC voltages is required. A high inductance in the DC-loop will kill the reduction of switching losses in this topology.
- Matrix Inverter [6]: At most applications a low inductive connection with the DC voltage will solve the overshoot problems, but in more complex topologies as matrix inverter circuits, there is no DC voltage available and the requirements become more ambitious. Here the low inductive connections between all the switches and all the three inputs and the three output terminals are required.

Conclusions

Parasitic inductance in power modules is a burden especially for high power applications. It limits the switching frequency and the overvoltage generates problems with reliability (RBSOA) of the inverter system. The first results of the new idea to separate the current paths into a static low resistive screw contact and in a transient low inductive PCB-based connection are promising. The limit for reduction of stray inductance is not yet reached. The new solution is a new milestone for low inductive high power module technology. The 2nH target turns from an imaginary target into a realistic one.

Literature

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