Cutting Vehicle Emissions with Advanced Power Electronics

As car designers seek greater fuel efficiency to meet ambitious government-imposed emissions targets, improvements in power electronics and packaging technology can help to increase the number of kilometres travelled in exchange for the CO_2 emitted. **Benjamin Jackson and Shishir Rai, Product Management Automotive MOSFETs, International Rectifier Corp., El Segundo, USA**

Governments have identified reducing CO_2 emissions from cars as a major component of efforts to reduce greenhouse gas emissions under obligations such as the Kyoto protocol. In the EU, for example, some 20% of overall CO_2 emissions are attributed to road transport and a reduction strategy is now in place aiming to reduce average CO_2 emissions from new cars to 120 grams per kilometre by 2012. Although this target is not likely to be met on time, average new car emissions have fallen considerably and the European Commission is about to assess the feasibility of a new proposal from the European Parliament to reach 70g CO_2/km by 2025.

Electrifying the common car

With this increasing focus on emissions, fuel efficiency is growing in importance to car designers. In addition to improving aspects such as engine design and fuel management, components including power steering systems, water pumps and cooling fans have transitioned from being driven by the engine to become fully electric units. This has removed mechanical loads that sap the engine's power, and has also reduced the overall weight of the vehicle, delivering a net improvement in fuel efficiency.

Electrical systems are even more pervasive in hybrid-electric vehicles. A number of architectures are in use; a common arrangement places a motor/generator in the powertrain between the internal combustion engine and the gearbox. The motor/generator works with the engine to assist acceleration, is capable of propelling the car on battery power alone with the engine turned off, and is also able to recover kinetic energy normally lost during braking. An increasing variety of hybrid vehicles are now available, from ultra-economical small cars to high-performance vehicles capable of out-accelerating a conventional equivalent while returning around 20% better fuel economy.

The ultimate destination, of course, is for the car to have full electric drive. The first generations of such vehicles for public consumption are being introduced to markets now.

In cars with hybrid or fully electric propulsion, large electric drives are needed for the propulsion system, but the demands for equipment such as electric power steering and various body and interior equipment like windscreen wipers, mirror and seat adjusters, and HVAC controls will continue. Since conserving battery energy is crucially important, to maximise the travelling range of the vehicle, all of these drives and power-conversion systems must be extremely efficient.

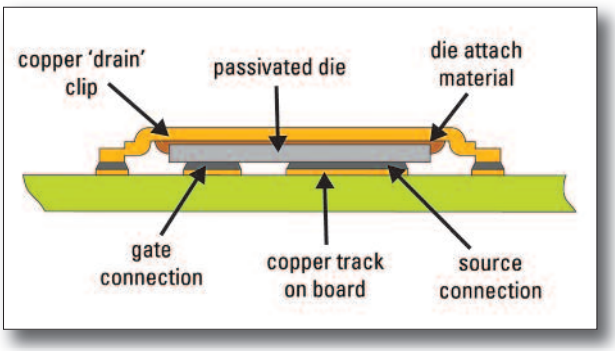

Figure 1: Cross-section of a generic DirectFET device

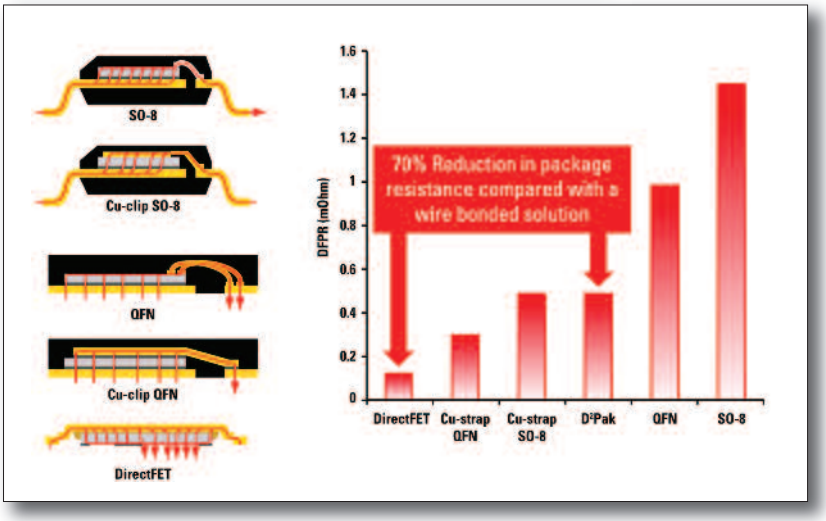

Figure 2: Comparison of package die-free package resistances (DFPR)

Efficient power semiconductors

Engineers designing drives for automotive applications must not only choose the most power-efficient topology for the drive, but also need to consider the properties of the power electronic components selected; in particular, the electrical losses incurred in the power MOSFETs used in the various bridge drivers, inverters and general power-switching functions throughout the vehicle's electrical infrastructure.

Manufacturers of power MOSFETs have made great strides in optimising the performance of the chip, to minimise both on-state resistance as well as losses during turn-on and turn-off. These conduction and switching losses are the two dominant loss mechanisms in a power MOSFET die, and

are usually interdependent: optimising the device for low conduction losses tends to sacrifice some switching performance, and vice versa. For this reason, a number of device types are available, allowing designers to prioritise low conduction loss where the MOSFET will have a high duty cycle or alternatively low switching loss in situations where fast switching is needed, or to choose a device offering a balance of both properties for general-purpose applications.

Another major component of losses in power devices is concerned with the electrical connections between the MOSFET die and the external terminals. The properties of these connections - particularly those to the source and drain, which carry the load current - are critical in determining the MOSFET's performance. Ideally, a metallic connection of large cross-sectional area is desirable. This effectively minimises the resistance of the connection and helps achieve a low value of Die-Free Package Resistance (DFPR), which defines the resistance which the package contributes to the on-resitance of the device.

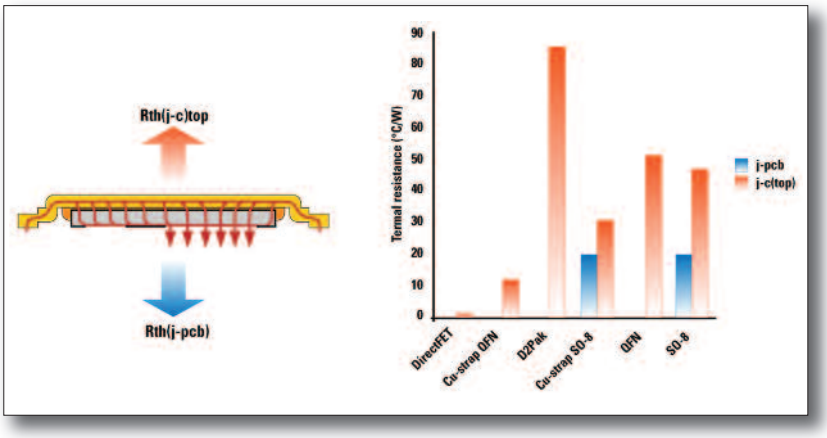

Figure 3: **Advantage of double-sided cooling**

Increasing the cross-sectional area of the connections also reduces the associated inductance, which increases efficiency, reduces heat generation and improves switching performance.

A large number of power package variants have been developed, particularly since the advent of surface-mount technology, aiming to increase the conductivity of these connections so as to improve both the efficiency and current rating of the device.

By optimising the silicon for low on-state resistance and ensuring the package has a low DFPR, the device designer can achieve a power MOSFET offering low overall on-state resistance, or $R_{DS(ON)}$.

Improving package design

Traditionally, wire bonding has been the dominant technique for connecting the die to the package terminals. Bondwires are inexpensive and straightforward to implement by bonding directly to the top metal of the die. However, each individual wire has a small cross-sectional area, which imposes parasitic resistance and inductance. To combat these effects and achieve the desired current-carrying capability, multiple bondwires must often be connected in parallel. Increasing the

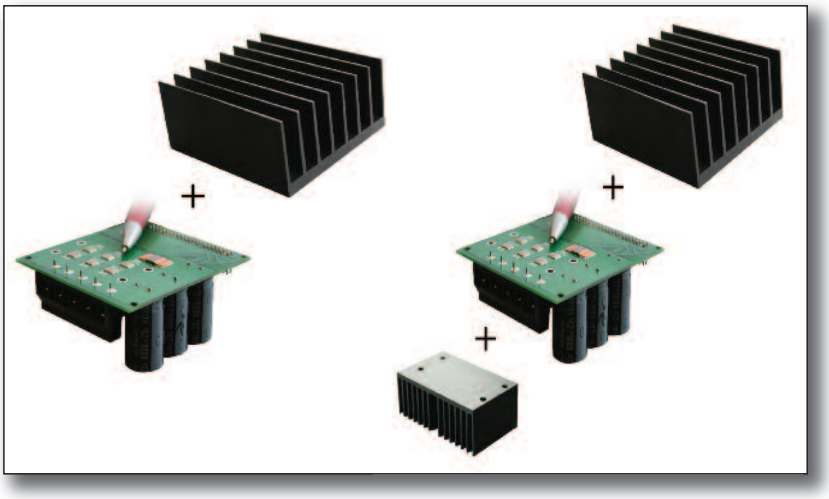

Figure 4: Bottom side of DirectFET inverter board and the heatsink (left) and additional heatsink for dual sided cooling (right)

number of individual connections however, also reduces the reliability of the device. A further disadvantage is that the bondwires on the top surface of the die prevent the use of other packaging techniques for removing heat directly through the upper surface of the package. However, cooling through the PCB becomes impractical in high-power applications. A complicated and costly mechanical attachment to a chassis or heatsink is then required. For these reasons, it can be argued that bondwire technology is one of the biggest roadblocks to improving both the thermal and electrical performance of power semiconductor packaging.

International Rectifier's DirectFET® technology eliminates bond wires from power MOSFET packaging altogether. The MOSFET die is fabricated with a solderable front metal finish in conjunction with a proprietary passivation system, which produces large gate and source contacts on one surface of the die and a large drain connection on the backside. The die is flipped, which exposes the gate and source metallisation on the underside of the package. These are then soldered directly to the PCB. A copper can is attached to the drain connection on the top-side of the flipped die. The can covers the entire upper surface area of the die, and is then brought down to create coplanar drain connections at the level of the PCB. Die-attach adhesive secures the die inside the can. Figure 1 illustrates the cross-section of a generic DirectFET device.

Eliminating the wirebonds also improves the DFPR to 150µΩ, which is insignificant compared to the on-resistance of the MOSFET die. Figure 2 compares the DirectFET DFPR with typical figures for legacy power packages, showing at least 70% improvement over the wire-bonded D2PAK package.

Furthermore, the DirectFET can is conductive and is equivalent of a 7oz PCB trace. This feature enables novel layouts of the power section in inverter and DC/DC converter, where the can itself acts as a busbar or PCB trace thereby saving PCB space and reducing PCB I^2R losses.

In addition to eliminating package resistance associated with a conventional leadframe and wirebonds, DirectFET also eliminates plastic packaging materials, which have poor thermal conductivity. The large copper drain connection also provides an alternate path for heat dissipation and an efficient thermal interface to an external heatsink. With effective cooling of both the top and bottom sides of the package, DirectFET significantly reduces thermal resistance compared to other power packages, as Figure 3 illustrates.

A further advantage of the DirectFET package is that the die utilizes a high percentage of the package PCB footprint. This allows a larger silicon die to fit in a much smaller DirectFET package enabling lower on-state resistance and higher power densities. By significantly reducing electrical losses, physical size and weight while allowing simpler mechanical assemblies, DirectFET delivers many advantages for designers of automotive equipment.

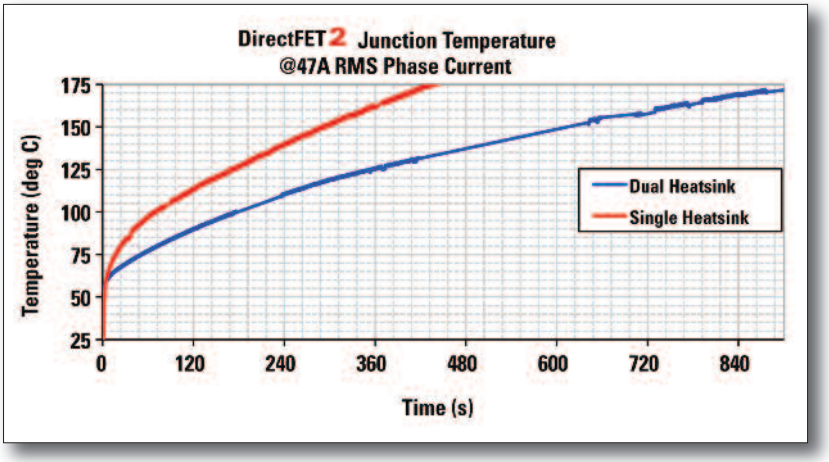

Figure 5: Comparison of single- and double-sided cooling performance

Automotive DirectFET in practice

To conclude with a practical example, Figure 4 shows a three-phase inverter board built using AUIRF7736M2 40V 3mΩ max. DirectFET power MOSFETs. The board has two layers of 71µm thick copper trace and measures 77mm x 83mm with all six DirectFETs fitting in an area of only 17mm x 47mm. At room temperature, the board can be operated at $40A_{RMS}$ continuously or at $50A_{RMS}$ for 5 minutes from a nominal 13V battery voltage. This performance is achieved with a single heatsink in contact with the DirectFETs as illustrated on the left hand side of Figure 4.

When a second heatsink is attached on the top side of the board (as illustrated on the right hand side of Figure 4) it allows the heat to spread evenly between the heatsinks resulting in a reduction in maximum junction temperature of the DirectFETs. When the board was operated at $47A_{RMS}$ with and without the top heatsink, it was found that that after 6 minutes of continuous operation the junction temperature of the DirectFETs was 35°C cooler when the top heatsink was attached. The graph of Figure 5 compares the die temperature with single- and double-sided cooling.

DirectFETs thus enable compact designs and offer the flexibility to cool the package from both sides. This results in maximizing the performance in a smaller space while also improving reliability by reducing the die temperature, thereby accomplishing more from less.

Literature

"Power Density and Performance Improvement of New Automotive Power Semiconductor Packages", Power Electronics Europe 1/2010, pages 20 - 22