Past, Present and Future of HPT-IGCT

The integrated gate-commutated thyristor (HPT-IGCT) is a state-of-the-art bipolar turn-off device for high power applications. New devices employing this technology have been released during the past few years and in this article we take a look at the newest member in ABB's product portfolio - the 5.5 kV asymmetric HPT-IGCT. The development of the HPT-IGCT continues, however, and in this article we will also take a look at one interesting device in the pipeline. **Tobias Wikström and Björn Backlund, ABB Switzerland Ltd, Semiconductors**

The IGCT was introduced about 15 years ago and has established itself as a preferred technology for handling very high power. The applications range from industrial drives and track-side supplies to power quality and high-current breakers. The IGCT is available as reverse conducting devices with an integrated free-wheeling diode and as asymmetric devices. The first devices, as well as most devices made today, use a flat p-base but a new family of devices, referred to as HPT-IGCT, using a corrugated p-base, has been developed recently.

IGCT basics

The first device in the HPT-IGCT family was the asymmetric 4500 V device 5SHY 55L4500 released in 2009. In 2010, 5SHY 42L6500 followed, an asymmetric 6500 V device and in 2012, yet another asymmetric device 5SHY 50L5500 rated 5500 V was released. All these devices use the same package (see Figure 1) with a copper pole piece diameter of 85 mm.

The main strengths of the device lie in its thyristor-like on-state with maximal possibilities for engineering the on-state plasma distribution for optimal trade-off between on-state and turn-off losses, its rugged mechanical design and good thermal coupling to the cooler. Two disadvantages of the IGCT compared to the IGBT, the only competitor device in the power range of the IGCT, is the relatively large effort needed to control the device -

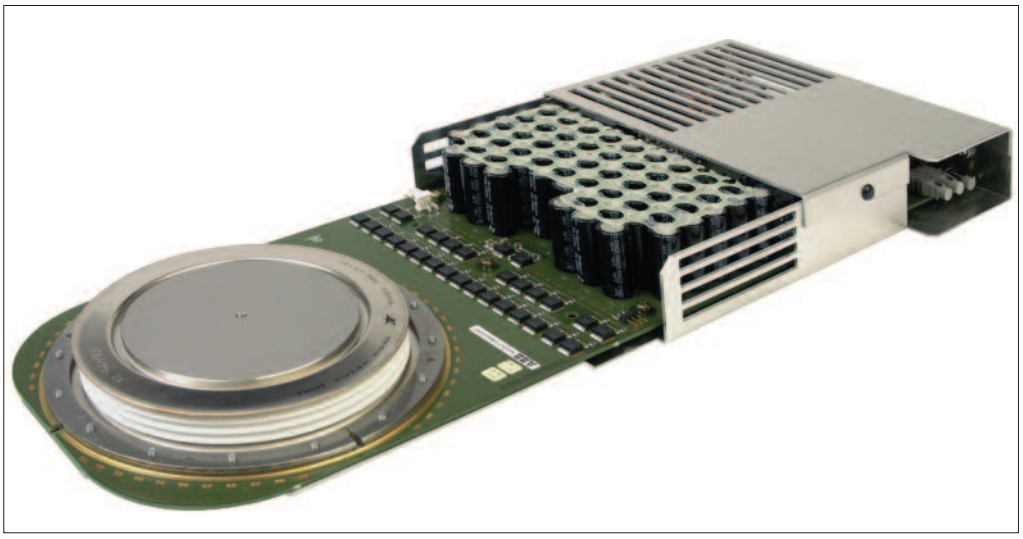

Figure 1: The HPT-IGCT, consisting of the silicon switch in a hermetic ceramic housing on the left, closely coupled to the gate driving circuit on the right

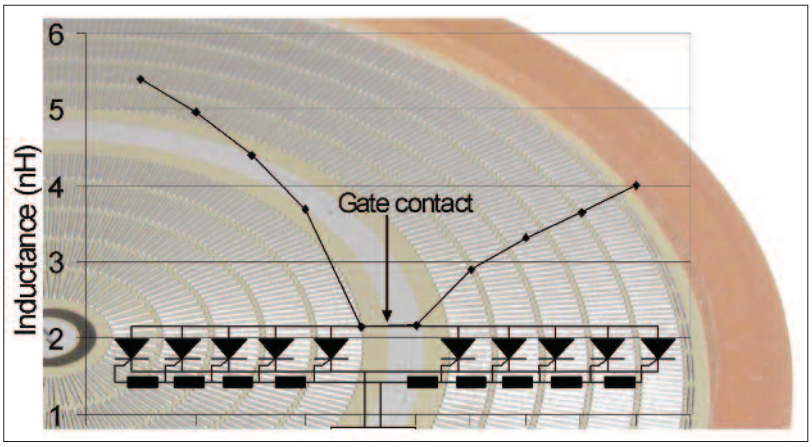

Figure 2: Inductive situation (simulated values) of the individual segment rings on an IGCT wafer showing how inductances can be distributed over the wafer. The rings far away from the gate contact are more heavily loaded by inductance than the rings in the vicinity. Hence, the gate signal will propagate at some finite speed and disfavor the gate-remote regions

tens of Watts for a 3.6kA device - as well as the inability to control the anode voltage during turn-on. The former is due to the fact that it is a current-controlled device. The latter is due to it being a thyristor and, as such, it is either off or on and the transition between those states is only stable in theory. Hence, implementing it in most common inverter topologies means protecting the antiparallel diode at turn-on. Nevertheless, thanks to its low losses and efficient cooling, it is and continues to be the preferred choice for many manufacturers of very large power inverters. Other requirements for applications such as breakers for large currents can only be met using the low on-state of the IGCT.

The maximum controllable current (MCC) of the IGCT does not scale linearly with device area. The reason is the inductive (and resistive) coupling to areas remotely placed from the gate contact. The area scales with the square of the diameter, whereas the MCC merely scales linearly, using the same technology. A graphical summary of this situation is presented in Figure 2. The technology can be improved by decreasing the total inductance in the package (i.e. the minimum, 2 nH, in Figure 2.), improving the local ruggedness to facilitate more current redistribution and increasing the driving gate voltage. The high-power technology was built using the first two.

High power design elements

The enablers for very high current turn-off are a combination of improving the local ruggedness of the silicon device itself by employing p-base corrugation, and increasing the gate's reach by minimizing the impedance, mostly in the gate driver circuit itself.

Finding the optimum for the p-base corrugation used for improving local ruggedness means trading off many parameters, such as blocking capability, thermal budget, process limitations and ruggedness. In general, the higher the device voltage, the deeper and more highly doped the p-base has to be made.

The improvements to the gate unit include improved lifetime of the capacitors used, using a 6- instead of 4-layered PCB substrate, increasing the parallel connection of the turn-off channel by increasing the number of MOSFET switches and capacitors, as well as optimizing the layout of the components on the gate unit. With careful selection of the used components, it is also possible to reduce the losses in the gate unit.

A further improvement to the gate unit is the possibility to equip the IGCT with an anode-voltage sensor feature to improve the applicability of the device, facilitating early error detection.

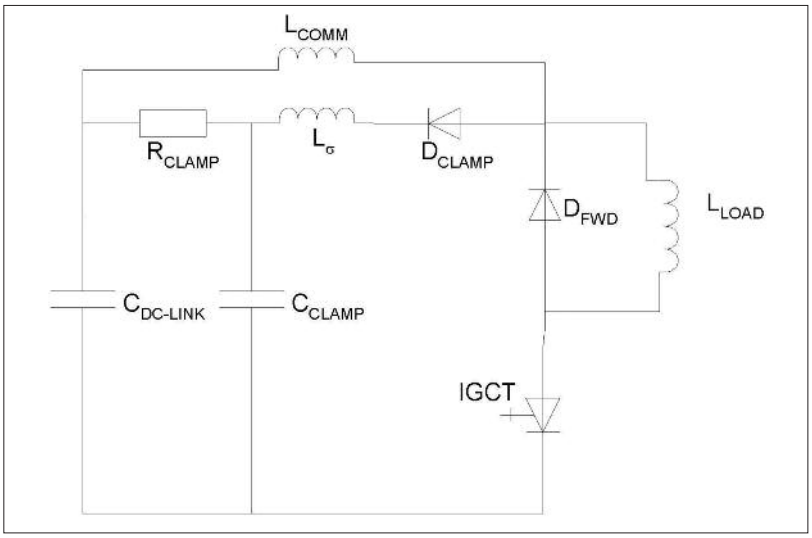

Figure 3: Circuit used in dynamic testing of the IGCTs (parameters: C_{CLAMP} = 8μF, L_σ = 300nH, R_{CLAMP} = 0.6 Ω, L_{COMM} = 6 μH)

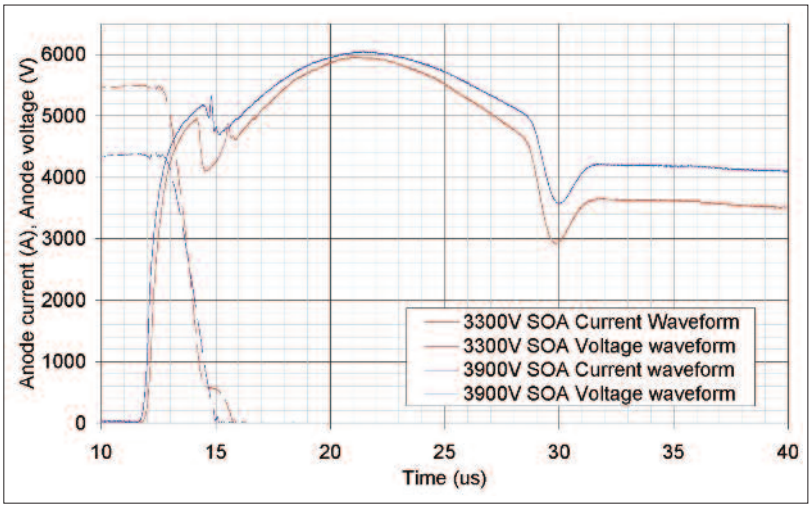

Figure 4: Current handling capability of the 5.5 kV HPT IGCT. At 3.3 kV DC-link voltage, more than 5.5 kV can be controlled (device testing stopped without destruction). At 3.9 kV, the tests stopped at around 4.4 kA, as the over-voltages involved exceed 6 kV, and hence the specified device capability by more than 500 V

The IGCT technology can utilize all commonly used lifetime adjustment techniques. Using electron irradiation, proton irradiation, or both, one can tailor the electron-hole plasma distribution to the best shape and tune the trade-off between static and dynamic losses to the best fit for the application. Thanks to the vast surplus of charge in the on-state, lifetime attenuating techniques can be utilized within a broad range. The 5.5kV device was designed using electrons and proton irradiation from the anode side, which significantly reduces the overall losses.

5500 V device capabilities

Dynamic electrical testing was carried out in a circuit displayed in Figure 3. The clamp circuit used to protect the freewheeling diode is close to the application and facilitates rapid and reliable testing, as opposed to measuring replicas of inverters.

Safe operating area (SOA) and losses

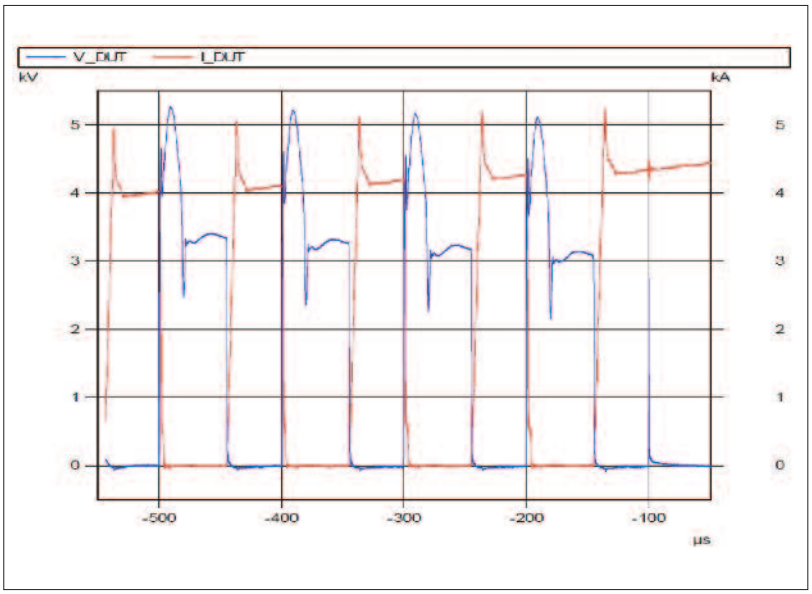

Figure 5: **Waveforms from the 10 kHz burst measurement. This example failed at the fifth pulse, at 4.4 kA**

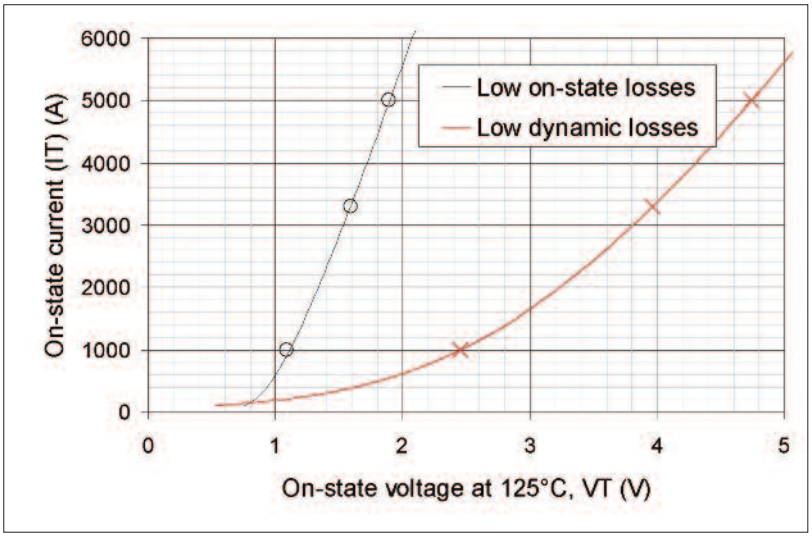

Figure 6: **Flexibility of on-state voltage tailoring in IGCT technology**

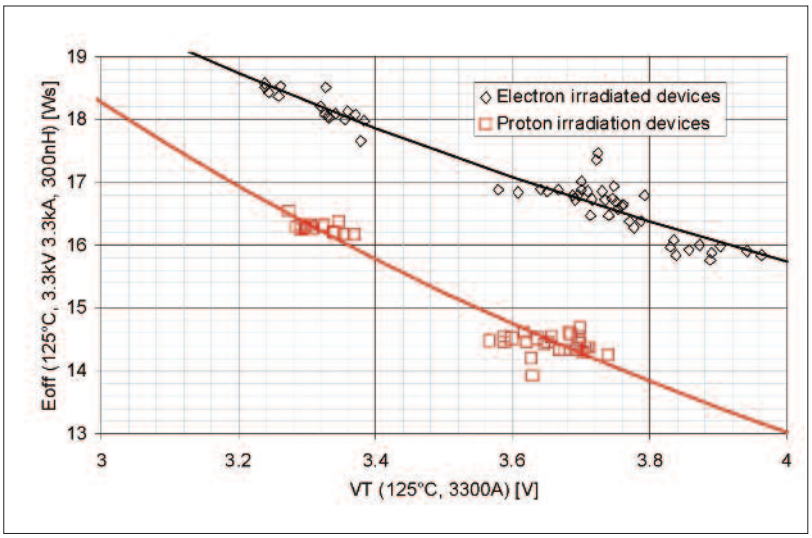

Figure 7: **Loss trade-off for the 5.5 kA IGCT switching 3.3 kA at 3.3 kV with a T_j of 125°C. Additional circuit parameters are listed in the caption of Figure 3**

were evaluated in the dynamic circuit, both at single pulse as well as at burst frequency (10 kHz) for special applications. Samples of waveforms from SOA measurements are presented in Figure 4. Noteworthy is that SOA testing was interrupted when the maximal voltage reached 6 kV during testing. Beyond 6 kV, one would risk a blocking failure in the clamp-circuit discharge following the switching transient, which would not add any information, as this condition would be far beyond specified capabilities.

The burst capability of the device was tested - five pulses at 10 kHz. As the temperature coefficient of the MCC is negative, the failures always occur at the fifth pulse. Due to limitations in the test circuit, it is not possible to test at constant current and voltage. Instead, the current increases and the voltage decreases as the pulse train progresses. In this mode, the IGCT withstands a current of around 4 kA at a voltage between 3 - 3.3 kV. Of course, when switching at this speed, the process is more or less adiabatic which means that the wafer temperature is significantly higher than the allowed 125°C after pulse number 5, if the starting temperature is 112°C. A typical pulse pattern from the burst tests is presented in Figure 5.

To optimize the losses in the 5.5 kV HPT-IGCT, both proton and electron irradiation are used. Figure 6 shows the high flexibility that is possible using different irradiation doses.

Using these lifetime tailoring techniques, a profound influence can be seen on the loss trade-off (Figure 7).

Before a newly developed device is released, it must undergo extended reliability testing. The performance of the device in the presence of cosmic rays is especially of interest with new Silicon specifications and Thyristor designs. Testing was done in a proton beam, for which a sound correlation to actual cosmic rays has been established, with the obvious advantage that the testing is done in a matter of hours instead of years (Figure 8).

In the pipeline - the 150 mm IGCT

The quest for ever higher power ratings makes the option of expanding into larger Silicon diameters viable. Since bipolar devices using 150 mm Silicon since have been in production for some time now, the means are available. In addition, the improved scalability of the HPT technology is an important enabler for taking such a step. The first 150 mm reverse conducting 4.5 kV HPT-IGCT prototypes have recently been

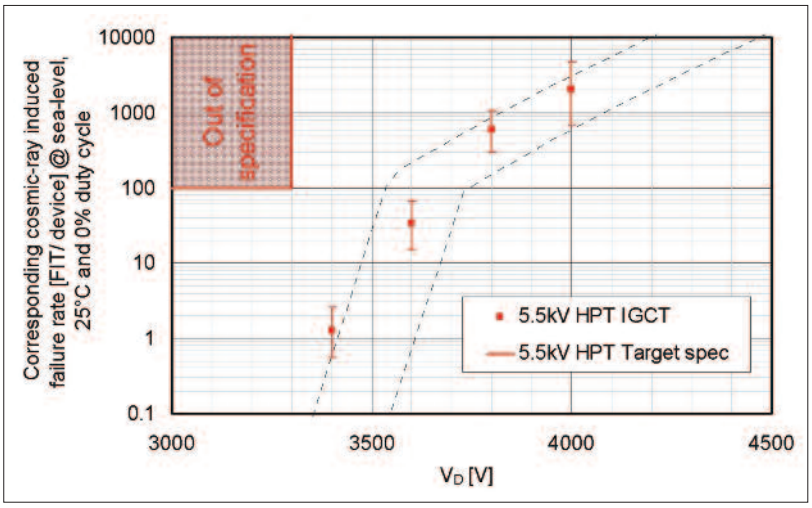

Figure 8: Corresponding failure rates due to cosmic rays measured using biased devices in a high-energy proton beam. The specification can be used arbitrarily; however, the 100 FIT level has become the accepted standard where failures due to cosmic rays will become a significant factor in the field

manufactured and a sample is shown in Figure 9.

This device is expected to have a rated SOA capability in excess of 7 kA against a DC voltage of 2.8 kV at similar conditions as presented in Figure 3. With this device, it will be possible to make 3-level inverters up to about 20 MW without the need for series or parallel connection of power semiconductor devices. With the free-wheeling diode already integrated in the IGCT package, assembly designs can be improved. Critical to the performance is the size and uniformity of the inductance for the segment rings. However, by employing the design elements from the existing HPT-IGCTs, the wafer has the targeted performance in respect to uniformity and absolute inductance.

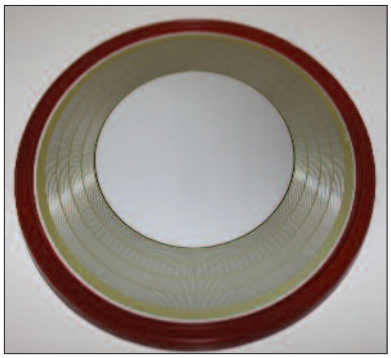

Figure 9: Prototype of 150mm 4.5 kV RC-IGCT

Today, the added challenges lie in the design of the housing package and the gate unit. On the wafer design front, the main challenge is to provide a soft integrated diode performance under different operational conditions including the best IGCT versus diode area ratio selection. Hence, there is still some work to be done before the device is ready, since extensive electrical and environmental qualifications also lie ahead before the first devices can leave the factory.