

Crack-Proofed High-Voltage Ceramic Capacitors

Syfer StackiCap™ surface mount multi-layer capacitors (MLC) are designed to provide high capacitance voltage (CV) in compact packages and offer the greatest volumetric efficiency and CV per unit mass of X7R ceramic capacitors. Syfer have developed a unique process. Combined with FlexiCap stress relieving terminations these parts have the potential to replace film and tantalum capacitors and make many stacked products obsolete. **Chris Noade, Marketing Manager, and Matthew Ellis, Application Engineer, Syfer Technology, Arminghall, UK**

StackiCap are suitable for a plethora of power electronics applications such as switch mode power supplies for filtering, tank and snubber, DC/DC converter, DC block, voltage multipliers etc. So far 1812 and 2220 case sizes have been launched and are commercially available, sizes up to 8060 are under development.

Downsizing potential

Offering significant increases in available capacitance StackiCap can offer significant downsizing over existing technology. Figure 1 shows the initial product range sizes of 1812 and 2220 alongside two development sizes, 2225 and 3640. 5550

and 8060 development sizes are not shown. Figure 2 shows a range of stacked and stacked leaded assemblies of sizes 2225, 3640, 5550 and 8060 up to a maximum of 5 in a stack. Figures 3 and 4 show examples of what can be replaced with a single StackiCap component. In the most extreme cases an 8060 1 kV 470 nF could be replaced with a single 2220 1 kV 470 nF and a 3640 1 kV 180 nF could be replaced with a single 1812 1 kV 180 nF, these are 10:1 and 7:1 footprint reductions respectively.

The first parts to become available in the StackiCap family will be 1812 and 2220 case sizes, with 200 V to 1 kV and

500 to 3 kV operating voltage ranges respectively. Syfer's 2220 500 V device features 1 μF capacitance in a single chip. The 3 kV part also features a 33 nF capacitance previously found only in the much larger 5550 case size. In the 1812 range, the 200 V part also features 1 μF capacitance, while the 1 kV device features 150 nF capacitance, previously only possible in larger size components.

Historical limitations

The limits of design are defined by the failure modes and there are many failure modes which limit the extent to which mid to high voltage MLCC can be developed. There are extrinsic failure modes such as mechanical and thermal cracking but we will look at the intrinsic ones which are in the hands of the manufacturer.

The limiting factor for MLCC has changed over time, early MLCC were limited mainly by the quality and purity of the dielectric materials themselves with point defects and contamination (see Figure 5), limiting the maximum number of layers and the minimum thickness of those layers. As dielectric materials and materials preparation and processing improved the limiting factor became the dielectric strength of the material itself.

Once this point had been reached one could imagine that thicker and larger parts could be manufactured without fear of dielectric breakdown (Figure 6), or point failures, however a new failure mode appeared, electromechanical stress cracking. Commonly referred to as piezo electric it can also follow electrostrictive behavior (see Figure 7). This is the failure mode that has been the limiting factor for MLCC manufacturers for some time now, it affects most class II barium titanate base dielectrics and becomes an issue for larger size, 1210 upwards, and higher voltage,

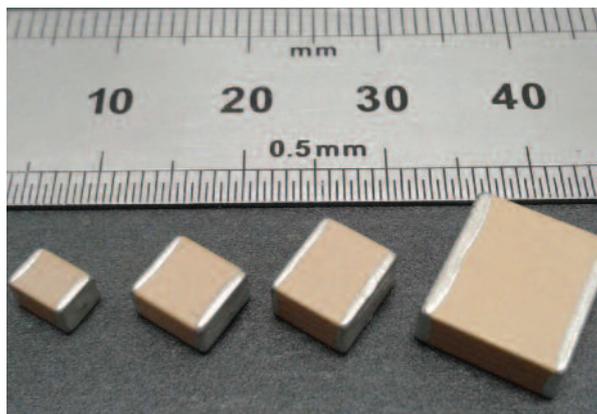


Figure 1: StackiCap sizes 1812 to 3640

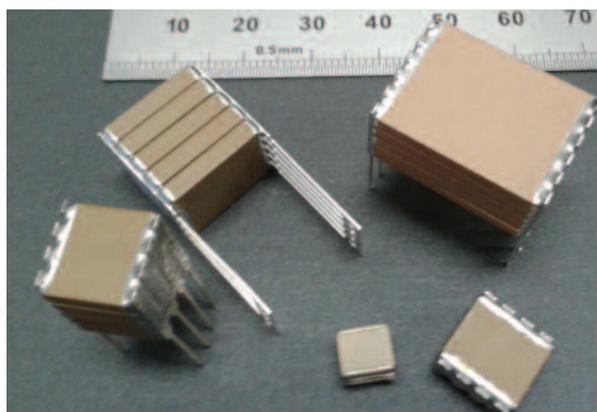


Figure 2: Various stacked assemblies up to 8060 5 stack

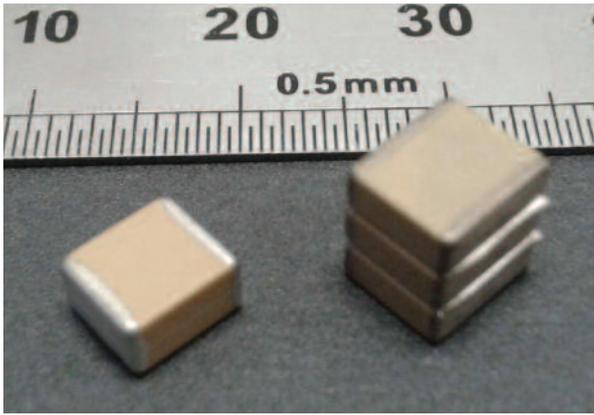


Figure 3: 2220 500 V 1 µF StackiCap™ and 2225 3 Stack 500 V 1 µF

labor intensive, costly and can lead to other reliability issues. Other solutions involve special dielectric formulations but these are usually a trade-off for dielectric constant and therefore the ultimate capacitance value available.

The technology behind StackiCap

After a series of trials and iterations Syfer have developed a single chip solution to this electromechanical failure limitation. The novel and patent pending aspect, GB Pat. App. 1210261.2, is an inbuilt stress relieving layer which allows the capacitor to exhibit the electrical and physical behavior of multiple, thinner, components whilst exploiting the manufacture and process benefits of being a single unit. The stress relieving layer is made up of a combination of already utilised material systems and is formed during the standard manufacturing process (see Figure8). The layer is positioned in the place/s where mechanical stress is the greatest allowing for mechanical decoupling of the multiple component layers with 2, 3 and 4 “stack” versions trialled at this point.

With FlexiCap flexible termination material and no need to attach components together to form a stack there is no need for a lead frame allowing for standard tape and reel packaging with pick and place capability.

Extensive testing

StackiCap technology has been under development for some time, parts and materials have been subjected to Syfer’s standard quality control and reliability regime. In addition to the standard inspection and tests performed during batch manufacture, a sample of batches is also randomly selected for additional routine endurance, humidity and bend tests. Reliability tests are also conducted by external test laboratories as part of maintaining product approvals and are also conducted to assess long-term product performance.

The released StackiCap range has passed all testing and has amassed over 2,000,000 hours of reliability test time. High Reliability testing is also ongoing with a full AEC-Q200 Rev D qualification under way for 1812 and 2220 case sizes, additional rel qualification testing can be considered on request.

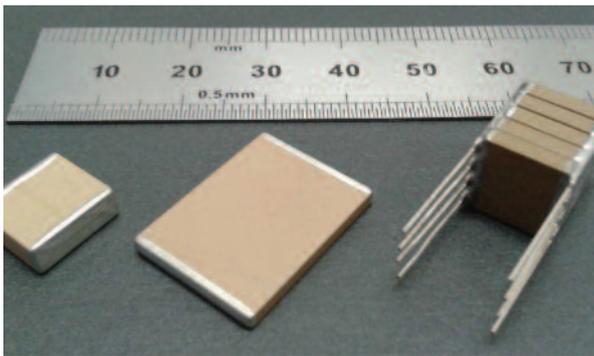


Figure 4: 3640 500 V 3.3 µF StackiCap with 8060 and 3640 5 stack alternatives



Figure 5: Contamination defect

200 V upwards components.

The crack typically runs through the centre of the component along one or two dielectric layers. Most solutions involve



Figure 6: Dielectric breakdown

stacking capacitors together with lead frames in order to increase the available capacitance for a given footprint but this is

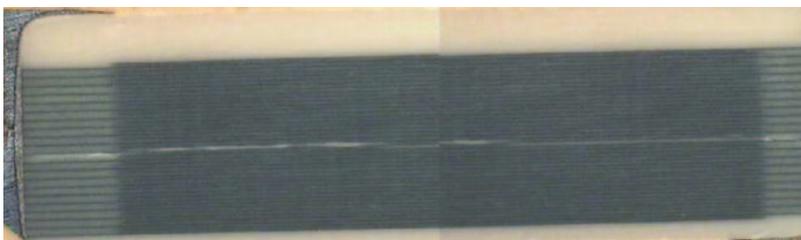


Figure 7: Piezo stress crack failure

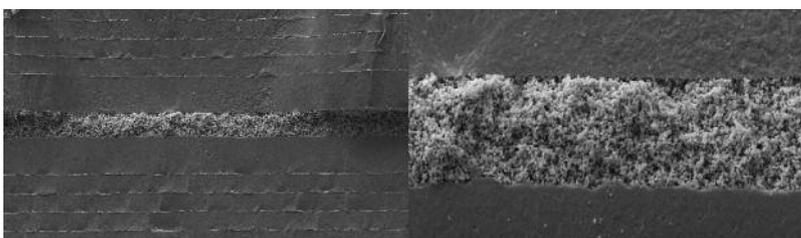


Figure 8: SEM micrograph of fracture sections showing the stress relieving “spongy” layer

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