A New Standard in Dual Power MOSFET Packaging

International Rectifier's patented (US6946740) new dual Power MOSFET in a Power Quad Flat No-lead (PQFN) package leverages the latest advances in packaging technology to increase power density, efficiency, and thermal capability in non-isolated DC/DC converters. **Kevin Ream, Power MOSFET Marketing Manager, International Rectifier, El Segundo, USA**

In today's fast paced digital world, technology is constantly evolving at breakneck speeds. Whether it's pushing more content across the web or handheld devices, information in the forms of data, video, or sound is constantly pushing the extremes of communications, data storage, and server technology. The increased bandwidth, memory size, and switching speeds required to support this comes at the expense of increased power. When you throw in variables such as environmental concerns and limited form factors, power density and efficiency become the driving factors in today's power system designs.

Many of today's high performance, high power systems use a distributed architecture for distributing power within. An intermediate bus converter will take the system input voltage and down convert it to a lower bus voltage, typically 8-14 V. This voltage is locally converted to a lower voltage (5 V, 3.3 V, 1.8 V, 1.2 V, 0.9 V,…) to power the processors, DSPs, FPGAs, and/or memory and is typically handled by a synchronous buck DC/DC converter (see Figure 1). Power designers are tasked with optimizing this circuit by trading off efficiency, size, and cost. One option for reducing the size and cost of the circuit is to use a dual MOSFET as opposed to two singles. Given today's advances in Silicon technology and packaging, this has now become a viable alternative.

Traditional Dual MOSFET

A traditional dual MOSFET in a 5 mm x 6 mm PQFN package targeted at synchronous buck DC/DC converters originated from duals in the standard SOIC-8 package and is supported by many vendors in the industry today. It contains both a Control and Synchronous MOSFET whose cross sectional view is shown embedded into Figure 1's simplified DC/DC converter schematic and footprint. The die from the Control MOSFET's source is connected to the Synchronous MOSFET's drain by a copper clip via a common exposed pad. This exposed pad is connected to the switch node in the DC/DC converter. The Synchronous MOSFET's source is connected to the lead frame via a clip. This in-turn is connected to the GND plane of the DC/DC converter.

There are two key disadvantages to the traditional dual MOSFET approach. The main disadvantage is that the drain of the Synchronous MOSFET is connected to the board. Since the Synchronous MOSFET's clip is a thermal bottleneck, most of the heat is transferred out of the PQFN package via the exposed drain pads at the bottom of the board and this drain pad is localized around the switch node of the DC/DC converter. Another major source of heat is the circuit's output inductor, L1 in Figure 1. This is also localized around the circuits switch node. Both of these contribute to a concentrated thermal hot spot at the switch node which leads to unnecessary levels of heat. Note that, this is also true for approaches which use two single MOSFETs. Recall that a MOSFET has a positive RDS(on) temperature coefficient and this unnecessary increase in temperature leads to an increase in conduction losses (I^2R). It is quite ironic that a power designer will sacrifice cost to design in the lowest $R_{DS(on)}$ Synchronous MOSFET only to experience an unwanted rise in conduction losses due to poor thermal performance.

The second disadvantage of the traditional dual MOSFET in a PQFN power

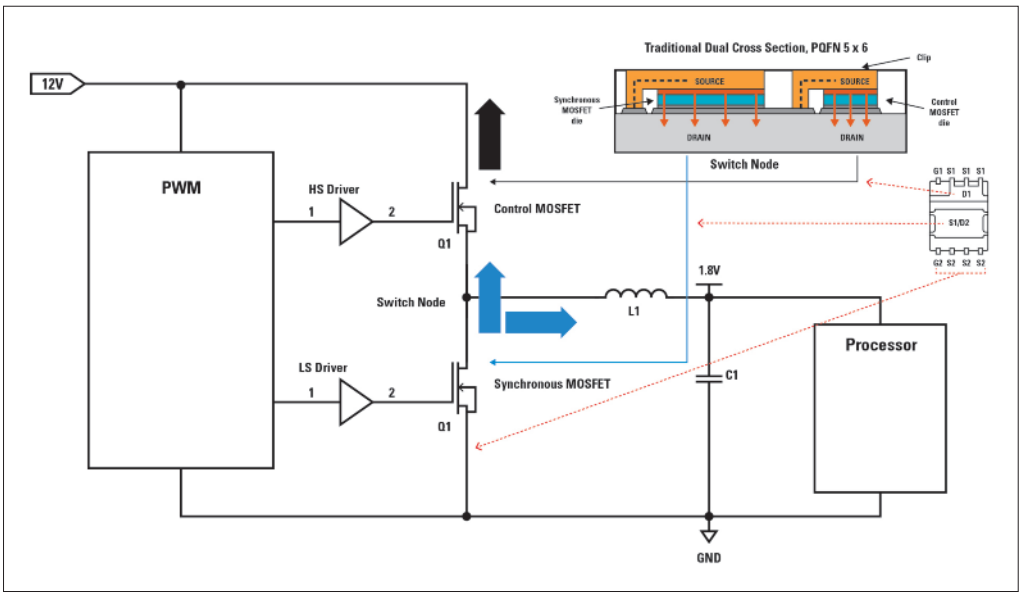

Figure 1: Simplified schematic of Synchronous Buck DC/DC Converter utilizing traditional dual MOSFET

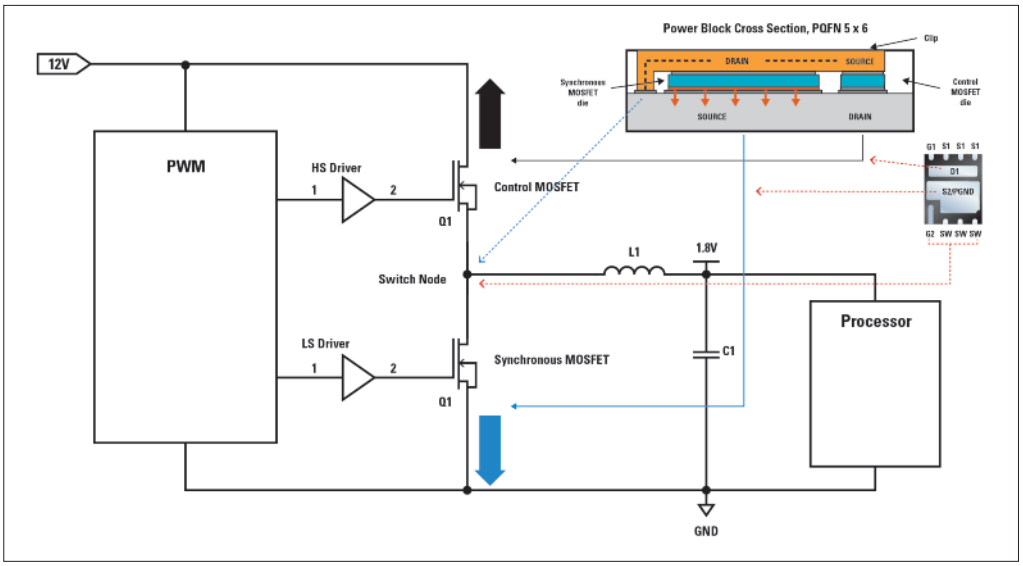

Figure 2: Simplified schematic of Synchronous Buck DC/DC Converter utilizing the power block

package is that it relies on two copper clips for interconnecting the Synchronous and Control MOSFETs. This takes up valuable internal package space which could be used for a larger die, i.e., lower $R_{DS(on)}$ Synchronous MOSFET, leading to a decrease in power density. It also does not allow for optimal placement of the die within the package leading to increased package parasitics and higher peak ringing.

Power Block

Recently, a new package that also contains the Synchronous and Control MOSFET in a single 5 mm x 6 mm PQFN package was introduced. The advantages to this package over a traditional dual include:

- Synchronous MOSFET source (not drain) is facing the PCB
- Single clip to connect the Synchronous and Control MOSFETs
- Multi sourced

Figure 2 shows the cross section of the power block package embedded within the DC/DC converter simplified schematic. Recall that the majority of heat generated in a low-voltage MOSFET is at the junction/source of the device. Notice that the Synchronous MOSFET's source is facing the PCB in the power block package and the single copper clip is the switch node. This source-down configuration allows the majority of the heat within the package to be directed towards the GND plane of the board and away from the switch node and output inductor. This translates into lower PCB and MOSFET temperatures thereby improving the efficiency of the converter.

The power block also employs a MonoFETky synchronous MOSFET which minimizes QRR related switching losses and dead-time diode conduction losses. Combined with an ultra-low package interconnect inductance, this minimizes the reverse recovery current yielding a 0.2-0.4% efficiency improvement over traditional dual MOSFETs. Figure 3 shows the improvements in both efficiency and thermals when comparing the power block to best in-class similarly specified MOSFETs.

Flipping the Synchronous MOSFET also allows for the use of a single copper clip to connect the two MOSFETs within the package whereas the traditional dual uses two clips. This has the following advantages:

- Increased utilization of die area within the package -> higher power density
- Excellent die placement allow optimal input bypassing -> lower peak ringing
- Reduction in package parasitics -> lower peak ringing.

Using a single copper clip also allows for the exposure of the clip on the topside of the package by simple, inexpensive grinding techniques. This could not be reliably achieved with the traditional dual two clip package due to the discrepancies in clip height. Comparing two similarly specified power blocks, both exposed to 200 LFM of air flow, one could realize a 12°C lower PCB temperature (based upon simulation results) leading to a 24% improvement in Total Thermal Resistance (θ_{JMA}).

Given that today's high performance DC/DC converters switch as high as 400-600 kHz, package parasitics become an increasing concern. One of the advantages to connecting the control MOSFET's source to the synchronous MOSFET's drain (switch node) internally via a single copper clip is a significant reduction in package parasitics. If you couple this benefit with the very tight layout of the internal die, designs which

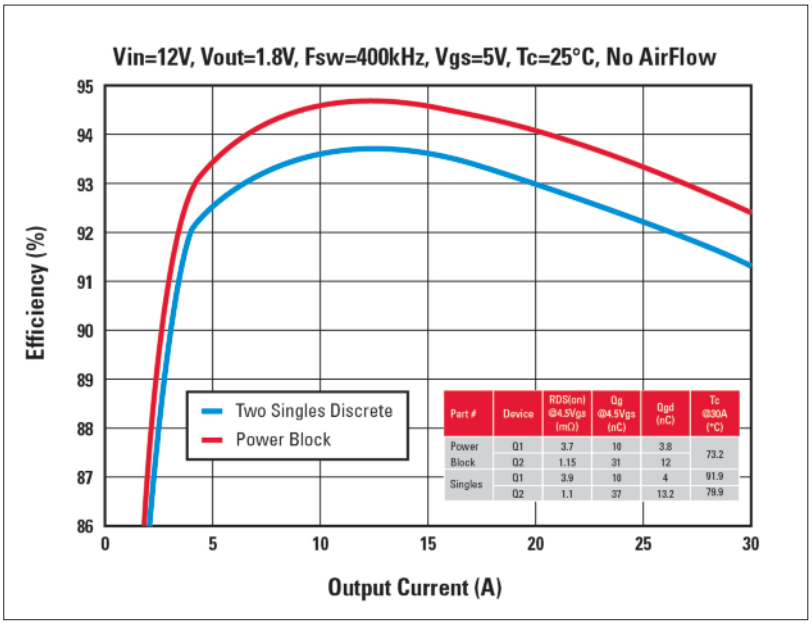

Figure 3: Efficiency and thermal results for power block vs. best in-class singles

had typically used 30 V MOSFETs in the past to accommodate ringing and overshoot can now utilize 25 V Silicon. This translates into a cost savings due to the fact that for the same $R_{DS(on)}$ a 25 V MOSFET's Silicon is smaller than a 30 V device.

Stacked Dual MOSFET

One additional dual used within the industry today stacks the Control MOSFET on top of the Synchronous MOSFET. Similar to the power block, the Synchronous MOSFET's source faces the PCB so efficient heat transfer to the GND plane is realized. One of the main disadvantages to this approach is that by stacking the MOSFETs, the heat from each MOSFET interact causing an unwanted rise in $R_{DS(on)}$, thereby leading to increased power dissipation and lower efficiency when compared to the power block. Additionally, two copper clips are required adding to manufacturing complexity and higher profile of the device. A summary of the pros and cons of each dual package technology is shown in Table 1.

	Traditional Dual MOSFET	Stacked Dual MOSFET	Power Block
Pro	• Smaller than 2 discretes	• Smaller than 2 discretes • Synchronous MOSFETs source is facing the PCB	• Smaller than 2 discretes • Synchronous MOSFETs source is facing the PCB • Using single copper clip
Con	• Synchronous MOSFET drain (not the source) is facing the PCB • Using 2 copper clips	• Proprietary footprint for a long time (due to unique silicon technology) • Stacked MOSFET makes them heat each other more than non-stacked • Using 2 copper clips	
Foot print	• Industry-standard	• Proprietary	• Industry-standard

Table 1: Pros and Cons of Dual MOSFET package technology

Conclusion

In order to meet the power density and efficiency targets of today's high performance systems, the very best MOSFET silicon AND packaging technology is required. By flipping the synchronous MOSFET so the source side is down (facing the PCB), and internally connecting its drain to the source of the control MOSFET via a single copper clip, the power block package is capable of achieving power densities never before realized by traditional duals. Couple this with the latest high performance silicon, excellent die placement and package utilization, the new power block package is poised to become the industry standard dual for high performance, non-isolated DC/DC converters.