A Two-Phase Interleaved One Cycle Control PFC for Charger Applications

The electrification of cars is bringing new challenges to the power electronics designers, AC/DC and DC/DC converters are now also needed in the automotive world and car manufacturers and OEMs are striving to address this need in an economical and efficient way. **Davide Giacomini, Product Management Director, Automotive Division, International Rectifier, Italy**

This article discusses the implementation of a two-phase interleaved OCC PFC, used in an AC/DC charger for automotive applications, delivering up to 3 kW output power. Shown are the several steps of the OCC-PFC implementation, from the current sensing to the synchronization and interleaving of the two or more phases of the converter. Results of the real hardware implementation are presented and discussed using waveforms and performances measured in the demo-board.

Hardware implementation

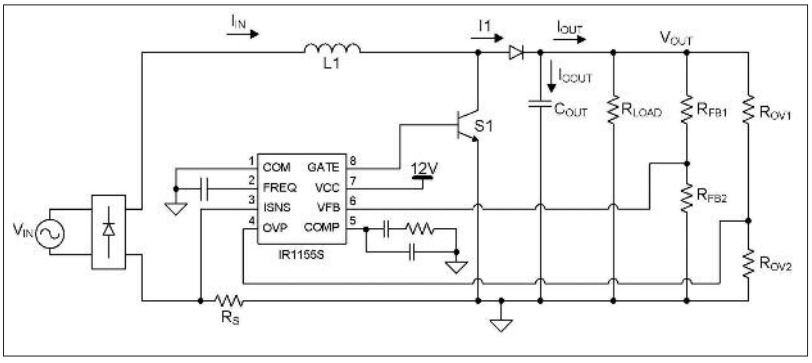
Figure 1 shows the basic application circuit of the IR1155S, the only real OCC IC controller available in the market. In this topology the input voltage sensing is missing and the current sensing is done by reading the negative voltage across the Rs resistor, since the IR1155S ground pin sits on the power ground of the converter for proper IGBT gate driving.

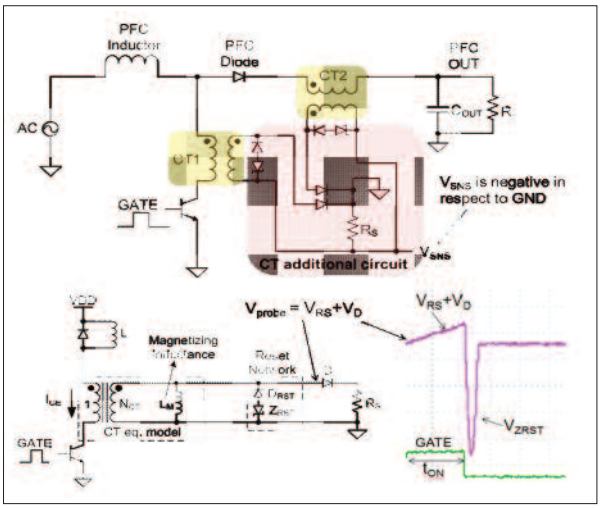
Current sensing stage

For proper operation of the interleaved system each phase current information is needed, as for what it is observed in Figure 1 this is not immediately feasible by duplicating the same schematic since the two channels information will not be independent.

Figure 2 shows the simple circuit used to perform the current measurements, by inserting to small high frequency CT in series to the switch and to the rectifying diode the complete current waveform can be reconstructed and the information correctly fed back into the V_{sns} pin of the IR1155S controller.

The solution, despite apparently complicated, allows an excellent reconstruction of the full current waveform in each phase of the PFC and the correct OCC algorithm implementation on each stage.





ABOVE Figure 1: OCC PFC implementation using IR1155S control IC

LEFT Figure 2: OCC-PFC current sensing using current transformers and current transformer reset network

Clock synchronization and interleaving

The IR1155S uses an internal oscillator that is also internally mirrored to obtain the information for the integration slope of the OCC controller. For this reason we cannot simply use an external clock signal but we need to synchronize each controller clock to an external signal and let it generate its internal ramp.

By observing the oscillator block schematic of the controller, we noticed that the oscillator does not accept a simple external turn-off signal to earlier terminate it, instead we need to tweak it to do it by itself and to maintain a minimum dead time as well. Figure 3 shows the hardware solution used and the related waveforms. The comparators are open-collector output type pulled-up to a voltage higher than 4 V, so to force the internal set of the IR1155S; after the input clock rising the dead time period also starts and will end when the comparator input has gone below the 2.5 V reference. The dead time is now defined by the external RC derivative network.

Current sharing between phases

The current sharing has been implemented in a novel and simple

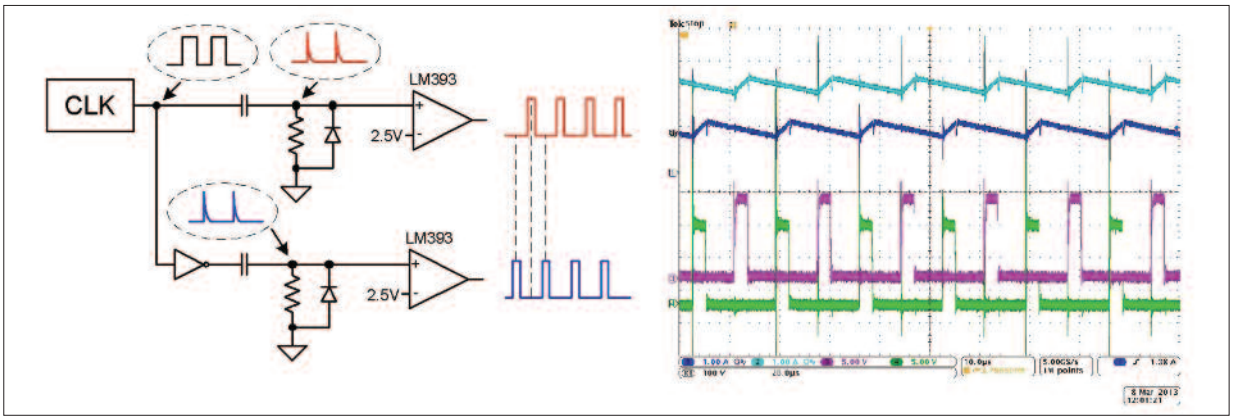


Figure 3: **Synchronisation and interleaving circuit and waveforms (CH1: L1 current, CH2: L2 current, CH3: gate 1, CH4: gate 2)**

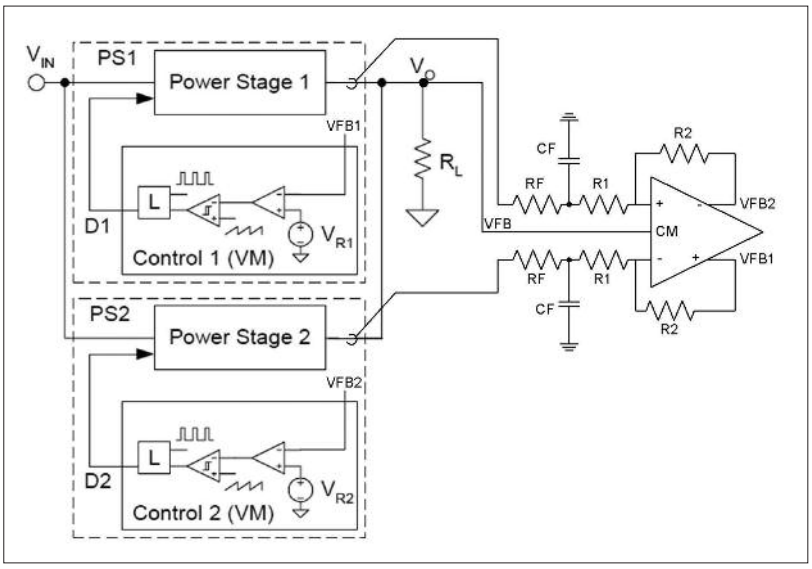


Figure 4: **Novel current sharing technique**

solution, here called *Current Dependent Voltage Feedback*, which allows using any pair of single phase PFC controllers though these have not been designed for current sharing. The idea is based on integrating the current feedback information on top of the voltage feedback on each controller loop, Figure 4 shows the implemented solution block schematic.

The same current sense information used for the OCC algorithm implementation is here used for the current sharing: each current feedback is filtered to recover the average value information and then amplified by a pure differential amplifier whose common mode output is set by the resistor divider connected to the PFC output voltage and it will be equal to the reference voltage of the controller in static conditions.

To be noted is that the amplifier output relative to the input section 1 actually sets the voltage feedback of the controller of section 2, by doing this an increase in the current of section 1 results in a lower Vfb2 signal to the controller of section 1 that then increases its duty cycle and current to compensate the difference.

Figure 5 shows the circuit implementation and the resulting waveforms in steady state at 1.5 kW output of this novel current sharing technique.

Experimental results

A two-phase interleaved OCC PFC for automotive charger application has been

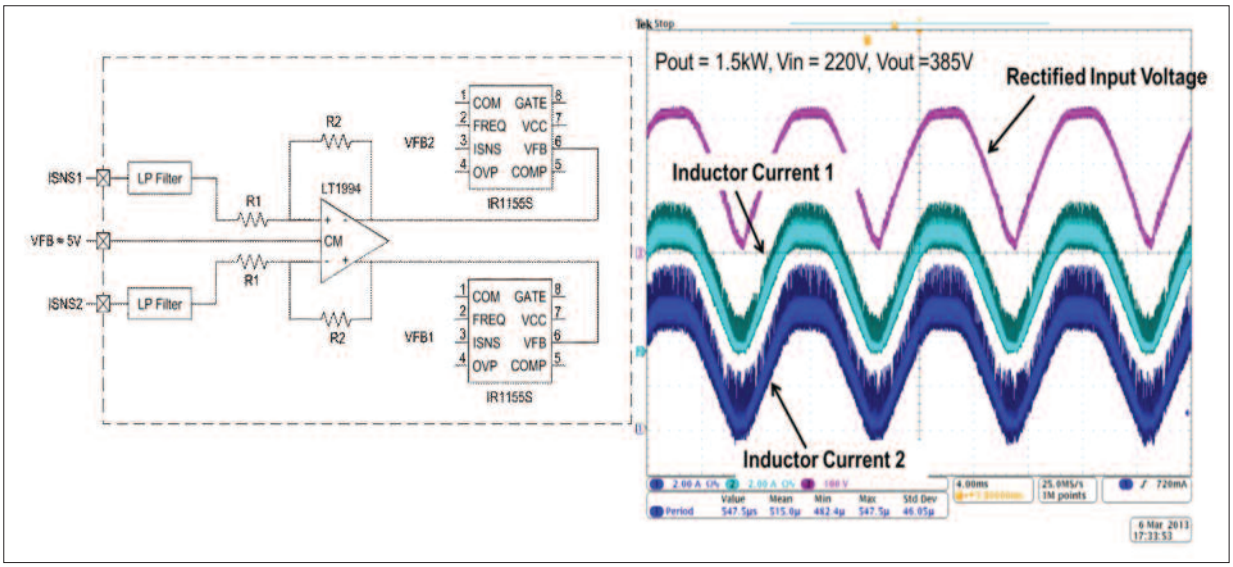
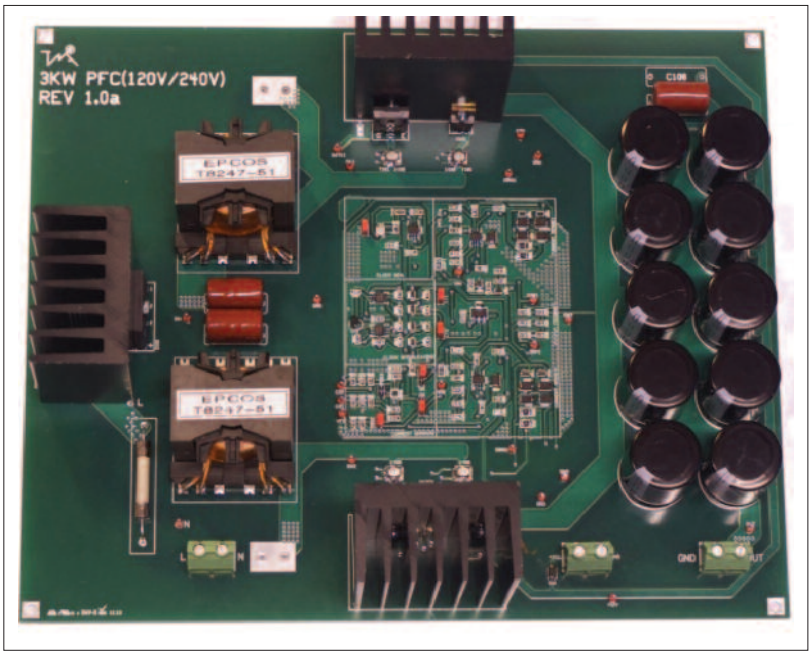


Figure 5: **Current Dependent Voltage Feedback implementation (CH1: L2 current, CH2: L1 current, CH3: rectified input voltage)**



RIGHT Figure 6: Two phase interleaved OCC-PFC demo-board

implemented with the following targets:

- V_{IN}: 100 V AC/240 V AC
- Max I_{IN}: 16 A
- V_{OUT}: 385 V
- L: 250 µH
- C_{OUT}: 3 mF
- Freq: 50 kHz – 100 kHz
- P_{OUT} : 3 kW

Since the high power output the switches of choice have been the IGBTs, considered more reliable and rugged than SuperJunction MOSFETs in this application, the rectifying diodes selected are of Ultrafast family, though also SiC diodes have been successfully tested in the same board.

Main power devices used in the solution are the following: AUIRGP65G40N (IGBTs, 2x), ETX1506 (diodes, 2x) and IR1155S (OCC controllers, 2x). The board has been tested at different input voltages and switching frequencies to verify the performances and efficiency of the solution.

Figure 6 shows the demo-board, the large area in the center of the PCB is the control area with all external electronics needed to interleave the two IR1155S sections. Most of those components can be integrated in a single chip solution for future optimization of the circuit.

The board has been tested at different switching frequencies; Figure 7 shows the final PFC factor vs. output power and switching frequency (50 kHz) and the total power dissipation and efficiency vs. power output, of the two phases OCC-PFC converter. Maximum PFC factor is achieved at higher frequency, however a good balance between PFC and efficiency is reached at this power level for 50 kHz switching frequency. A maximum efficiency of 98 % is achieved at 230 V AC input.

Conclusion

A novel two-phases interleaved One Cycle Control PFC for Automotive Applications has been proposed and verified both in simulation and hardware, each phase uses a IR1155S OCC-PFC controller and some external electronics has been added to synchronize the two stages and equally share the current. The advantages of the chosen topology and control strategy are evident; no high voltage sense input, simple implementation with easy compensation, rugged IGBT switches and robust control system compared to standard CCM PFCs. Performances of the demo-board are confirming the expected results with an efficiency in excess of 98 % and a power factor coefficient above 99 % for > 700 W output. The proposed solution presents a viable alternative for a reliable realization of the PFC stage for level 1 and 2 Automotive AC/DC chargers and verifies the applicability of the dual phase OCC-PFC concept.

BELOW Figure 7: PFC performances vs. output power, total power dissipation and efficiency