New 3-Level Topology for Efficient Solar Applications

Three-level topologies' most persuasive selling points are high efficiency and reduced filtering effort. Several three-level topologies feature prominently single-phase solar applications. This article presents a new alternative that also meets the requirements for reactive power and the need to drive down costs. Pro and cons are benchmarked against two established three-level solutions and the discussion concludes with a first look at power modules designed to support this new approach. **Michael Frisch and Temesi Ernö, Vincotech Germany and Hungary**

Solar inverters must generate sinusoidal output current to be fed into the public power grid. The simplest way of producing sinusoidal current is to use an H-bridge inverter with pulse width modulation (PWM) of DC voltage and an output filter. The three-level topology serves to reduce switching losses and the output filter's effort. With two-level modulation, the power semiconductor has to switch at higher voltages, e.g. 400 V. In a singlephase, three-level system the filter's primary output is shorted during freewheeling, this will reduce the switched

voltage. This reduces switching losses and the size of the output filter by half, albeit while still using the same PWM frequency. Excitation is the same as in the standard two-level H-bridge with bipolar switching, but the output of the H-bridge is shorted during freewheeling. In a single phase 3 level system is the output primary of the filter shorted (Figure 1 right), this will reduce the switched voltage.

Advantages of 3-level operation

In 2-level operation energy will be regenerated during freewheeling back to the DC-ling capacitor according to equation 1

 $\mathsf{E}_{\mathsf{regeneration}} = \mathsf{U}_{\mathsf{DC}} * \mathsf{I}_{\mathsf{Output}} * \mathsf{t}_{(\mathsf{off})}$

(1)

 $The energy injected into the grid results to: \\ E_{Out} = E_{Exication} - E_{regeneration} = U_{DC} * I_{Output} * t_{ON} - \\ U_{DC} * I_{Output} * t_{Off} (2) \\ E_{Out} = U_{DC} * I_{Output} * (t_{on} - t_{off}) (3)$

The regenerated energy has to pass the inverter twice without value (excitation and regeneration) and it will each time cause additional power dissipation.

With 3-level operation the voltage at a symmetrical output filter is changing between VDC (e.g. +400 V) and half of the actual output voltage (e.g. 0..160 V at 230 V AC grid). The switching losses and the size of the output filter may be minimized using still the same PWM frequency. The excitation works like in standard 2-level H-bridge with bipolar switching, but during freewheeling the H-bridge is turned off and the output shorted.

HERIC-and H5-topology

The HERIC-based inverter circuit (Figure 1) implements a dynamic short connection at the output using two sets of IGBTs and diodes in serial array. The sets are connected in an anti-parallel circuit at the H-bridge's output. For every half-wave, two different IGBTs of the H-bridge are switched with PWM during real power (where the current and voltage have the same polarity). The IGBTs at the output are turned on and off during the corresponding half-wave.

Pros - low static losses in third-level mode:

- Voltage drop at real power during ON 2 IGBTs
- Voltage drop at real power during OFF and freewheeling - 2 IGBTs + 2 diodes
- Voltage drop at reactive power during OFF and freewheeling - 2 diodes

Cons - complex structure:

Requires 6 IGBTs (four of the ultrafast switching variety) and 6 fast diodes

The H5-topology (Figure 2) offers a different solution for the same approach. The additional IGBT is switched via PWM together with the low-side IGBTs, while the high-side IGBTs are turned on and off during the corresponding half-wave at real power.

Pros - fewer components:

- Requires 5 IGBTs and 5 fast diodes
- Just three of the five IGBTs have to be of the ultrafast switching variety (if the focus is on real power efficiency)

Cons - high static losses:

 Voltage drop at real power during ON - 3 IGBTs

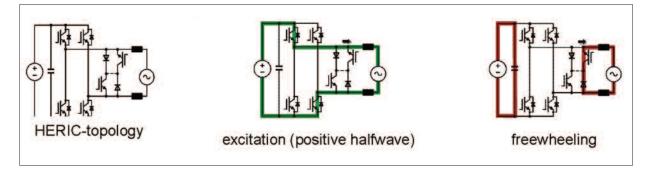


Figure 1: HERIC-topology in excitation and freewheeling mode

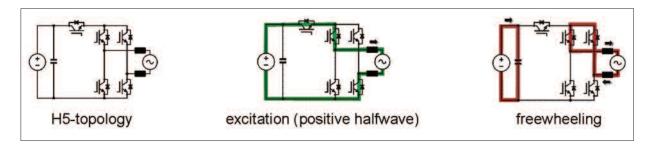


Figure 2: H5-topology in excitation and freewheeling mode

- Voltage drop at real power during OFF and freewheeling - 1 IGBT + 1 diode
- Voltage drop at reactive power during OFF and freewheeling - 3 diodes
- 5th switch requires an extra power supply for its gate drive

New H6.5-topology

The new topology also uses six IGBTs like

Real power - On

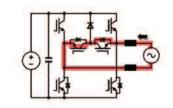
negative half-wave

Real power - On

the HERIC topology, but it requires just five diodes (Figure 3).

The new topology achieves the same real power performance as the HERIC topology. There is a price to pay for reducing the number of diodes from six to five, namely one additional junction at freewheeling during reactive power. However, this is of negligible importance in solar applications.

Real power - Off-Freewheeling / On-Reactive Power



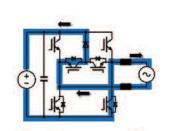
Real power - Off-Freewheeling / On-Reactive Power

Pros - low static losses at real power operation:

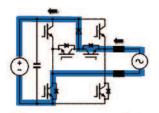
- Voltage drop at real power during ON 2 IGBTs
- Voltage drop at real power during OFF and freewheeling - 2 IGBTs + 2 diodes

Cons - complex structure:

 Requires 6 IGBTs (four of the ultrafast switching variety) and 5 fast diodes



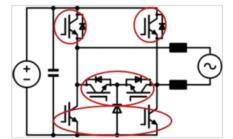
Reactive power - Off-Freewheeling



Reactive power - Off-Freewheeling

Figure 3: H6.5-topology working in different modes

H6.5 topology featuring a common collector in the freewheeling path with three



H6.5 topology featuring a common emitter in the freewheeling path with four voltage potentials for the gate drive circuit

Figure 4: H6.5-topology with common collector (left) and common emitter

voltage potentials for the gate drive circuit

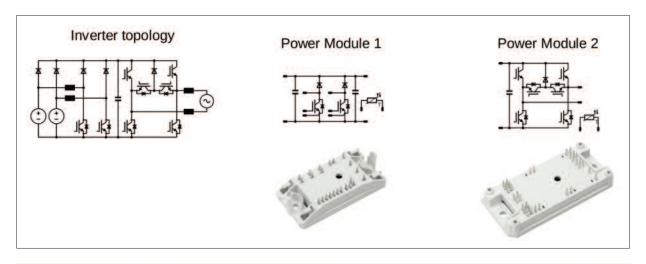


Figure 5: 2x Boost + H6.5 Inverter

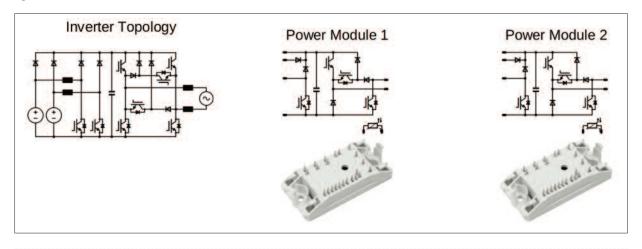


Figure 6: 2x Boost + Halfwave Inverter

 Voltage drop at reactive power during OFF and freewheeling - 3 diodes

Power modules designed to support the new topology

To integrate the semiconductors, the power module will have to

- provide two independent boost stages for MPP (maximum power point) tracking
- incorporate the new H6.5 topology
- handle a high switching frequency, e.g. 40 kHz
- enable low-inductance integration of DC capacitors
- integrate all components in the commutation circuit, even at reactive power
- feature a temperature sensor
- furnish a good thermal interface.

The new topology may be implemented with a common collector or common emitter (see Figure 4) for the freewheeling path. The advantage of using a common collector for the IGBTs in the freewheeling path is that no additional power supply will be required because the emitter is shared with the high-side IGBTs of the H-bridge. This input provides the underpinning for two new modules.

The 2x Boost + H6.5 Inverter (Figure 5) uses a standard 2x booster module and implements the new topology in a second module based on the flow 1 housing. This structure also supports designs where the MPP tracker and inverter are sited at different locations on the PCB.

The 2x Boost + Halfwave Inverter (Figure 6) combines one boost stage and the inverter components for one half-wave in a single module. The advantage is that the two modules' power dissipation is identical, regardless of the input voltage. Two identical modules can make up the inverter's power electronics core. The corresponding IGBT of the switching device is located in the other module, which makes this solution extremely resilient to Xconduction at fast turn-on.

Both options incorporate all components of the commutation circuit inside one module. If they are distributed between two modules, the inductance of both modules' electrical interfaces causes over-voltage at turn-off, which limits options for using fast components.

Conclusion

An unprecedented three-level topology for single-phase solar inverters provides a new alternative to legacy solutions such as HERIC and H5 topologies. This new topology may be used in real power and reactive power modes. Two different power module designs are available with this new topology.

