Zero Voltage Switching Revolutionizes Buck Regulator Performance

Typical point-of-load (POL) applications step down from an intermediate bus voltage, 12 V or lower, to a regulated voltage of a few volts, or increasingly less than a volt. System architects would like to derive stable, regulated power rails for high-current consuming devices (processors and FPGAs) directly from distribution voltages, typically 48 V. Conventional converter limitations preclude doing so because the higher step-down ratio sharply increases power losses; a 2-stage (or more) voltage conversion chain has been the default solution. A significant improvement in efficiency can be delivered by power components that are based upon the ZVS topology. **Robert Gendron, Vice President, Semiconductor Power Solutions, Vicor, Andover, USA**

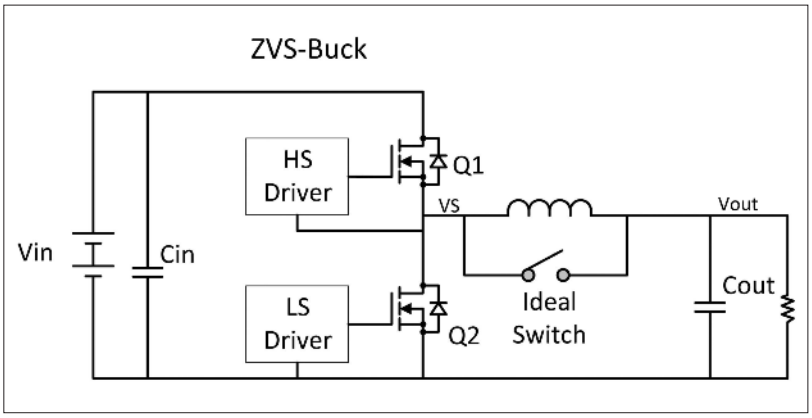
Increased losses with high step-down ratios are largely a consequence of the utilization of "hard" switching, under which MOSFETs turn on or off at high currents and voltages. A new buck topology utilizing Zero Voltage Switching (ZVS) cuts power losses arising from several causes – it reduces switching losses and also cuts gate driving losses, as well as eliminating FET body diode conduction.

The niPOL (non-isolated POL regulator) has benefited from improvements in device packaging, Silicon integration and MOSFET technology. While existing solutions work well over a narrow voltage range, efficiency and throughput power tend to drop somewhat at modest step-down ratios of 10:1 or 12:1. They fall off drastically for a wide input range with a step-ratio approaching 36:1, due to the hard-switched buck regulator's inherent losses.

Losses in conventional buck topologies can be traced to a number of specific sources; predominantly from hard switching, body diode conduction and gate drive loss, which are described below.

Conduction of high currents while voltage is imposed on a switch – a situation that arises while the device transitions from off to on – causes switching losses proportional to frequency and operating voltage. Improved MOSFET technology and switching speed can reduce the time when current and voltage are simultaneously applied. But this brings its own problems; hard switching usually results in spiking, ringing, and increased EMI. The approach becomes less attractive over a wider operational range requiring higher voltage or frequency.

Losses in the synchronous switch body-diode occur because there usually is some conduction time when the synchronous MOSFET turns off before the high-side switch turns on. Body diode conduction requires stored charge accumulated while conducting to be swept away (reverse



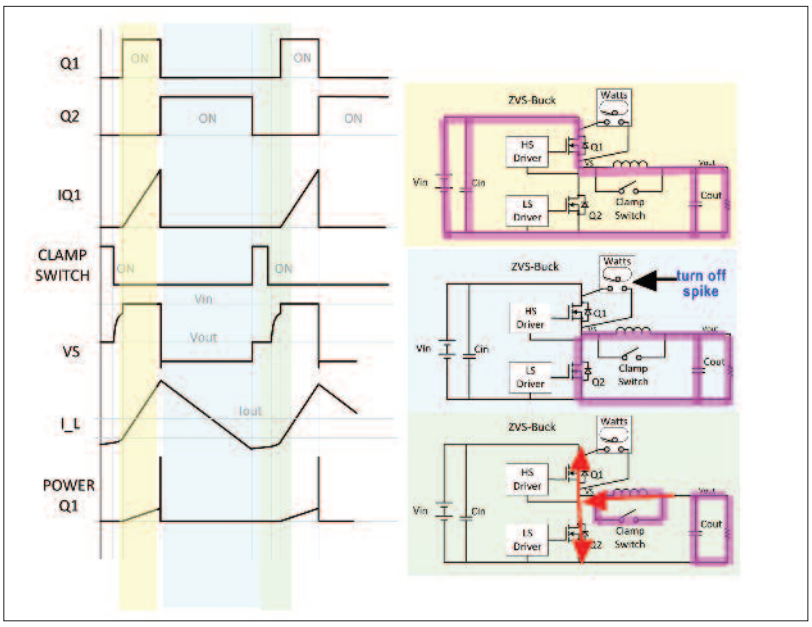


Figure 1: **ZVS Buck topology and switching cycle timing diagram**

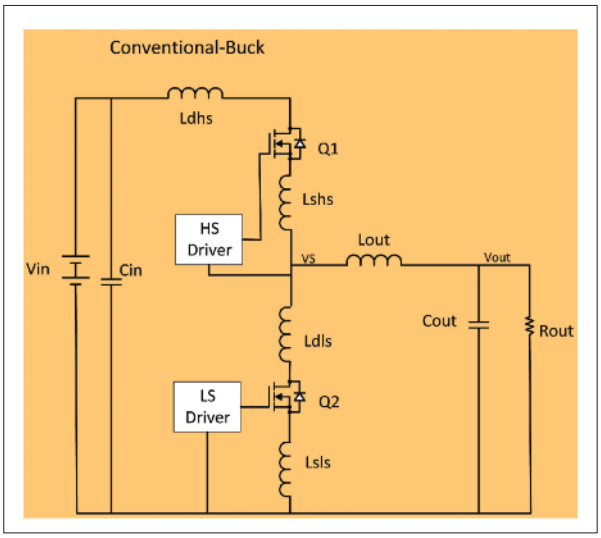


Figure 2: **Conventional Buck topology**

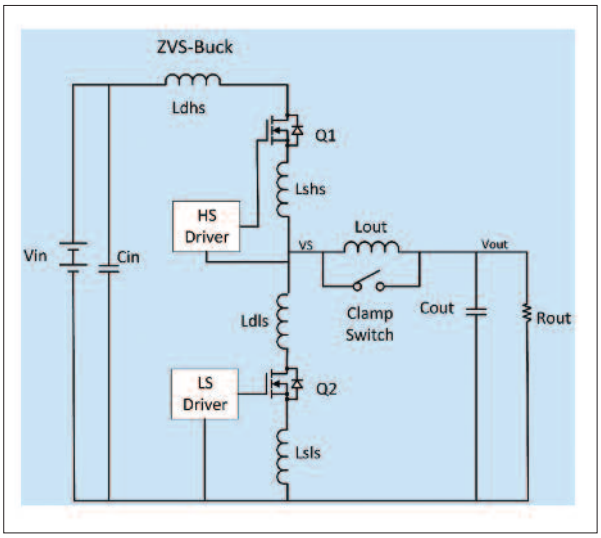


Figure 3: **ZVS Buck**

recovery) before the diode can support any reverse blocking voltage. This causes power losses which are also proportional to the switching frequency.

Each transition of the MOSFET state also takes power from the gate driving stage. The power is the same for each transition, so losses are also proportional to switching frequency.

ZVS topology

ZVS Buck Topology (Figure 1) is identical to a conventional buck regulator, except for an added clamp switch across the output inductor: energy stored in the output inductor is directed to ensure that switching takes place under zero-voltage conditions.

The ZVS switching cycle comprises three main states; Q1 on-phase, Q2 on-phase, and clamp phase. After Q1 turns on, current through the output inductor builds from zero to a peak set by Q1's on-time, the voltage across the inductor ($V_{in} - V_{out}$) and the inductor value; energy is stored in the output inductor and charge is supplied to the output capacitor. During the Q1 on-phase, the majority of the power dissipated is in the MOSFET's on-resistance.

Next, Q1 turns off rapidly and Q2 turns on to free-wheel the energy stored in the output inductor

to the load and output capacitor. As there is a series L-C circuit involved, this current will decline as part of the initial stage of its oscillatory behavior and in due course will reverse. As Q1 turns off, there are losses proportional to the peak inductor current.

The ZVS Buck topology fundamentally operates in 'discontinuous mode'. However, a key aspect of its operation is that the synchronous MOSFET Q2 is held on for longer than might otherwise be expected, beyond the point at which the inductor current passes through zero and reverses. In this short interval of reverse current, (some) energy is again stored in the inductor. The converter's controller sets the level of this accumulated energy at the value needed for the following phase, based on several parameters including input voltage and output load.

When the synchronous MOSFET Q2 finally turns off, the clamp switch turns on to circulate the inductor current and conserve the energy stored in the previous phase, before the next switching cycle takes place. Note that, in this clamp phase, Q2 stays off; there is no body diode conduction and no associated reverse recovery losses.

The clamp switch is opened at the end of the clamp phase, before Q1 is turned on. Now, a different resonance comes into play; the energy stored in the inductor resonates in the tank circuit formed by the output inductor and the paralleled drain-source capacitances of Q1 and Q2, so the VS node sees the first part of a sinusoidal waveform, taking it towards V_{in}. With suitable timing (calculated by the controller) Q1 is turned on when the VS node is nearly equal to V_{in}, minimizing switching losses and the Miller effect, due to the small drain-source voltage difference.

The Miller effect is eliminated from the high-side MOSFET at turn-on: the high-side gate driver can be smaller and consume less power. The high-side MOSFET does not have to turn on particularly fast, resulting in smooth waveforms and less noise.

Conventional vs ZVS Buck operation

Figures 2 and 3 depict basic conventional and ZVS buck topologies. Figures 4 and 5 show waveforms from steady-state simulations of those circuits with realistic values – for today's packaging and construction – applied in respect of MOSFET package parasitic inductances, and lumped parasitic inductance of the PCB traces. In both cases, the step-down is from 36 V to 12 V at 8 A; the conventional converter has an output inductor of 2 µH for a switching frequency of 650 kHz. For

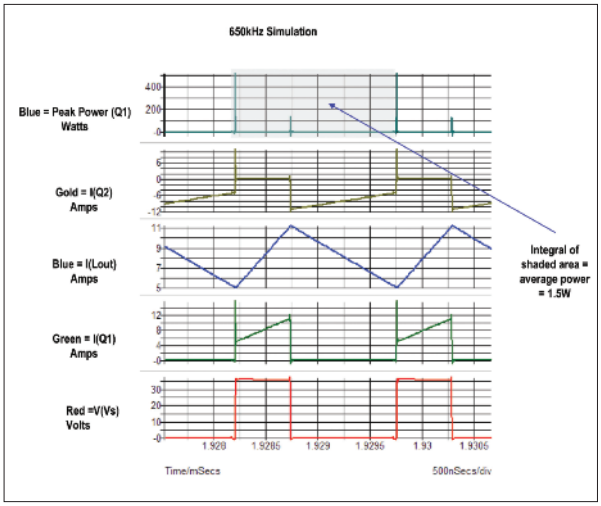


Figure 4: **Conventional Buck waveforms**

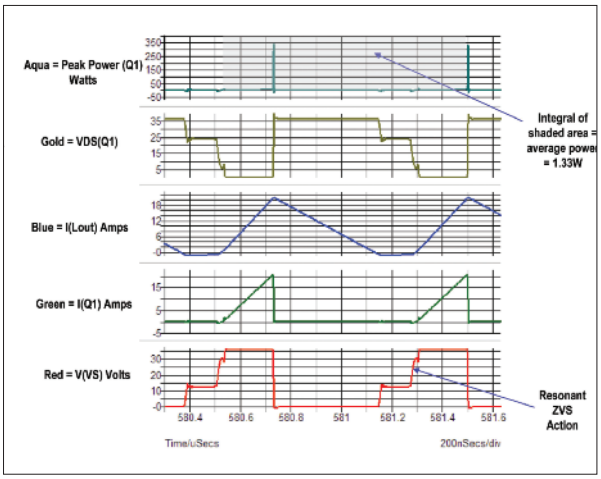


Figure 5: **ZVS Buck waveforms**

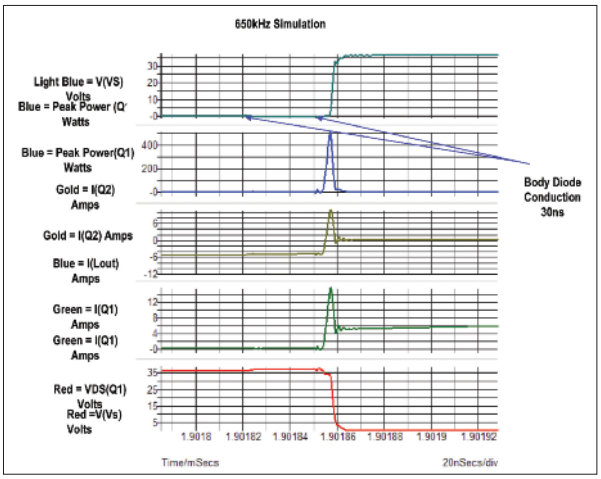


Figure 6: **Detailed waveforms for Q1 turn-on**

the ZVS Buck the inductor is 230 nH for operation at 1.3 MHz.

Note that in Figure 4 (conventional buck) inductor current is continuous, ranging between 5 A and 11 A: for the ZVS buck, operations is discontinuous, and the reversal of inductor current in the clamping phase is apparent. Figure 4 reveals high losses at turn-on and somewhat lower losses at turn-off, whereas the conduction losses in the MOSFET's on-resistance are quite low. Average power dissipation in the high-side MOSFET is 1.5 W: 0.24 W in conduction, 0.213 W through turn-off and 1.047 W over the turn-on. The turn-on element dominates: Figure 6 expands (time axis) this phase.

To avoid cross conduction, there is a 30 ns dead time between Q2 turning off and Q1 turning on; during this time, the body diode of Q2 is forward biased and it carries the current freewheeling through the output inductor. When Q1 turns on, that body diode must go through reverse recovery, before it can block the reverse voltage. This accounts for the current spike in Q1, which simultaneously sees a large V_{DS}, almost equal to V_{in}: hence the large power loss. Further effects, due to parasitic inductances, also contribute.

ZVS Buck

The simulation shows that at 1.3 MHz the average power dissipation in the high-side MOSFET Q1, including switching losses and conduction losses, is 1.33 W. This is lower than the conventional regulator despite operation at twice the switching frequency and a much smaller inductor. Figure 5 also confirms that as the voltage across Q1 has been contrived to be nearly zero as it is turned on, the associated losses are virtually zero: also, there is no body diode conduction prior to the turn-on of Q1 and no reverse recovery effects, including reverse recovery loss in the body diode of Q2.

The PI33XX family (Figure 7) of wide input range DC/DC regulators is configured using ZVS topology and Picor's high performance Silicon controller architecture. The 10 mm x 14 mm SiP package requires only the output inductor and a few ceramic capacitors to form a complete buck converter. The family supports wide input range of 8 V – 36 V, to outputs from 1 V to 15 V, at high power and efficiency. As noted above, the inductor can be small and the switching frequency high, typically allowing 120 W to be output from 25 mm x 21.5 mm PCB area with 98 % peak efficiency.

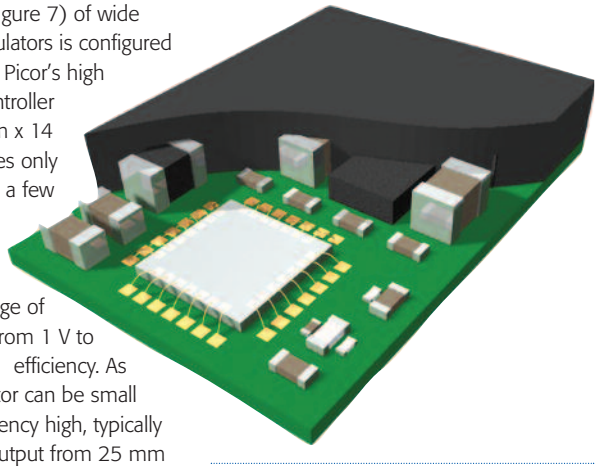


Figure 7: **Construction of the PI33XX family of DC/DC converters**

The converter's discontinuous operation allows efficient operation with 20 ns minimum on-time, overcoming limitations on step-down ratios. This addresses the requirement to reduce the number of conversion stages in power distribution. A buck converter capable of supplying point-of-load directly from a 48V rail, going up to 60 V, is now a practical proposition. Figure 8 shows an efficiency curve for a 48 V to 2.5 V ZVS buck, at 10 A output. Even at the maximum input voltage of 60 V, the efficiency curve stays above 92 % and peaks up to 94 % above 50 % load.

These performance figures represent a significant improvement over conventional buck converter, demonstrating the significant improvement in efficiency delivered by power components that are based upon the ZVS topology.

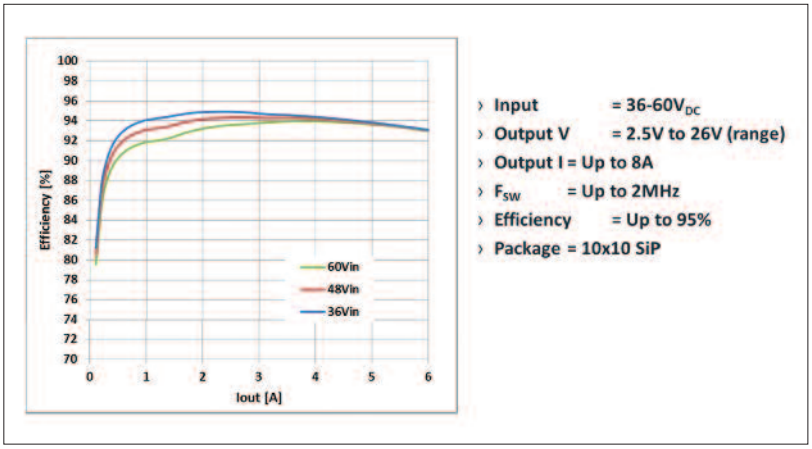


Figure 8: **PI3501 efficiency curves (provisional results)**