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# A New Approach to Circuit Breaker Design Using Silicon Carbide Switches

Mechanical circuit breakers can be low cost with minimal losses, but they operate slowly and wear out. Solid state versions overcome the problems and are becoming increasing viable as replacements at ever-high currents. This article discusses the issues and introduces a new Silicon Carbide semiconductor, the DG-FET as an enabler for better performance.

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**Mechanical circuit breakers have been** around for a long time and do the basic job very well – they are low loss when on and provide excellent isolation when off. They do have their downsides though, with slow make/break times and arcing across the contacts, degrading their operating lifetime, particularly with DC power lines. Complex arrangements have been devised to disconnect quickly but it might still take around 10 milliseconds, allowing significant and possibly damaging energy to pass after a short circuit is detected, for example. Similarly, DC arcs can be suppressed to an extent with labyrinth clearances, a magnetic bias field or even blasts of compressed air. However, there are new applications for high current DC circuit breakers where this complexity cannot be afforded such as in EVs, where cost, size and weight are major issues.

## Solid-state breakers have been a partial solution

Solid-state circuit breakers (SSCBs), typically using IGBTs, can break power lines perhaps a thousand times faster than mechanical types with no arcing or aging problems, but they are imperfect switches, dropping around 1.5 V, producing tens or hundreds of watts of dissipation at the current levels seen in EV traction drives, for example. The unit and heatsinking costs are substantial and the power loss effectively reduces battery energy available for driving range, so in EVs, IGBT-based SSCBs are not seen as viable.

Silicon MOSFET-based SSCBs have been an alternative, with their on-resistance potentially dissipating less power than IGBTs which have a fixed saturation voltage. However, at high current levels with high voltage devices, sufficiently low on-resistances are not yet available. For example, at 500 A, an IGBT could drop

| Feature | Solid state (Si, SJ, SiC, IGBT, IGCT) | Electromechanical |
|---|---|---|
| Full controllability | ★★★★★ | ★★★ |
| High speed | ★★★★★ | ★★ |
| Conduction loss | ★★ | ★★★★★ |
| No arcing | ★★★★★ | ★★ |
| Use cycles: no maintenance | ★★★★★ | ★★ |
| Cost per amp | ★★ | ★★★★★ |
| Voltage rating vs. on Rds(on) | ★★★ | ★★★★★ |

Table 1: **Mechanical and solid-state circuit breakers compared**

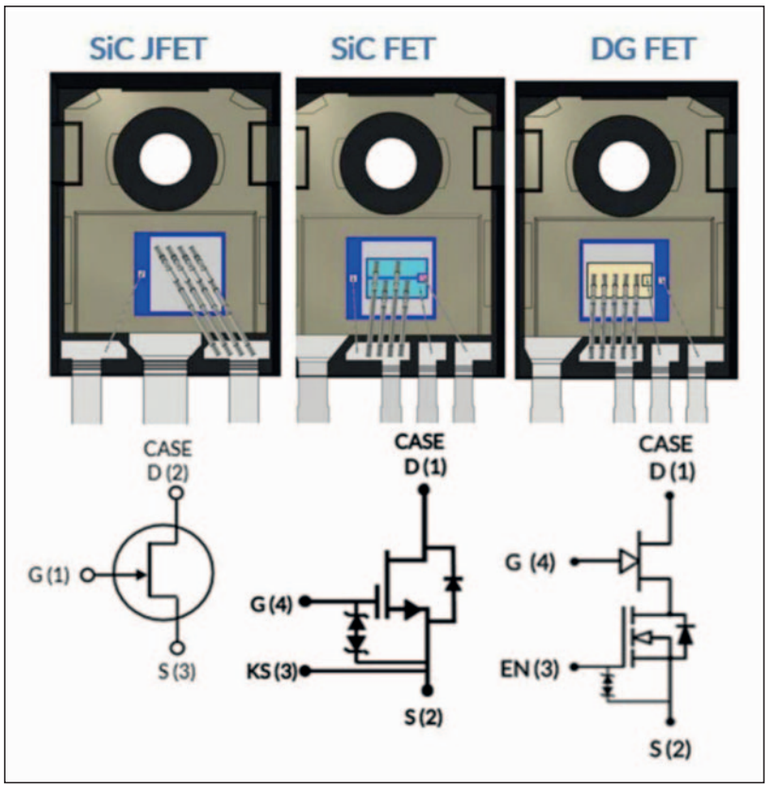


Figure 1: **A SiC JFET (left), SiC FET (middle) and a DG-FET (right)**

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around 1.7 V with 850 W dissipation, equivalent to a MOSFET with 3.4 mΩ on-resistance, which is not available from single devices rated at 400 V and higher. Paralleled MOSFETs reduce dissipation, but ten plus would be needed to match an IGBT in this scenario and if bi-directional conduction is required, as would be typical in an EV application, the number doubles anyway and costs spiral. Table 1 summarizes the relative performance attributes of mechanical and solid-state circuit breakers.

## A new technology for SSCBs

Wide band-gap semiconductors such as Silicon Carbide types (SiC) usually hit the headlines for their fast switching speed, but they also have inherently around 10x better on-resistance for a given die area and voltage rating than Silicon. This makes them potential candidates for small, efficient SSCB switches, and the high material operating temperature and better thermal conductivity are additional benefits for peak power dissipation considerations.

Although SiC MOSFETs are most common, the simpler JFET construction (Figure 1, left) can be preferred in the SSCB application with its better on-resistance, $R_{DS(ON)}$. The device is normally-on with no gate drive but this is often a better characteristic for SSCBs, defaulting to the conducting state with no bias voltages present. Another arrangement is the SiC FET (Figure 1, middle). This device is a 'cascode' combination of a SiC JFET and a Silicon MOSFET which is normally-off, with a simple 0-12 V gate drive. On-resistance is 5-15 % higher than the SiC JFET on its own though, for the same voltage and current class of device.

A new device has now appeared, the 'Dual Gate FET' or DG-FET (Figure 1, right) which is the SiC FET cascode with its two gates uncommitted and brought out to separate pins. The advantage is that the gate drive voltages can now be 'fine-tuned' for the absolute minimum on-resistance, typically by driving the JFET gate a little positive in voltage. The Silicon MOSFET gate then acts just as an 'enable' signal. The two die are 'stacked' for minimum connection distance and losses.

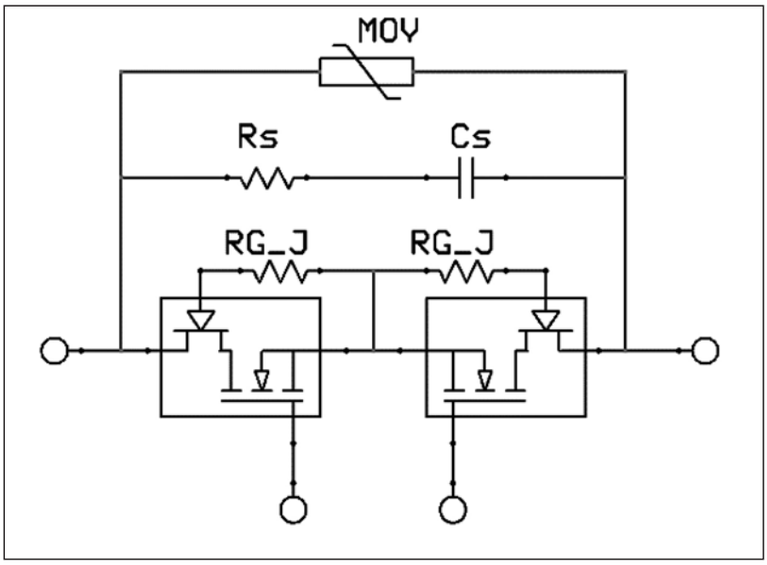


Figure 3: **DG-FETs as a bi-directional solid-state circuit breaker**

## Temperature sensing with a DG-FET

When the gate of the JFET In a SiC DG-FET is taken positive, at around 2 V, a diode action appears and current flows. If the current is accurately limited to say 1 mA, the voltage at the gate has a direct relationship to the die temperature, so can be used as a sense for over-temperature protection or even long-term state-of-health monitoring. This is a valuable feature in SSCB applications to detect any long-term degradation of cooling efficiency, for example, as the DG-FET may have continuous high current passing and significant dissipation. The effectiveness of current sharing in parallel device can also be monitored by evaluating differences in die temperature. Figure 2 shows the typical relationship between die temperature and SiC JFET gate-source voltage.

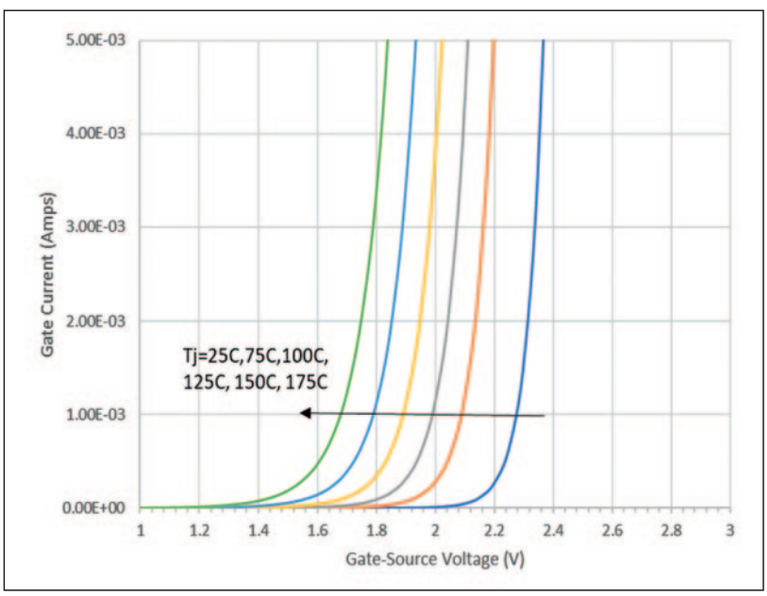


Figure 2: **SiC JFET gate-source voltage scales with die temperature at fixed current**

## SSCBs with SiC DG-FETs

Figure 3 shows a practical circuit using SiC DG-FETs for a bi-directional SSCB. Gate resistors slow switching to avoid EMI and instability, and the snubber network helps prevent damaging voltage overshoot on switch-off. The MOV also clamps voltage transients induced by line inductance between the DC source and load during switching. Although the DG-FETs do have a robust avalanche rating, it can be beneficial to employ an MOV to absorb the energy stored in the line inductance between source and load, since this can become quite large. A large energy MOV is going to cost a lot less than a SiC FET with the same energy rating in avalanche. With this technique, the cost of the SiC used can be reduced. In fact, using a MOV that better limits peak voltage, lower voltage rating SiC devices can be used, which in turn reduces on-state resistance and cost.

To take our example of requiring 3 mΩ devices to be equivalent to a current IGBT, for a uni-directional SSCB, one 1200V dual-gate device from UnitedSiC could be used, which contains six paralleled 9 mΩ FETs, achieving 2.2 mΩ

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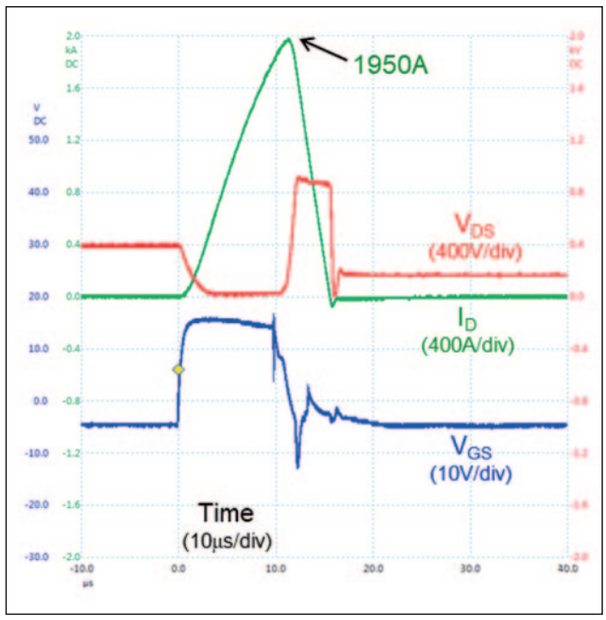
with 1200 V withstand and 300 A rating. These can be packaged in a SOT-227 module, comparable with an IGBT solution with similar performance.

UnitedSiC have trialed this arrangement and demonstrated the device interrupting a peak fault current of 1950 A safely (Figure 4). SiC JFETs have an inherent current limiting characteristic from an internal channel 'pinch-off' effect and the positive temperature coefficient of their on-resistance helps with current sharing between the paralleled devices, in contrast to IGBTs which do not naturally share current when paralleled.




**LEFT Figure 4: A SiC FET SSCB interrupts nearly 2000 A safely**

### Future SSCBs

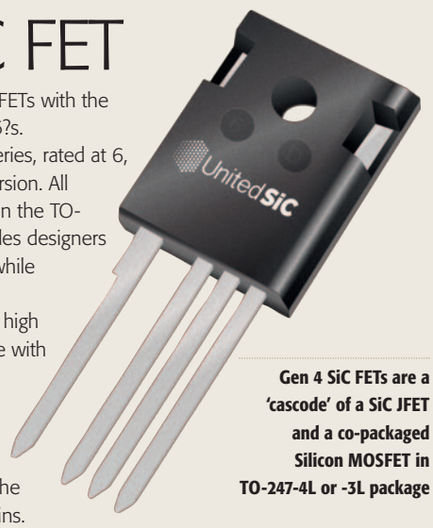
Mechanical circuit breakers, with their speed, arcing and lifetime problems will surely give way to solid state versions at higher and higher power levels as semiconductor performance advances. Even today, an automotive-grade breaker is expensive and as the market expands, particularly in EVs, the solid-state version costs will drop quickly, making it a compelling alternative given the added benefits in speed and reliability. SiC devices are still in their relative infancy and it can be expected that prices will anyway fall over the coming years, with wafer costs predicted to halve. On-resistance performance will also improve, as the technology is some way from its theoretical best, so for a given voltage rating and die size, SiC RDS(ON) should drop to less than a third of its current value, with overall resistance approaching that of a mechanical solution, with all associated connector and cable resistances included. When the lifetime costs of mechanical breaker maintenance and regular replacement are factored in, the SiC version looks more attractive still.

# UnitedSiC Announces 6 mΩ SiC FET

The company has responded to the power designer's requests for higher-performance, higher-efficient SiC FETs with the announcement of the 750 V 7 6 mΩ device which provides a robust short-circuit withstand time rating of 5?s.

The announcement of September 14 includes nine new device/package options in the 750 V SiC FET series, rated at 6, 9, 11, 23, 33, and 44 mΩ. The contribution of wiring in TO-247 package amounts to 1mΩ in the 6 mΩ version. All devices are available in the TO-247-4L package while the 18, 23, 33, 44, and 60 mΩ 7devices also come in the TO-247-3L. Complemented by the already available 18 and 60 mΩ devices, this 750 V expanded series provides designers with more device options, enabling more design flexibility to achieve an optimum cost/efficiency trade-off while maintaining generous design margins and circuit robustness.

Gen 4 SiC FETs are a 'cascode' of a SiC JFET and a co-packaged Silicon MOSFET. These together provide high speed and low losses with high temperature operation, while retaining an easy, stable, and robust gate drive with integral ESD protection. The advantages are quantified by Figures of Merit (FoM) such as RDS(on) x A, a measure of conduction losses per unit die area. Gen 4 SiC FETs achieve the lowest values in the market at both high and low die temperatures. FoM RDS(on) x EOSS/QOSS is important in hard-switching applications. FoM RDS(on) x COSS(tr) is critical in soft-switching applications. "With SiC FETs the switching losses are controlled by the SiC JFET and not directly the the gate charge of the low voltage MOSFET, thus the typical FoM = Ron x Qg is not useful with SiC FETs," Anup Bhalla explains.




**Gen 4 SiC FETs are a 'cascode' of a SiC JFET and a co-packaged Silicon MOSFET in TO-247-4L or -3L package**

**LEFT: "Sintering is the mechanism by which the SiC JFET chip is attached to the Cu leadframe of the package, thus reducing thermal resistance and avoiding solder cracking," Anup Bhalla explains**

For hard switching applications, the integral body diode of SiC FETs is superior in recovery speed and forward voltage drop to competing Si MOSFET or SiC MOSFET technologies. Other advantages incorporated into the Gen 4 technology are reduced thermal resistance from die to case by advanced wafer thinning techniques and silver-sinter die-attach. "Sintering is the mechanism by which the SiC JFET chip is attached to the Cu leadframe of the package, and by which the low voltage MOSFET is attached to the top of the Sic JFET", Bhalla underlines.

With their latest improvements in switching efficiency and on-resistance, the new UnitedSiC SiC FETs are ideal for challenging, emerging applications. These include traction drives and on- and off-board chargers in electric vehicles and all stages of uni- and bi-directional power conversion in renewable energy inverters, power factor correction, telecoms converters and AC/DC or DC/DC power conversion generally. Established applications also benefit from use of the devices for an easy boost in efficiency with their backwards compatibility with Si MOSFET and IGBT gate drives and established TO-247 packaging. Pricing (1000-up, FOB USA) for the new 750 V Gen 4 SiC FETs range from $4.15 for the UJ4C075044K3S, to $23.46 for the UJ4SC075006K4S. All devices are available from authorized distributors.