NewSpace demands low voltage, high current power for performance and longevity

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Satellite operators are offering increasingly sophisticated on-board processing capabilities necessitating the use of the latest ultradeepsubmicron FPGAs and ASICs. These have demanding, low-voltage, high-current, power requirements and OEMs are being challenged to offer more functionality from smaller payloads and platforms. Cost and time-to-market are also key drivers!

Relatively, smaller satellites harvest less energy and with operators increasingly using faster and more on-board processing, there is a requirement that as much of the possible power budget is available for the payload. Traditional power-distribution architectures comprising an isolated DC-DC to step-down the external bus input, followed by localized POLs to produce the required load voltages, are becoming too inefficient because of large I2R drops. To deliver the next generation of New Space missions, improvements are needed in conversion loss, power density, physical size and a transient response compatible with the switching speeds of the latest ultradeepsubmicron devices.

Instead of the conventional, intermediate power-distribution comprising an isolated DCDC followed by buck bricks, Vicor Corporation's patented Factorized Power Architecture (FPA™) uses a modular approach to minimize I^2R distribution losses, maximize efficiency and improve transient response.

The FPA comprises two stages: voltage regulation followed by transformation. First, a buck-boost topology is used to generate a 48V intermediate rail from an external source, which is significantly higher than the lower legacy buses typically input to POLs. For example, a 48V output bus requires four times less current than a 12V intermediate bus for the same power ($P = VI$) and PDN losses are the square of the current ($P = I^2R$), which reduces by sixteen. Placing a regulator first to produce 48V achieves the highest efficiency, allowing smaller satellites to avail of more of the harvested energy.

The second stage of the FPA uses a transformer to convert the 48V intermediate rail to the desired load voltage, e.g. 1V. The output is a fixed fraction of the input (K-factor) defined by the turns ratio. Stepping down the voltage increases the current by the same amount, e.g. a 1A input current would be multiplied to an output of 48A:

A Pre-Regulation Module (PRM™) and a Voltage-Transformation Module (VTM™) current multiplier combine to realize the FPA, with each device fulfilling its specialized role to enable complete DC-DC conversion. The PRM generates a regulated 'factorized bus' from an unregulated input followed by the VTM, which transforms (steps down) the 48V to the desired load voltage.

The VTM's high bandwidth avoids the need for large point-of-load capacitance. Even without any external output capacitors, the output of a VTM exhibits a limited voltage perturbation in response to a sudden power surge. A minimal amount of external bypass capacitance (in the form of low ESR/ESL ceramic capacitors) is sufficient to eliminate any transient voltage overshoot. Without imposing the bandwidth limitations of an internal control loop struggling to maintain regulation, the VTM offers a unique capacitance-multiplication feature. For example, the effective, shunt output capacitance is 2304 times the input capacitance when a K factor of 1/48 is used, i.e. $C_{SEC} = C_{PRI} * K^2$. This means that significantly less decoupling is needed downstream of the VTM and only a small amount of capacitance at its input offers the same energy storage as the bulky tantalums typically added to the 1V output of a traditional buck brick as illustrated in Figure 1.

Low impedance is a key requirement for powering low-voltage, high current loads efficiently and the use of a VTM also reduces the effective resistance seen from the secondary side by K^2. This allows the VTM to be placed at the load, either laterally or vertically, resulting in a lower-loss PDN. The FPA's lower-current, higher-voltage intermediate bus means that the PRM can be located physically away from the VTM without impacting efficiency. This

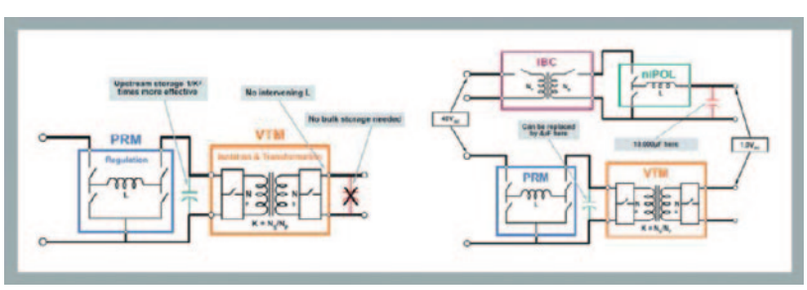

Figure 1: **These diagrams show how the FPA compares to a traditional, intermediate architecture.**

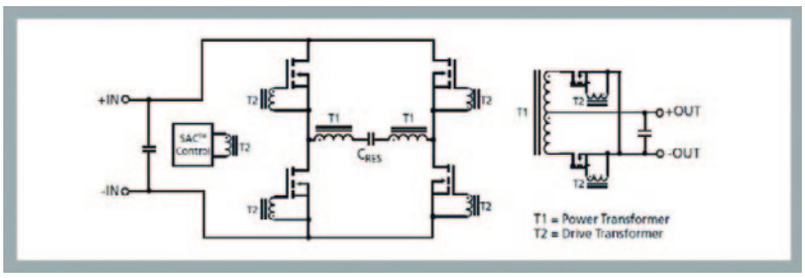

Figure 2: The full-bridge, SAC series-resonant topology offers advantages over existing space-grade DC-DCs.

gives you more flexibility when deciding where to place the PRM, less worries about area congestion at the load and more freedom to size power planes for maximum current density. This floor-planning is very different to the traditional brick approach, which requires the isolated DC-DC and POLs to be close together to minimize I^2R distribution losses.

Present space-grade, isolated DC-DCs and buck POLs are PWM-based devices with the output power proportional to the duty cycle of the switching frequency. These hardswitched converters use a square wave to drive an inductor or transformer with the MOSFET dissipating energy as it is turned on and off. A square wave contains lots of harmonics that must be filtered or they will conduct or radiate throughout the system. The VTM's topology uses a sinusoidal current in the primary winding, producing a cleaner output noise spectrum requiring less filtering. Existing space-qualified buck regulators and forward/flyback DC-DCs specify efficiencies in the range of 67 – 95% and 47 – 87% respectively.

Today, there are 12 suppliers of space-grade switching POLs offering almost 30 nonisolated convertors. Input voltages range from 3 to 16V, load voltages and currents from 0.785 to 9.6V and 4 to 18A respectively, with switching frequencies from 100kHz to 1MHz. Previously, I described the theory of conversion for the buck topology, what criteria to consider when selecting space-qualified parts, and how to choose values for the inductor, input, and output capacitance.

There are seven vendors of space-qualified isolating DC-DCs offering over 30 families of parts generating single, double, or triple standard voltages, or in some cases, adjustable, regulated, stepped-down intermediate outputs. Power ratings range from 2.5 to 500W. Previously, I described the theory of conversion for the forward and flyback topologies.

To meet the power-distribution and low-voltage, high-current needs of future NewSpace constellations, Vicor is qualifying its novel, Sine Amplitude Converter (SAC™) topology for space applications. This patented, ZCS/ZVS technology offers higher efficiencies, larger power densities, and lower EMI emissions than existing space-grade DC-DCs. SAC is a transformer-based, series-resonant, forward architecture that operates at a fixed frequency equal to the resonance of a primary tank circuit as shown in Figure 2.

The FETs in the primary side are locked to the natural resonant frequency of the series tank circuit and switch at zero-voltage crossing points, eliminating power dissipation and increasing efficiency. At resonance, the inductive and capacitive reactances cancel minimizing the output impedance, which becomes purely resistive reducing droop. The resulting very-low output impedance allows the VTM to respond almost instantaneously ($< 1\mu s$) to step changes in the load. The current flowing through the tank is a sinusoid that contributes less harmonic content, resulting in a cleaner output noise spectrum, requiring less filtering of the load voltage.

The SAC has a forward topology with the input energy passing to the output. The leakage inductance of the primary is minimized since it is not a critical storage element. The unique operation of the SAC forward topology enables a higher switching frequency and the use of smaller magnetics with lower intrinsic losses. The resulting increase in efficiency means less power is wasted during conversion, easing thermal management and allowing for more output current and a larger power density from a smaller package. Faster operation transfers energy to the output more often, improving the transient response to dynamic load changes to a few cycles.

Vicor is planning to bring to orbit a range of DC-DCs. Parts have already been de-risked and designed-in by **Boeing for an O3b satellite** offering space-based internet. Initially four rad-tolerant DC-DCs will be offered:

- A 300W, 9A, 849W/in³, isolating, ZVS/ZCS, SAC bus converter module (BCM3423PA0A35C0S), which accepts a DC source from 94 to 105V and outputs a fixed load voltage 1/3 of the input, ranging from 31 to 35V. Its maximum ambient efficiency is specified at 94% in a package size of 33.5×23.1×7.4mm weighing 25.9g.
- A 200W, 7.7A, 797W/in³, non-isolating ZVS buck-boost regulator, (PRM2919P36B35B0S), which accepts an input from 30 to 36V and outputs an adjustable load voltage from 13.4 to 35V. Its maximum ambient efficiency is specified at 96% in a package size of 29.2×19.0×7.4mm weighing 18.2g.
- A 200W, 50A, 1204W/in³, isolating, ZVS/ZCS, SAC DC-DC (VTM2919P32G0450S), which accepts a line voltage from 16 to 32V and outputs a fixed load voltage of 1/8 of the input, ranging from 2 to 4V. Its maximum ambient efficiency is specified at 93% in a package size of 29.2×19.0×4.9mm weighing 11g.
- A 150W, 150A, 903W/in³, isolating,

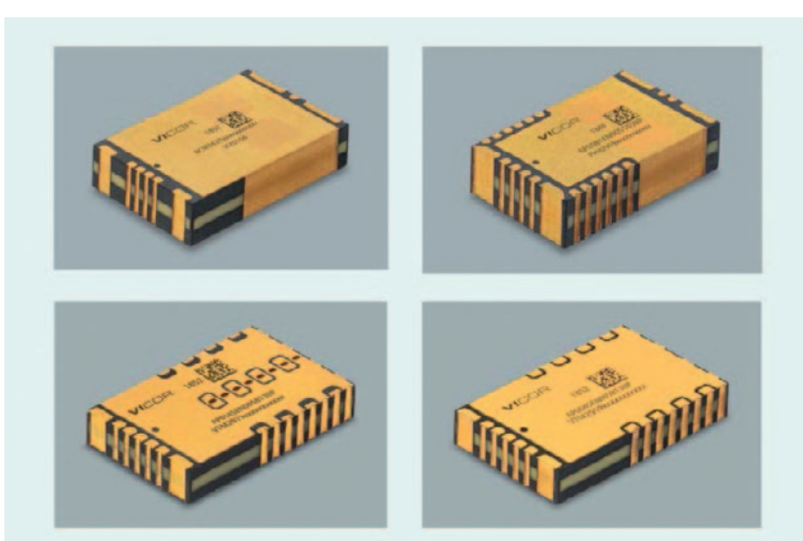

Figure 3: Vicor will offer these new BCM, PRM, and VTM rad-tolerant DC-DCs.

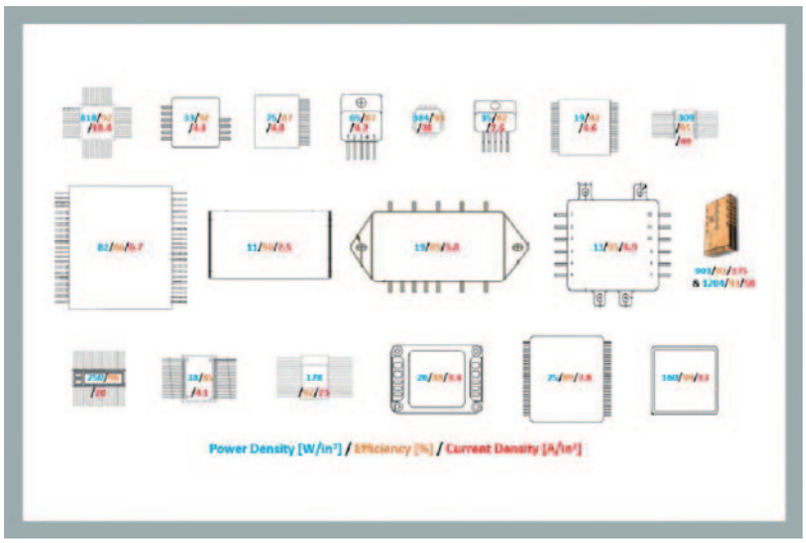

Figure 4: **This diagram compares space-qualified switching POLs with the VTM2919 DC-DCs.**

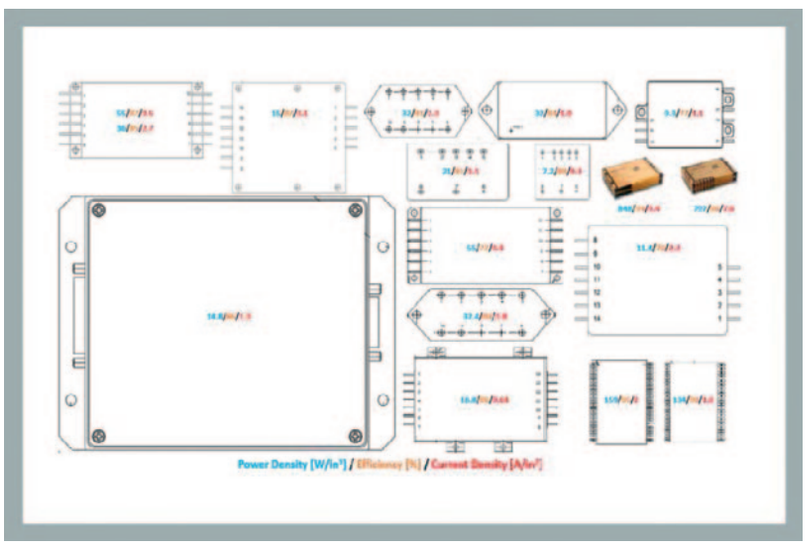

Figure 5: **This diagram compares space-qualified isolated DC-DCs with the BCM and PRM DC-DCs.**

ZVS/ZCS, SAC DC-DC (VTM2919P35K01A5S), which accepts a line voltage from 13.4 to 35V and outputs a fixed load voltage 1/32 of the input, ranging from 0.42 to 1.1V. Its maximum ambient efficiency is specified at 91% in a package size of 29.2×19.0×4.9mm weighing 13.3g.

The four DC-DCs have been designed using a redundant system architecture containing two identical parallel powertrains with fault tolerant control to meet single-event-effect (SEE) requirements. To reduce manufacturing costs, the parts have been packaged in a plated, epoxy-moulded resin BGA with excellent thermal conductivity, branded as **SMChiP™**, compatible with standard surface-mount, pick-and-place, and reflow assembly processes (Figure 3). The DC-DCs are EAR99, specified from –40 to 125°C and offer various overvoltage, short-circuit current, undervoltage, and thermal protection features. The target total-dose is 50kRad (Si) with SEE and other reliability data to be released later this year. Datasheets are available and bespoke input/output options can also be ordered.

To highlight the superior densities offered by the new rad-tolerant DCDCs, Figures 4 and 5 compare their relative sizes with existing space-grade switching POLs and isolated DCDCs respectively. The power density of each convertor in W/in^3, its efficiency in % and current density in A/in^2, have been annotated in blue, orange, and red respectively. A range of efficiencies are typically specified for different load conditions and the maximum values from each datasheet are displayed below.

The new, rad-tolerant, COTS SAC DC-DCs are an innovative and enabling technology for NewSpace applications. When compared with existing qualified converters, they deliver major increases in output power, density, and efficiency in a smaller volume and lighter form-factor. Regulated voltages are significantly cleaner with less bulk decoupling. Parts will have heritage from next year and evaluation boards are available to help you de-risk future mission needs.

The FPA is a major advance to reduce the I2R distribution losses handicapping existing intermediate power architectures. A low-current, factorized bus allows much more freedom to place the BCM® and PRM away from the typically-congested load area.

A modular, 100V PDN solution now exists offering SWaP benefits to supply the latest, ultra-deep-submicron, space-grade semiconductors. The VTMs provide high-performing ratiometric DC-DCs and when combined with a PRM, enable a complete closed-loop FPA exploiting the efficiency advantages of a high-voltage factorized bus (Figure 6).

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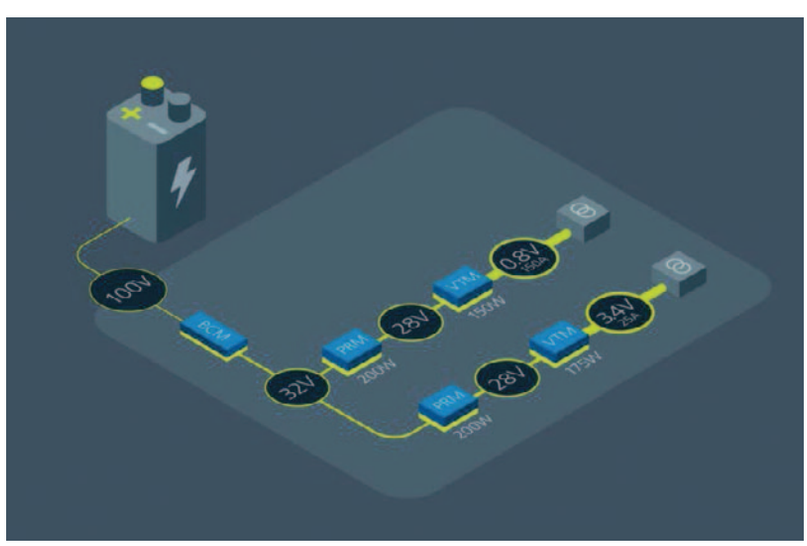

Figure 6: **A modular 100V power-distribution solution now exists for spacecraft avionics.**