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Why gate drivers are key to successful electric vehicle designs

By Allegro MicroSystems

Power-conversion technology plays a key role in every electric vehicle. In a typical vehicle, the on-board charger (OBC) alone has as many as three power-conversion stages in addition to further high-power-conversion stages to drive the traction motors.

When embarking on the design of a new electric vehicle, gate drivers probably are not the first components that come to mind. Yet, choosing the right gate driver technology can cut costs and help designers create more-reliable, more-efficient vehicles.

Gate drivers are key to the design of power conversion systems, whether in electric vehicles or other applications. They enable the flow of large currents through power transistors, which are increasingly moving from silicon insulated gate bipolar transistors (IGBTs) to different transistor structures in materials such as silicon carbide (SiC) MOSFET and gallium nitride (GaN) enhanced mode transistors.

SiC transistors can handle higher voltages—up to 1700 V—and higher currents at higher temperatures than silicon IGBTs, while GaN devices support higher switching speeds—up to 2 MHz—enabling smaller system designs. All these power devices, and there can be many of them at each level of conversion in a design, need to be very robust and reliable to meet strict safety standards in an electric vehicle.

All these switches need different control voltages to be provided from the gate drivers as efficiently and accurately as possible. The gate drivers need to match the requirements of the power switches, and this is key to the performance of the system. The quickness of the switching of the devices and the quality of the output impact the performance of the whole power conversion.

The gate driver also needs to cope with a wide variety of conditions. Gate drivers can be situated on the low-voltage side of a bridge, or on the high-voltage side of the bridge, in the hostile environment of an inverter or in a charger.

As a result, a gate driver's performance is evaluated along multiple criteria: the ability to minimize the cost, size, and weight of the power-conversion modules while maximizing reliability and efficiency. Component count and design complexity influence all of these characteristics in a power-conversion module.

Choices for gate drivers are extensive, and choosing the driver is just where the work begins. Designers also need to provide a source of power to drive the gates of the switches. This can be a challenge. Supplies must frequently be isolated from the controlled ground, and multiple supplies are often required, which can create a new set of design challenges and trade-offs. Therefore, choosing the right gate driver technology can have a big impact on the success of a vehicle in the marketplace. However, it is not easy to find the right solution for a gate driver and its power sub-system.

Delivering reliable gate-drive signal and energy to the gate of any device is the first job of any gate driver, and this needs to be achieved with a low propagation time from the system controller to the FET gate. Low propagation time gives more flexibility for the management of the dead time between the ON and OFF cycles of the power devices, improving system efficiency.

Switch types, such as SiC MOSFETs and GaN transistors, have begun to exhibit improved switching transition speeds in recent years. This means the common mode transient immunity (CMTI) of the gate driver needs to be up to the challenge. Failure to meet this requirement will mean unexpected transitions on the transistor gate and potential destructive events in a system.

Conventional designs drive the gates of

Figure 1: Gate drivers are an increasingly important part of the design of on-board chargers and traction inverters for lithium ion battery systems in electric vehicles.

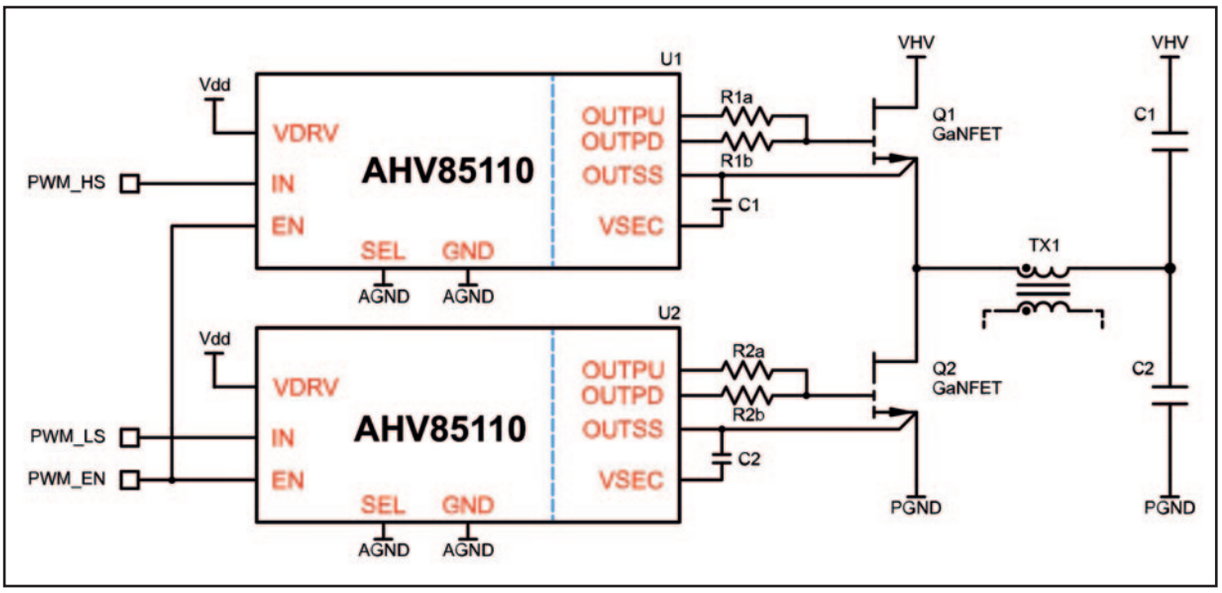

Figure 2: A typical half-bridge application that uses the Allegro MicroSystems AHV85110 gate driver with Power-Thru technology and eliminates the high-side bootstrap.

the power-module semiconductor switches using external DC-DC bias supplies. These designs are both complex and high in component count, and some require as many as eight or nine separate bias supplies, which typically include transformers and other bulky components.

In addition to the added cost, size, and weight that come with these bias supplies, the added component count and circuit complexity affect reliability. Even in designs where care has been taken to minimize the loading and stress on components, every component remains a potential point of failure. The bias supplies included in conventional designs add potential points of failure and must also be sized for the highest operational switching frequency, which results in less-efficient operation at lower frequencies.

ELIMINATING THE BIAS SUPPLY

Power-conversion technologies that require fewer components than conventional technologies have fewer points of failure, which directly improves reliability and leads to fewer potential warranty claims and enhanced product reputation.

One new approach to transfer power to gate drivers, is to use a novel magnetic coupling device within the integrated circuit to eliminate the need for bias supplies, which is what the Power-Thru technology from Allegro MicroSystems does: It transfers the gate on/off logic signal with the power needed to drive the gate of the switch, eliminating the need for external auxiliary power. The reduced component count and complexity cuts engineering time by making modules much easier to design and to qualify. This also allows the gate driver to track the power consumption of the gate control with the switching frequency, enabling automatic optimization of efficiency.

This technology reduces the size and weight of the gate driver and brings additional benefits. Smaller gate driver assemblies enable shorter signal paths with reduced parasitic capacitance and inductance, which reduces the risk of damage caused by ringing and voltage spikes. Smaller gate drivers also leave more space for the power stages, enabling the use of more-efficient designs.

The Power-Thru technology also removes the need for a bootstrap circuit to create the floating voltage required for controlling the high-side switches. This, in turn, eliminates all the trade-offs and complexity in choosing the optimal combination of components to use in this bootstrap circuit.

The Power-Thru technology consists of a tiny magnetic-based isolation structure that enables efficient power transfer across the boundary from the low-voltage signal to the high-voltage system. This boundary carries not only the gate drive signal information but also all the drive power required to drive the external FET switch. The magnetic coupling provides complete electrical isolation, so Power-Thru drivers are equally suitable for use in high-side, low-side, and isolated applications.

By eliminating the need for auxiliary power supplies, the Power-Thru gate drivers can free up time to concentrate on core design challenges.

In one example, nine separate bias rails were able to be merged into a single rail. The reduced component count can reduce BOM costs, system size, and build complexity. This reduced complexity can improve the likelihood of early success in testing and validation and can increase reliability in application as there are less parts that might fail.

The Power-Thru gate drivers also only require a single capacitor to be specified, which speeds design time and improves the likelihood of early design success.

Gate driver operation

For power-on, it is more important to think in terms of charge transfer than simply charging the input capacitance, C_{ISS}, of the FET. FET capacitances are also highly nonlinear, and the capacitance depends largely on the FET V_{DS}.

The high rate of change of voltages and currents in power-switching circuits can create inductor currents and capacitor voltage drops. One example is the false power-on of a FET due to a dv/dt event.

For example, after the power-off of the low-side FET and the elapse of a suitable dead time, power-on of the high-side FET occurs. This produces a rapidly changing switch-node voltage at the drain of the low-side FET. The resulting capacitor current flowing in the gate-drain capacitance, CGD, and driver output cause the voltage on the gate of the low-side FET to rise. If this voltage spike peaks beyond the threshold voltage, V_{TH}, the FET will conduct. Because the high-side FET is also conducting, a potentially destructive shoot-through event can result. As the typical FET capacitors are highly nonlinear and a function of V_{DS}, the effect of iCGD gate drive current can be more pronounced at lower values of V_{DS}.

This inevitable iCGD current must be managed correctly and emphasizes the importance of a strong driver pull down

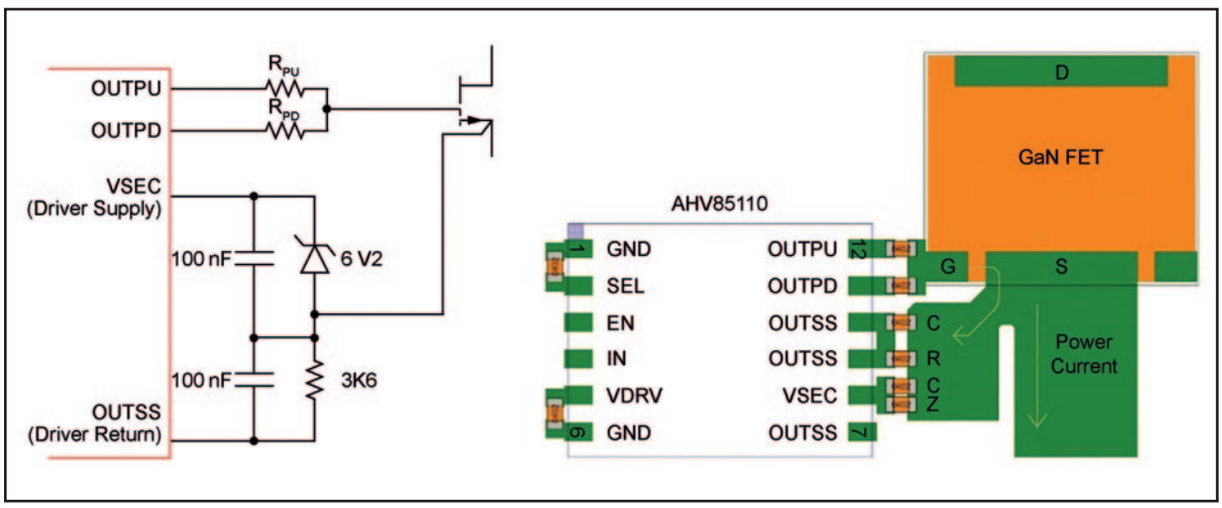

Figure 3: **Avoiding false power-on events in a gate driver design.**

and correct choice of gate resistor. The Allegro AHV85110 driver has independent pull-up and pull-down outputs, allowing independent choice of both resistors.

A popular method to further mitigate the effects of a false power-on event is through use of a bipolar output drive. Here, a suitable choice of driver supply voltage and Zener diode generates a voltage to prevent the false power-on event.

In any electronic circuit, there are many parasitic components that do not appear on the schematic. FET and IC bond wires and packaging along with PCB traces result in unwanted parasitic inductances. FET internal structures and overlapping PCB traces and power planes add circuit node capacitances. In most cases, these parasitic components have little or no impact on circuit performance. However, in power-switching circuits, they can have a severe effect and should be carefully considered. The internal structure, packaging, and pinout of the AHV85110 gate driver have been optimized to minimize such parasitics. The most effective way to reduce the external circuit parasitics is through good PCB layout.

The AHV85110 driver pinout easily facilitates the bipolar drive circuit without compromising on the key PCB layout guidelines.

PCB layout

Increasing the switching frequency can help to reduce the size of the magnet used in the power system, and it is now common to see switching frequencies greater than 500 kHz and even beyond 1 MHz in higher-power converter applications. This increase is further supported by the introduction of high-power, low $R_{DS(ON)}$ and low gate capacitance MOSFETs and GaN FETs.

The gate driver also needs to maximize the effectiveness of these FET switches. Faster switching edges both in the gate drive loop and the commutation loop are a continuous design challenge and the effects of PCB parasitic parameters can play a significant role in circuit operation.

PCB tracking and layout are fundamental parts of the operation of an electronic circuit. The PCB tracks introduce inductances and capacitances into the circuit, which can often be overlooked.

In power-switching circuits, these parasitic components can introduce voltage and current ringing on circuit nodes, which can greatly inhibit circuit performance and introduce undesired effects such as poor circuit operation and increased electromagnetic interference (EMI). A solution is often to add, after the fact, components such as snubbers and filters. A better approach is to eliminate or minimize the effects through good PCB layout practices.

Allegro drivers have the unique advantage in that they require the minimum of external components, particularly on the output side, which is the most critical from a PCB layout point of view. The drivers do not require a separate isolated or bootstrap diode—all of that functionality is included in the drivers using the Power-Thru technology.

The pinout of the device has been carefully designed for ease of PCB layout and optimal performance. The 12-pin, low-profile, surface-mount package (Allegro part number suffix LH) measures 10 mm × 7.66 mm × 2.53 mm. Several protection features are integrated, including undervoltage lockout on primary and secondary bias rails, internal pull-down on IN pin and OUTPD pin, fast response-enable input, and OUT pulse synchronization with first IN rising edge after enable, which avoids asynchronous pulses.

Good quality decoupling capacitors should be used for decoupling the primary, V_{DRV}, and secondary, CSEC, voltages, and the pinout of gate drivers such as the AHV85110 has been designed for the optimal positioning of these capacitors.

The FET drive on pin (OUTPU pin) and the FET drive off pin (OUTPD pin) can be implemented with direct connection to the FET gate or with series resistors to control the FET rise and fall times. Having these functions separated but adjacent on the module allows for independent control of the power-on and power-off times without the need for external parallel diode or transistor circuits, while still allowing the driver to be as close as possible to the driven FET.

The gate drive current return to the module is through the OUTSS pins, which are positioned to minimize the loop area for the gate current.

An example PCB layout is shown for the AHV85110 used with a commercially available GaN FET and following the recommended layout for the FET. The ever-increasing switching frequencies of power converters results in faster voltage and current transition edges—higher dv/dt and di/dt.

This higher-frequency operation, reduced dead time, and sharper switching edges means EMI considerations are also increasingly important yet are often the last considerations in a system design, which can make finishing a design difficult and time consuming. The reduction of components and circuits in and around the gate drive design helps dramatically reduce the EMI challenge in a system design through lower common-mode capacitance (Ccm). This reduces the circulating currents, reducing any EMI and reducing test time.

Good PCB layout practices can significantly reduce second-order effects, such as EMI, and can reduce or eliminate

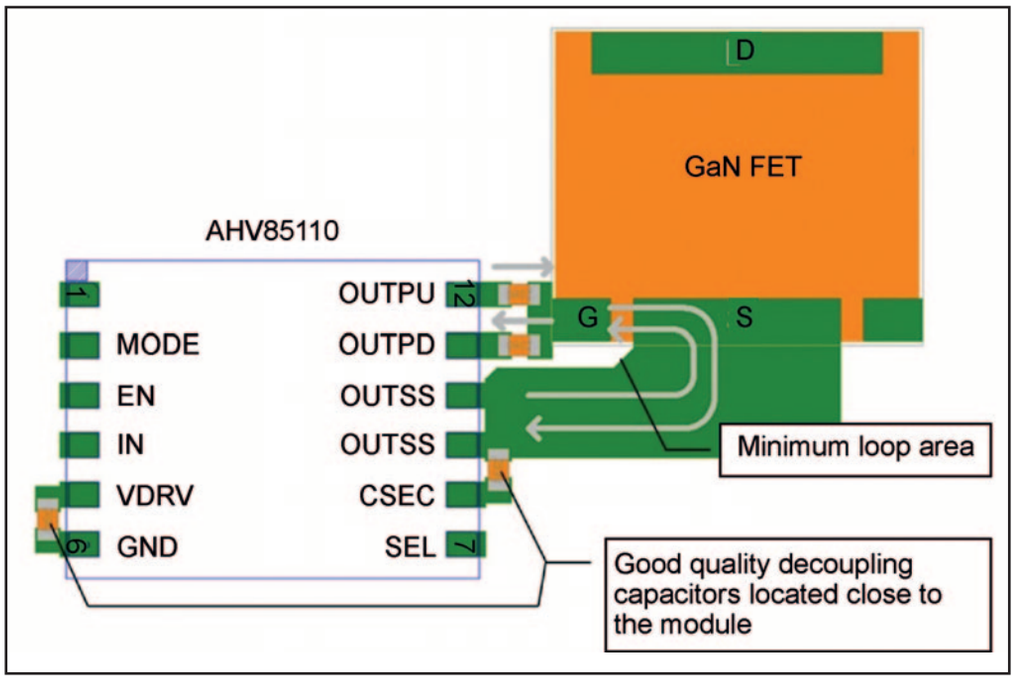

Figure 4: How the gate driver pinout reduces current loops in the PCB.

the need for circuits such as snubbers or filters required to manage these phenomena. Allegro has developed the AHV85110 and AHV85111 isolated GaN and MOSFET drivers with Power-Thru magnetic isolation to make this process easier, resulting in more effective gate drive designs.

Evaluation

The Allegro APEK85110 Half-Bridge Driver Switch Board is a demo board containing two AHV85110 gate drivers and two GaN FETs in a half-bridge configuration. This can be used to perform double pulse tests or to interface the half bridge to an existing LC power section. The isolated AHV85110 driver does not require secondary-side power or bootstrap components. Gate drive power is supplied to the secondary side from the primary-side supply voltage, V_{DRV}, and the amplitude of the gate drive can be varied by varying V_{DRV} between 7 and 15 V.

The evaluation board uses a bipolar gate drive arrangement, which is useful to mitigate against the effects of gate-drain capacitor currents. The secondary supply voltage is a function of the primary supply voltage and the Zener diode regulates the positive power-on voltage of the GaN FET. During the power-off period, the gate voltage is negative to allow more margin before the threshold voltage can be reached.

Ensuring availability

To keep production lines running, availability of devices is also key amidst a shortage of components for automotive designs. Car makers around the world have suffered from shortages of components such as gate drivers, and designers are increasingly aware of the supply chain issues of the devices they use.

The innovative magnetic isolation of the Allegro Power-Thru devices is built on standard 180 nm CMOS technology from dual-sourced tier one fabs, allowing flexibility of sourcing. Industry-leading packaging vendors and a range of second-source strategies are also used to ensure a secure supply of devices for some of the smallest high-voltage and high-efficiency power systems available.

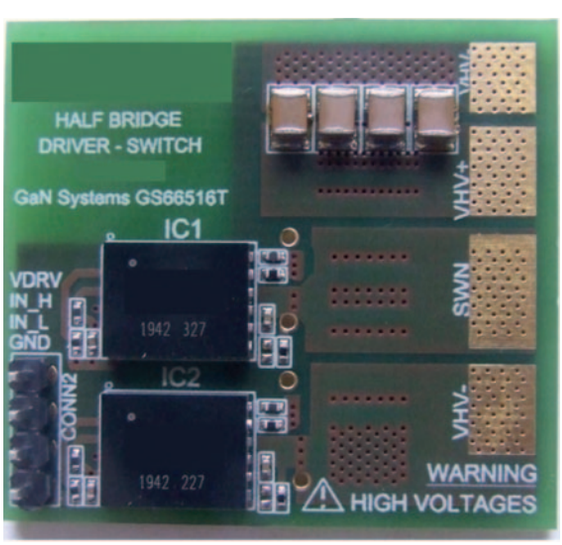

Figure 5: The APEK85110 half-bridge driver switch board.board.

Conclusion

The choice of gate driver is a key decision in the development of the power system of an electric vehicle. Whether this is a car, scooter, mining dump truck or tractor, the gate driver is there, controlling the power transistors in any power-conversion system.

The move to SiC and GaN transistors means there are many more factors for a designer to consider. The higher power, higher temperatures, and higher frequencies used with these devices are putting more focus on reliability of the design, which in turn is driving a reduction in the number of components. Smaller weight and size are also driving down the size of designs. All of this is driving up the levels of integration and the demands on the gate driver devices.

The Power-Thru magnetic isolation in the Allegro gate drivers enables higher levels of integration that can help to address issues such as EMI and parasitic effects on the board, reducing the time needed to design, test, and certify a system.

All these factors—along with the secure supply of the components in the design—must be considered when designing a power system for an electric vehicle.