eGaN FETs enable more than 4 kW/in³ power density for 48 V to 12 V power conversion

GaN transistors in Chip Scale Package (CSP) enable higher than 4 kW/in3 power density for 48V to 12V power conversion using an LLC resonant converter with up to 1 kW capability.

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Introduction

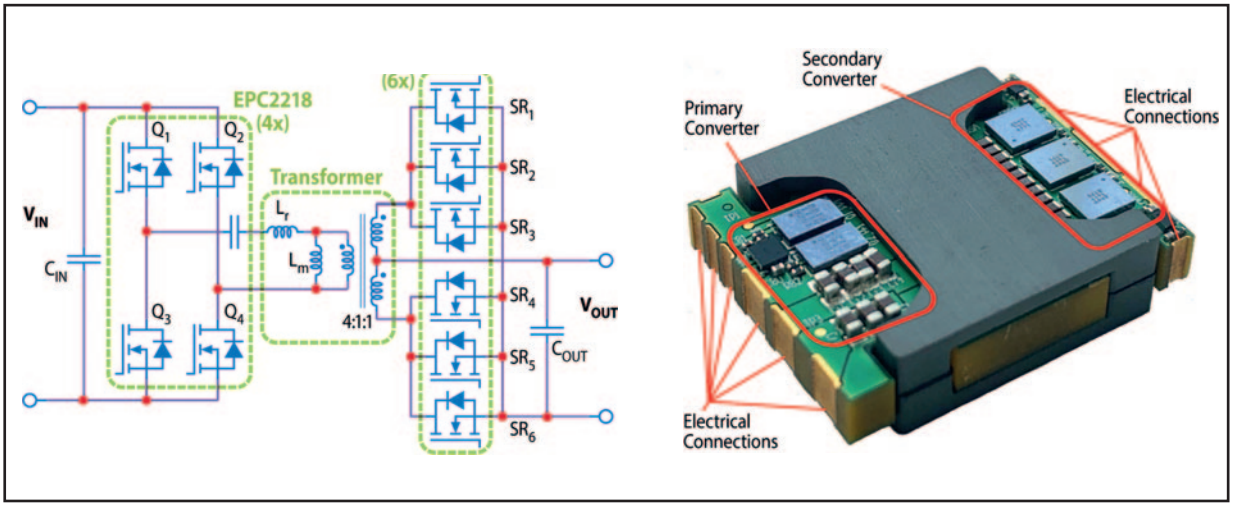
Growing computational power and miniaturization of electronics in computing and datacenters is increasingly putting pressure in 48 V power delivery and conversion systems. High efficiency and high-power density converters enable a reduction in power losses at the system level while allowing smaller form factors. In this context, LLC resonant topologies combined with GaN technology succeed to deliver outstanding performance, as it has been demonstrated with multiple examples [1-4]. This article will show the key design parameters and components to achieve beyond 4 kW/in3 of power density in a 48 V to 12 V LLC converter using eGaN FETs. This work is an evolution of [2] and it was first introduced in [1], demonstrating 96.3% peak efficiency and 93.8% when delivering 1 kW into a 12 V load and with module dimensions of 17.5 x 22.8 x 7.7 mm.

Converter Overview

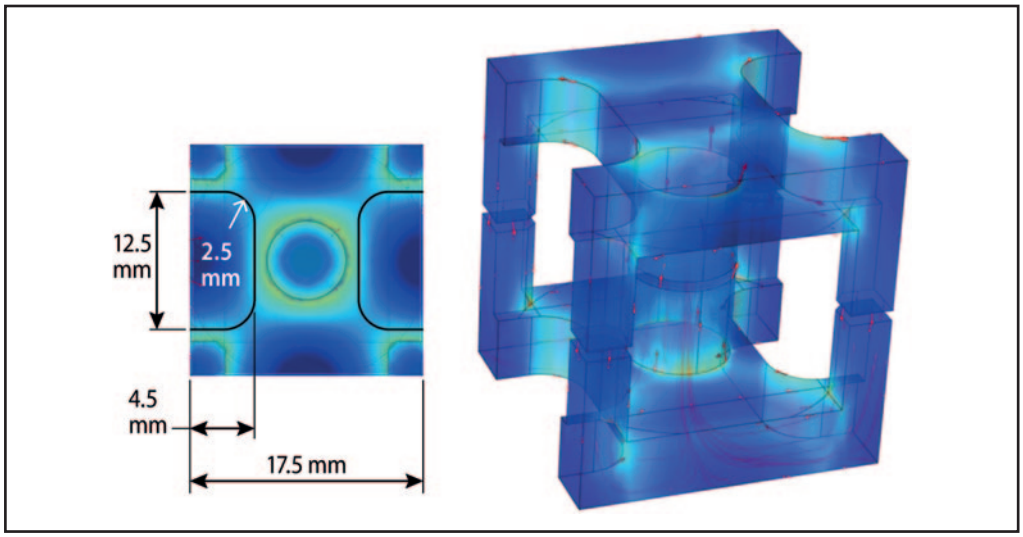
The LLC resonant converter presented here features a primary full bridge and a center-tapped full wave synchronous rectifier for the secondary as shown in Fig 1 (left). Both are coupled with a planar transformer having a 4:1 turns ratio. The power FETs used in the primary and secondary, together with the transformer and printed circuit boards are the key components of the module. Figure 1 (right) shows a photo of the overall module assembled

Power Transistors and Gate Drivers

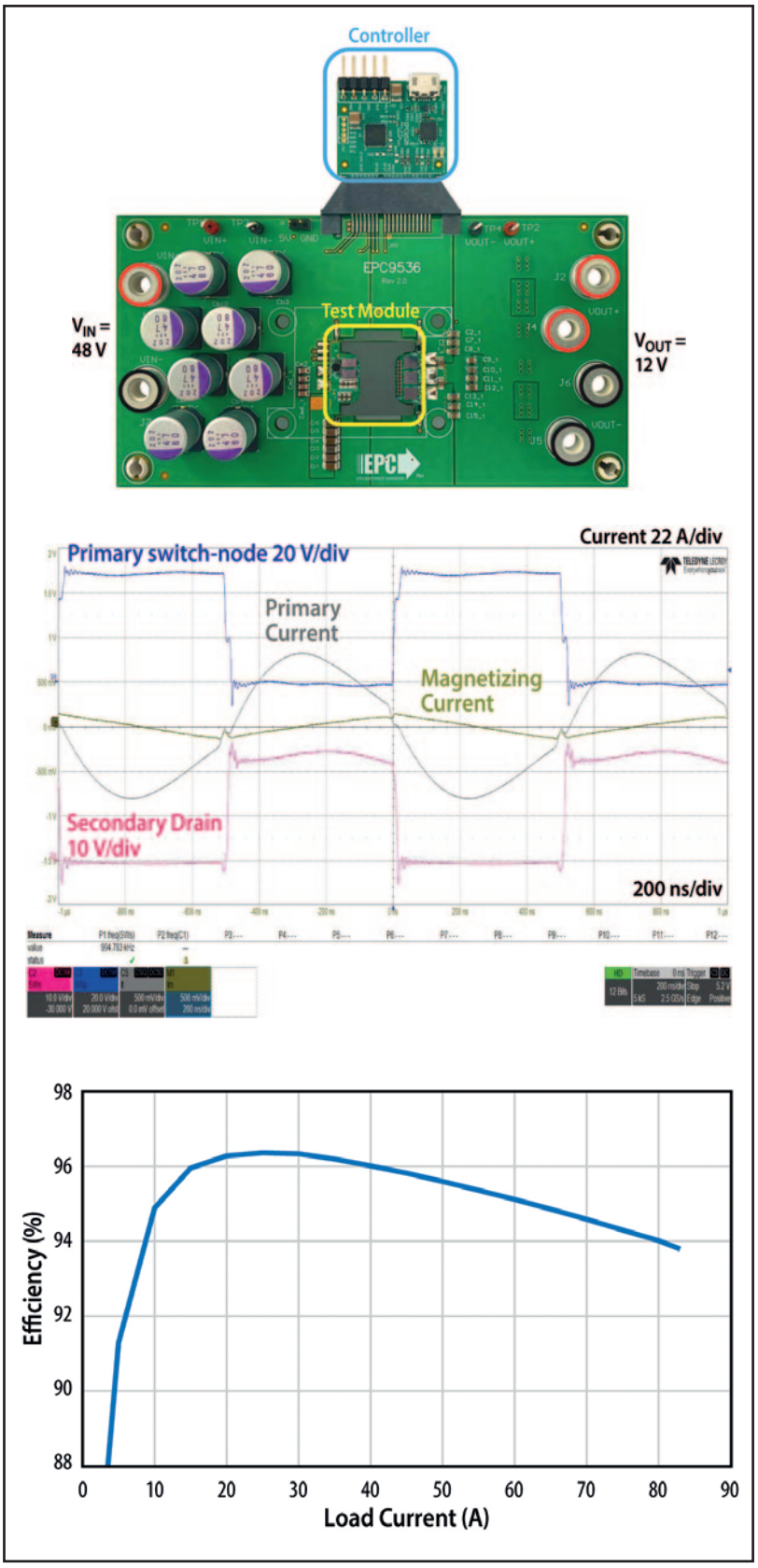
For the primary circuit, four 100 V rated



ABOVE: Fig. 1 **(left) Topology of the LLC converter, (right) photo of the assembled LLC power converter module**



RIGHT: Fig. 2 **(left) top view and dimensions of optimised core (right) full FEA model of the core showing the flux density throughout the core**



LEFT: Fig. 3 (top) Photo of the test system assembled, (centre) measured waveforms, (bottom) measured efficiency at V_{in} = 48 V

3.2 mΩ EPC2218 [5] are used in conjunction with two uP1966E [6], a half-bridge gate driver ICs. For the secondary rectifier, a total of six 40 V rated 1.55 mΩ EPC2067 [7] are used as synchronous rectifiers. These six transistors are divided into two branches, where each branch consists of an LMG1020 [8] low side gate driver controlling a parallel array of three EPC2067s. All power transistors and gate drivers are in CSP format for minimum size and lowest parasitic elements.

The choice of eGaN transistors is especially advantageous in the primary given the low RDS(on) * COSS figure of merit compared to equivalent Si MOSFETs. This is because for a similar RDS(on) and voltage rating, GaN transistors offer lower COSS, therefore minimizing the magnetizing current needed to achieve ZVS in as short transition time as possible. As a result, the frequency can be increased to the 1 MHz range enabling size reductions in the passive components while maintaining high efficiency.

The uP1966E half-bridge gate drivers used for the primary are an ideal match for this application where a minimum of 80V rating and minimum size and external components are key features. Similarly, the LMG1020 offers a tailored solution for this socket, given its minimum footprint and supporting circuitry required, as well as sufficient strength capable of driving the three paralleled EPC2067 FETs without compromising speed.

While the components listed above enable very high operating frequencies in a very compact form, some challenges arise from the different propagation delays between primary and secondary gate drivers. To overcome these mismatches, 3 unique PWM generators with independent dual edge control are used to align the desired synchronization between primary and secondary circuits. Such configuration provides the programmable flexibility needed to ensure a balanced square waveform in the primary, with control of the dead time to realize ZVS in the primary and maintain ZVS/ZCS in the rectifier transistors and minimize circulating energy.

Transformer Design

The transformer design and choice of core material are driven by the converter requirements, input/output voltage ratio of

4:1, desired output power of 1 kW at 1 MHz resonant frequency, and maximum size of 17.5 mm x 23 mm. Building on the experience from previous work [1,2] and aided by Finite Element Simulations a core shape with a single 6 mm diameter center post and four satellite flux return legs was designed and shown in Figure 2 (right). The 6 mm diameter for the center post was found to be the optimal dimension considering conduction losses in the copper windings and core losses, as analyzed in [1]. The final dimensions of the top and bottom side caps of the core shown in Figure 2 (left) are a compromise between flux density and magnetic core utilization, to open areas for placing components without increasing core losses. Note that the PCB real state close to the transformer windings is of utmost interest to minimizing parasitic inductance. As reported in the literature, this parasitic inductance in the secondary is detrimental to the performance by as much as 30% [4].

ML91S [9], the same soft-ferrite material used in prior work [2], was used for the transformer core. It provides good stability over temperature and frequency, even beyond 1 MHz, as well as less than 200 kW/m3 of flux density volumetric power loss. The airgap between the two core halves was tuned to realize a magnetizing inductance of approximately 1.8 µH.

PCB Design

With the transformer core dimensions defined, the primary and secondary windings were distributed over 16 layers routing the current around the center post of the transformer core. A single 3oz per layer was dedicated to each primary turn and three 3oz layers and one 2oz layer were paralleled for each branch of the secondary. The inner twelve layers are fabricated with standard PCB technology, whereas HDI technology was utilized for the outer layers. This way the primary and secondary components can be placed on the top and bottom sides of the board and the current efficiently routed down into the transformer windings.

Testing Results and Next Steps

To test the converter described in the previous sections, a motherboard was developed to provide input/output connections for the module, additional bus capacitance, housekeeping power supplies, sense connections for accurate efficiency measurements, and a connector for the controller board. A photo of the setup is provided in Fig. 3 (left), along with waveforms at full load (center) and the efficiency curve (right). Peak efficiency of 96.3% could be measured at 25 A and 93.8% at 84 A (1 kW).

In the next iteration of the converter, the controller and housekeeping power supplies will be integrated in the module while maintaining the same overall size. Moreover, a small resonant inductor will be added in series with the transformer to increase the Q factor while maintaining the same resonant frequency. The PCB will also experience changes as the 16-layer board will be replaced with a two-PCB solution to reduce copper losses and improve manufacturability of the overall system.

Conclusions

The module presented in this article demonstrates that GaN FETs can enable unprecedented levels of power density (>4 kW/in3) in 48 V to 12 V power converters, such as those needed in datacenters with a 48 V architecture. In particular, the combination of GaN technology featuring chip-scale packaging like those of eGaN transistors, and carefully designed magnetics, allow 1 kW load capability at 1 MHz frequency with peak efficiencies and full load efficiency of 96.3% and 93.8% respectively.

References

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