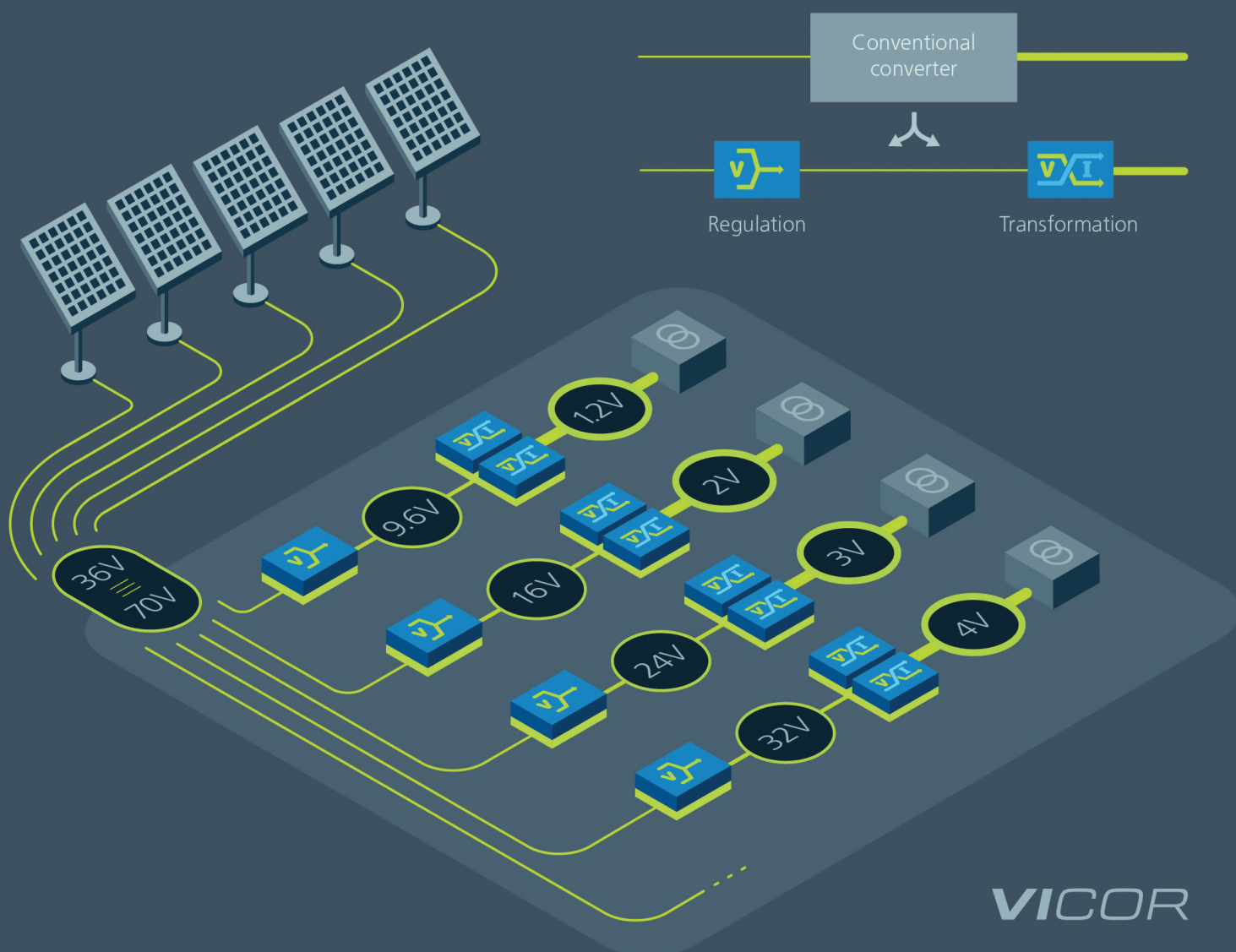


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Factorized Power Accelerates Coral Reef Restoration



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Editor Achim Scharf

Tel: +49 (0)892865 9794
 Fax: +49 (0)892800 132
 Email: PowerElectronicsEurope@t-online.de

Production Editor Chris Davis

Tel: +44 (0)1732 370340

Financial Manager Clare Jackson

Tel: +44 (0)1732 370340
 Fax: +44 (0)1732 360034

Reader/Circulation Enquiries

Perception
 Tel: +44 (0) 1825 701520
 Email: dfamedia@dmags.co.uk

INTERNATIONAL SALES OFFICES**Mainland Europe:**

Victoria Hufmann, Norbert Hufmann
 Tel: +49 911 9397 643 Fax: +49 911 9397 6459
 Email: pee@hufmann.info

Eastern US

Karen C Smith-Kernc
 email: KarenKCS@aol.com

Western US and Canada

Alan A Kernc
 Tel: +1 717 397 7100
 Fax: +1 717 397 7800
 email: AlanKCS@aol.com

Japan:

Yoshinori Ikeda,
Pacific Business Inc
 Tel: 81-(0)3-3661-6138
 Fax: 81-(0)3-3661-6139
 Email: pbi2010@gol.com

Taiwan

Prisco Ind. Service Corp.
 Tel: 886 2 2322 5266 Fax: 886 2 2322 2205

Publisher & UK Sales Ian Atkinson

Tel: +44 (0)1732 370340
 Fax: +44 (0)1732 360034
 Email: ian@dfamedia.co.uk
 www.power-mag.com

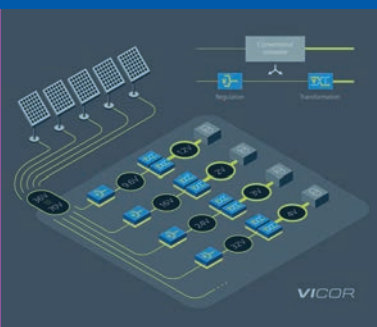
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**FEATURE STORY****Factorized Power Accelerates Coral Reef Restoration**

According to the latest figures over 70% of the world's coastlines are eroding, with 200 million people worldwide reliant on the protection that coral reefs offer. With 99% of remaining reefs projected to disappear by 2040, communities and livelihoods are at risk in areas such as Mexico, Indonesia and numerous smaller island habitats around the world. CCell uses renewable energy sources such as solar, wind and wave energy to power their reef growing systems. To drive a precisely calculated current through the seawater, Vicor recommended its FPA for efficiently converting wide-range, renewable energy into precision power delivery for the point of load. The mission of CCell Renewables is to combat coastal erosion and enhance marine ecosystems by restoring damaged coral reefs and growing new ones on a large scale. The technique is based on the electrolysis of seawater can produce incredibly strong limestone rock. More details on page 21.

Cover image supplied by Vicor corp., USA

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Market News

PEE looks at the latest Market News and company developments

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SiC MOSFET Technology with Silicon-Like Reliability

The performance potential of SiC is indisputable. The key challenge to be mastered is to determine which design approach achieves the biggest success in applications. Advanced design activities are focusing on the field of specific on-resistance as the major benchmark parameter for a given technology. However, it is essential to find the right balance between the primary performance indicators like resistance and switching losses and the additional aspects relevant for actual power electronics designs, e.g. sufficient reliability. **Dr. Peter Friedrichs,**

Infineon Technologies, Neuburg, Germany

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The New Brave Virtual World

The world is in the midst of a crisis of hitherto unseen proportions due to Covid-19 since March. The effects of the Corona virus pandemic are unprecedented, and the semiconductor industry is significantly feeling the impact. Also Infineon for instance is not immune to such a massive slump in the global economy. According to Infineon's CEO the company have largely been able to maintain operations in recent weeks. Nevertheless, the outlook for the second half of the fiscal year has significantly deteriorated. Expected is a sharp drop in revenue in the Automotive segment. The Industrial Power business envisions a downswing in home appliances and photovoltaic; but expects a quick rebound; delayed impact in drives, traction and wind followed by slow recovery.

In this crazy pandemic world (including banning of Europeans to enter the USA by President Donald Trump) a lot of events such as APEC in New Orleans, ISPSD in Vienna, PCIM or ECPE Tutorials have been postponed, canceled and/or reorganized as a virtual event. Even the Hawaiian (USA state) tourists looking for attending the VLSI Symposia 2020 can sit in their (home)office and take part virtually (see our event calendar under www.power-mag.com). This situation might be comfortable for a few but is causing heavy (financial) losses for the organizers, local infrastructures such as hotels and public transport, exhibitors, speakers and last but not least attendees as well as trade magazines.

APEC were able to publish most of its technical content, to minimize losses and finally offer substantial refunds to all participants. But perhaps most disappointing of all was the fact

that APEC 2020 was supposed to celebrate the conference's 35th anniversary. A lot of effort went for naught. "We did discuss how to take the conference virtual," Exposition Co-Chair Van Niemela said. "Of course, the Chinese authors had to pull out first, and we made arrangements to record their oral presentations. Then, when it became clear that the entire conference would have to be canceled, we made the conference proceedings and many presentations available to registrants electronically. However, the exposition which I co-chaired is a different beast, relying heavily on face-to-face discussions between potential suppliers and customers. We did not see a good way to do this virtually. Therefore, we offered full refunds to exhibitors, and we're focused on making the APEC '21 the excellent event we've come to expect."

Indeed it is not too early to start thinking about APEC 2021. The challenges of wrapping up APEC 2020 have caused some delay. But already planning for APEC '21 in Phoenix next March is ongoing. "And in this planning cycle, we're including a clear contingency plan in case it becomes necessary to cancel, including full refunds for all exhibitors and partners as we've been able to offer for APEC 2020. We certainly hope to see everyone at APEC '21, but we'll cancel again if necessary and plan for an even bigger APEC 2022 in Houston," Van Niemela underlined.

PCIM 2020 will go another way. Due to the increasing spread of Covid-19 in Europe and the associated ban on all major German events up to, and including the end of August, the PCIM Europe exhibition and conference 2020 in Nuremberg has already been postponed from May to July 2020, and will now in-person take place again next year - hopefully. But a virtual format will offer a digital alternative for knowledge transfer on July 7 - 8 2020. According to organizer Mesago participants can look forward to an interactive new event format. During the "PCIM Europe digital days", exhibitors and international speakers will present the latest trends and developments in power electronics on a virtual platform. Expected are numerous presentations on-demand and virtual round tables. In live chats, participants will have the opportunity to talk to exhibitors and speakers from industry and academia directly. In addition, a matchmaking tool will give the opportunity to make contacts with attendees, exhibitors and speakers. The virtual conference program will include the announced keynotes, presentations and round tables. The conference proceedings containing the manuscripts of all oral and poster presentations will be available in June.

For potential exhibitors Mesago have compiled various digital packages to present products and attract customers. The basic package costs 2,990 Euro, the premium package 4,990 Euro (limited to 30 companies), and the sponsor package 10,990 Euro (limited to 5 companies).

But all these activities cannot replace in-person events where networking is essential – also for journalists gathering all the rumors and news circulating in the power electronics industry and community. Nevertheless, PEE will keep you informed on what is going on in power electronics!

Enjoy reading.

Achim Scharf
PEE Editor

Solar and Wind Gains Competitiveness

Solar PV and onshore wind are now the cheapest sources of new-build generation for at least two-thirds of the global population. Those two-thirds live in locations that comprise 71 % of gross domestic product and 85 % of energy generation. Battery storage is now the cheapest new-build technology for peaking purposes (up to two-hours of discharge duration) in gas-importing regions, like Europe, China or Japan.

Recent analysis by research company BloombergNEF (BNEF) shows that the global benchmark levelized cost of electricity, or LCOE, for onshore wind and utility-scale PV, has fallen 9 % and 4 % since the second half of 2019 – to \$44 and \$50/MWh, respectively. Meanwhile, the benchmark LCOE for battery storage has tumbled to \$150/MWh, about half of what it was two years ago. Onshore wind has seen its most significant drop in cost since 2015. This is mainly due to a scale-up in turbine size, now averaging 4.1 MW, and priced at about \$0.7 million per MW for recently financed projects. Best-in-class onshore wind projects in Brazil can achieve an LCOE of \$24 per MWh, the lowest globally. Meanwhile top projects in the US, India and Spain follow at \$26, \$29 and \$29 per MWh respectively, excluding subsidies such as tax-credits. In China, the largest PV market, the solar benchmark is at \$38/MWh, down 9 % from the second half of 2019, following a rapid uptake in better performing monocrystalline modules. New-build solar in the country is now almost on par with the running cost of coal-fired power plants, at an average of \$35/MWh. This is significant as China advances on its deregulation agenda, opening up competition in the power sector.

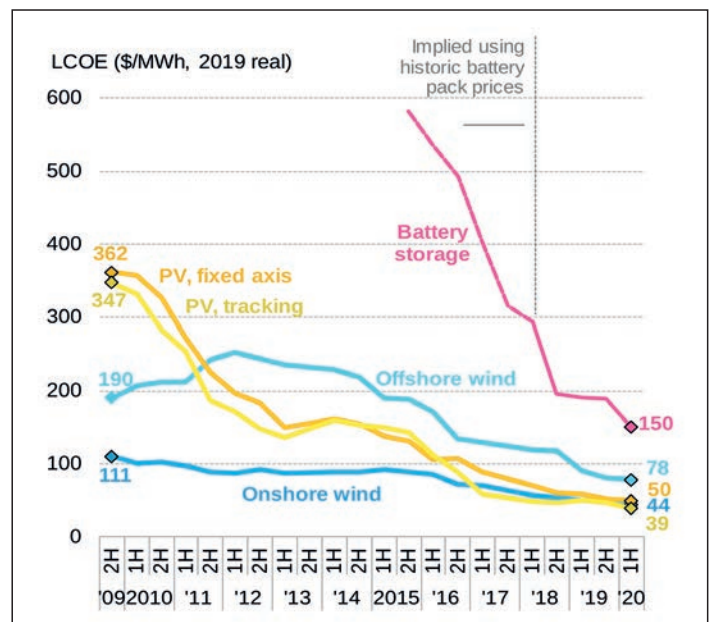
Globally, BNEF estimate that some of the cheapest PV projects financed in the last six months will be able to achieve an LCOE of \$23-29 per MWh, assuming competitive returns to their equity investors. Those projects can be found in Australia, China, or Chile, where they will challenge the existing fleet of fossil fuel power plants. "There have been dramatic improvements in the cost-competitiveness of solar and wind. Part of it is due to photovoltaic and wind technology getting better at extracting renewable resources. But our analysis also suggests that since 2016, auctions are forcing developers to realize cost savings by scaling up project size and portfolios. Larger scale enables them to slash balance-of-plant, operations and maintenance expenses – and have a stronger negotiating position when ordering equipment," BNEF analyst Tifenn Brandily commented. He estimates that the average onshore wind farm has doubled its capacity from 32 MW in 2016 to about 73 MW today. Solar farms are a third more powerful today, at 27 MW on average, compared to 2016. On current trends, the LCOE of best-in-class solar and wind projects will be pushing below \$20 per MWh this side of 2030. A decade ago, solar generation costs were well above \$300, while onshore wind power hovered above \$100 per MWh.

Battery storage is another example of how scale can unlock cost reductions. Today, BNEF estimates that the average capacity of storage projects sits at about 30 MWh, a fourfold rise compared to just 7 MWh per project four years ago. Since 2018, increasing project sizes combined with a rapidly expanding manufacturing base and more energy dense chemistries, have halved the LCOE of energy storage. BNEF's global LCOE benchmark sits now at

\$150/MWh for battery storage systems with a four-hour duration. China is home to the cheapest storage levelized costs globally, at \$115 per MWh. This competitive advantage hinges mainly on the proximity of developers to the equipment supply chain and the more widespread use of cheaper LFP (lithium iron phosphate) chemistries. In comparison, the levelized cost of open-cycle gas turbines per megawatt-hour sits today between \$99 in the US and \$235 in Japan, with China at \$145.

The Chinese behemoth that makes electric-car batteries for Tesla Inc. and Volkswagen AG developed a power pack that lasts more than a million miles – an industry landmark and a potential boon for automakers trying to sway drivers to their EV models. Contemporary Amperex Technology Co. Ltd. is ready to produce a battery that lasts 16 years and 2 million kilometers (1.24 million miles), Chairman Zeng Yuqun said. Warranties on batteries currently used in electric cars cover about 150,000 miles or eight years, according to BloombergNEF. Extending that lifespan is viewed as a key advance because the pack could be reused in a second vehicle. That would lower the expense of owning an electric vehicle, a positive for an industry that's seeking to recover sales momentum lost to the coronavirus outbreak and the slumping oil prices that made gas guzzlers more competitive.

<https://about.bnef.com/>



Global LCOE benchmarks – PV, wind and batteries (country weighted-average using the latest annual capacity additions. The storage LCOE is reflective of utility-scale projects with four-hour duration, it includes charging costs)
Source: BloombergNEF

Overall Car Market Expected to Shrink by 23 Percent

Sales of electric passenger vehicles are forecast to fall 18 % in 2020, to 1.7 million worldwide – with the coronavirus crisis interrupting ten successive years of strong growth. However, sales of combustion engine cars are set to drop even faster this year (by 23 %), and the long-term electrification of transport is projected to accelerate in the years ahead.

The annual Long-Term Electric Vehicle Outlook, published in May by BloombergNEF (BNEF), shows electric models accounting for 58 % of new passenger car sales globally by 2040, and 31

% of the whole car fleet. They will also make up 67 % of all municipal buses on the road by that year, plus 47 % of two-wheelers and 24% of light commercial vehicles. The figures have major implications for oil and electricity markets. Transport electrification, particularly in the form of two-wheelers, is already taking out almost 1 million barrels of oil demand per day and by 2040 it will remove 17.6 million barrels per day. Electric vehicles (EVs) of all types are seen adding 5.2 % to global electricity demand by 2040. "The Covid-19 pandemic is set to cause a major

downturn in global auto sales in 2020. It is raising difficult questions about automakers' priorities and their ability to fund the transition. The long-term trajectory has not changed, but the market will be bumpy for the next three years," commented Colin McKerracher, head of advanced transport for BNEF.

BNEF's analysis suggests that global sales of internal combustion engine, or ICE cars, peaked in 2017 and will continue their long-term decline after a temporary post-crisis recovery. For the first time, BNEF sees overall new passenger vehicle

sales peaking in 2036 as changing global demographics, increasing urbanization and more shared mobility outweigh the effects of economic development – though the fleet size keeps growing. Electric models are seen accounting for 3 % of global car sales in 2020, rising to 7 % in 2023, at some 5.4 million units. Further falls in lithium-ion battery prices will mean that the lifetime and upfront costs of an electric car ‘cross over’ with those of ICE equivalents in around

2025, on average. However, the date will vary greatly depending on the market, as early as 2022 for large cars in Europe but 2030 or after for small ones in India and Japan.

This year’s Outlook breaks new ground in examining prospects for the growth of electric two-wheelers and fuel-cell vehicles. It sees the latter technology accounting for 4 % of heavy-duty commercial vehicle sales and 6.5 % of municipal bus sales globally by 2040, but with higher shares

in East Asia and parts of Europe. Fuel cells are not seen encroaching far into lighter-duty commercial or passenger car markets.

The report sees fully autonomous vehicles or ‘robotaxis’ beginning to play a much larger role in the late 2030s, helped by the growing deployment of advanced driver assistance systems, or ADAS, and the build-out of sensor supply chains.

<https://about.bnef.com/>

EV/HEV Market Drives Power Semiconductors

The EV/HEV race has begun. More than \$300 billion of EV/HEV investments have been announced by different OEMs, clearly confirming the automotive industry’s commitment to governmental CO2 reduction targets.

According to Yole Développement the market figures are promising. In 2018, 1.32 million battery electric vehicles (BEV) were purchased, along with 0.75 million plug-in hybrid electric vehicles (PHEV) - compared to 0.78 million resp. 0.41 million units in 2017. This equates to year-over-year growth of 68 % and 84 %, respectively. Moreover, sales of other hybrid cars have also increased. Driven by the prosperous EV/HEV market, the market for power semiconductor electronics devices should have a bright future, with value exceeding \$3.7 billion in 2024 at a 2018 - 2024 CAGR of 21 %. IGBT modules represent the largest market, which is expected to double in five years. SiC power modules will also grow fast, with a 2018 - 2024 CAGR of 48 %.

A large variety of different technology approaches is typical of the EV/HEV industry, which is far from being consolidated on the technology end or the supply chain end. Nevertheless, several main technology trends have been identified by Yole. Fast scaling of battery manufacturing capacities, significant battery cost reduction, and regulatory changes have accelerated the transition towards stronger vehicle electrification and full EVs.

Modular vehicle platforms like the Volkswagen MEB enable cost reduction and reduce development time for new car models. A higher integration of different systems and subsystems enables automakers to use less parts - thus reducing cost, weight, and volume. In an electric axle (e-axle) electric motor, power electronics and gears are integrated in one compact system. The e-axle approach has strong support from Tier1 companies like Bosch, Schaeffler, GKN, and others, which see e-axle as a more complete EV/HEV solution to offer to different automotive OEMs.

Trends towards higher vehicle power and larger battery capacity have led to a new 800 V battery-voltage level in passenger cars. A rapidly growing market like EV/HEV brings not only plenty of opportunities, but also many challenges for players across the supply chain. Regarding EV/HEVs, conventional internal combustion engine (ICE) vehicle manufacturers are now at the same starting line and competing with newcomers like Tesla, the #1 BEV vendor so far. ICE automakers must invest significant effort to balance EV/HEV development with

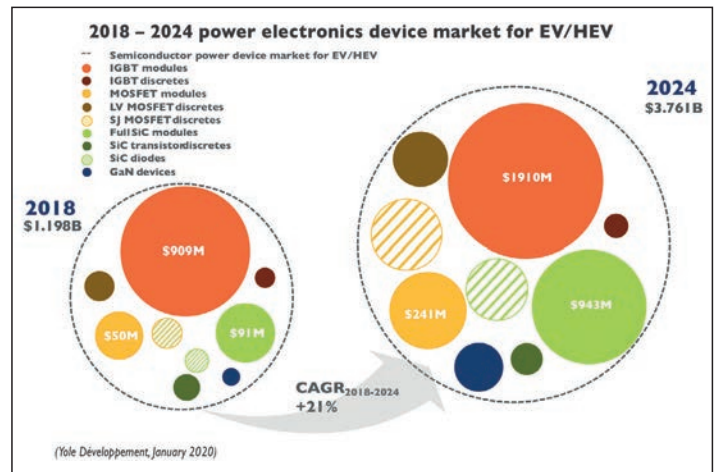
their existing ICE activities during a “transition period” – the length of which is hard to determine because of rapidly-changing incentive mechanisms and evolving customer needs.

To compensate, Tier1s are increasing their efforts in EV/HEV-related products. However, OEMs are becoming more and more intrusive, particularly in main inverters, with the objective of controlling the key EV/HEV elements. Established semiconductor device suppliers are in a similar situation, on the one hand facing the entrance of some Tiers 1’s in the device market, and addressing challengers from the emergence of WBG devices on the other.

China has different levels of technology and independency. Regarding battery, China has top suppliers like CATL and BYD. However, the majority of IGBT power modules used in

Chinese cars are still manufactured outside of China, which is not a sustainable solution for the Chinese industry and particularly for China’s government.

www.yole.fr



Infineon Reports Significantly Weaker Outlook

The world is in the midst of a crisis of hitherto unseen proportions. The effects of the coronavirus pandemic are unprecedented, and the semiconductor industry is significantly feeling the impact. Also Infineon is not immune to such a massive slump in the global economy.

“Our company is accustomed to coping with crisis situations. Despite all the difficulties, whether supply chain-related or in manufacturing, we have largely been able to maintain our operations in recent weeks. We also put cost-containment measures in place at an early stage. Nevertheless, the outlook for the second half of the fiscal year has significantly deteriorated. We expect a sharp drop in revenue in

the Automotive segment. We are monitoring the situation in our target markets very closely and are prepared to respond swiftly to a variety of possible scenarios,” Infineon’s CEO Dr. Reinhard Ploss stated. “Even in difficult times, Infineon continues to evolve. With the successful acquisition of Cypress, we are taking a major step forward in implementing our strategy of linking the real with the digital world.” Based on an assumed exchange rate of US\$1.10 to the Euro, revenue is expected to be around €7.6 billion excluding Cypress and around €8.4 billion including Cypress. This level of revenue would represent a 5 % decrease compared to the previous fiscal year.Regarding Infineon’s Industrial

Business Dr. Peter Wawer, Division President Industrial Power Control (IPC) envisions a downswing in home appliances and photovoltaic; but expects a quick rebound; delayed impact in drives, traction and wind followed by slow recovery.

www.infineon.com



“Even in difficult times, Infineon continues to evolve,” states CEO Reinhard Ploss by presenting 2Q 2020 results

Silicon Germanium (SiGe) Rectifiers Offers Fast Switching and Extraordinary SOA

For many circuit designs, the main challenges are integration of more functions per space, design for highest efficiency, and system miniaturization. SiGe rectifiers are an ideal solution, providing the benefits of high efficiency, ease of thermal design, and a small form factor. Low forward voltage and low Q_{rr} in combination with extremely high thermal stability are the main product features.

Nexperia's new SiGe rectifiers are housed in the clip-bonded FlatPower (CFP) packages CFP3 and CFP5. They are all AEC-Q101 compliant and qualified to $T_j = 175^\circ\text{C}$.

The SiGe diode is compared here with four other diodes which are specified for the same operation range and same packaging but hold different layer structures, namely Trench Schottky, Planar Schottky and PN diodes. This benchmark was performed in cooperation between the Helmut-Schmidt-Universität /Universität der Bundeswehr Hamburg and Nexperia. The more detailed final paper, authored by Ali Aneissi, Michael Meissner, K.F. Hoffmann (University Hamburg), and Reza Behtash, Sebastian Fahlbusch (Nexperia), will be presented by Ali Aneissi within the PCIM 2020 Digital Days.

State-of-the-art recap of diode technologies

It is important to note that the performance of the diodes can significantly differ from datasheet ratings in the presence of high speed switching.

Ideally, the switching speed of Schottky diodes is supposed to be determined by their parasitic junction capacitance only, as they are unipolar devices. However, the cross section of a Planar Schottky diode reveals that this is not necessarily the case. At the edges of the active area the device needs to be electrically terminated in a proper way in order to relieve the crowding of the electrical field and to avoid early breakdown and high leakage current.

This is accomplished by implanting p^- dopants into this area. The so-called guard ring structure reduces the net charge and thus the electrical field at the edges of the active area. Consequently, this additional PN-junction affects the forward and reverse characteristic, as the minority carriers

injected by the guard ring need to be evacuated before the Schottky diode starts blocking. As a result, the observed reverse recovery charge Q_{rr} is potentially higher than what would be expected from the parasitic capacitance of the datasheet.

The termination concept of Trench Schottky diodes differs from the termination of Planar Schottky diodes. In case of Trench Schottky diodes there is no guard ring and thus no additional PN-junction. Instead of the guard ring a wide trench filled with a field-plate is used to relax the electrical field at the edge of the active cell. For a given die size the absence of the guard ring could result in a lower recovery time t_{rr} compared to Planar Schottky diodes, even though the parasitic capacitance of a Trench Schottky diode is inherently higher.

In recent years, a new generation of diodes has been developed at Nexperia based on Silicon Germanium technology. The SiGe diode technology bridges the gap between PN and Schottky diodes and shows a better trade-off between the leakage current and the forward voltage drop V_f . In contrast to the Planar Schottky diode there is a p^- SiGe layer in between the Schottky metal and the n^- epitaxy-layer. The SiGe layer leads to an increased diffusion gradient of electrons and therefore to a higher current density for a given forward voltage drop. Equally, if V_f is lower, there is less storage charge in the n^- Si-layer for a given current density compared to a standard PN diode. Like in the case of Planar Schottky diodes, the cell termination for SiGe diodes also relies on a guard ring. However, in total less charge

is involved for a given current density, leading to a potentially lower t_{rr} of the SiGe diode.

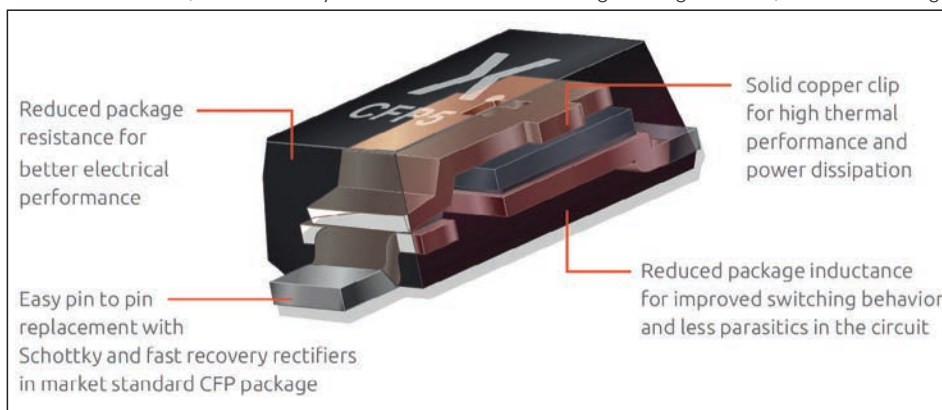
48 V/12 V converter application

The recent implementation of increased switching frequencies in power electronics due to wide bandgap switches is significantly affecting automotive 48 V/12 V converter designs. Thus a comprehensive performance comparison of a novel 120 V/3 A SiGe based diode with special regard to the suitability for such high frequency converters is performed.

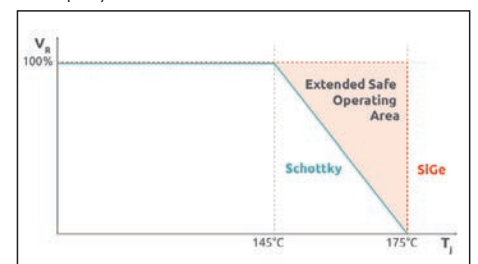
For this purpose, a low inductive double-pulse measurement circuit operating with very high transients with a 100V e-mode GaN-HEMT was designed. The considered main criteria are the conduction, switching and blocking characteristics. To further complement the analysis, robustness and EMI performance have been investigated. The design of the measuring PCB was thus optimized towards a minimal parasitic inductance within the commutation circuit. One method was to use inductance-minimized coaxial shunts by manually shortening the ground connected shield and by that omitting unnecessary conduction distance. Simultaneously, high accuracy measurement equipment with negligible influence on the circuit dynamics has been used. The total stray inductance L_α of the commutation circuit including the shunt results to about 5 nH.

Switching performance in comparison

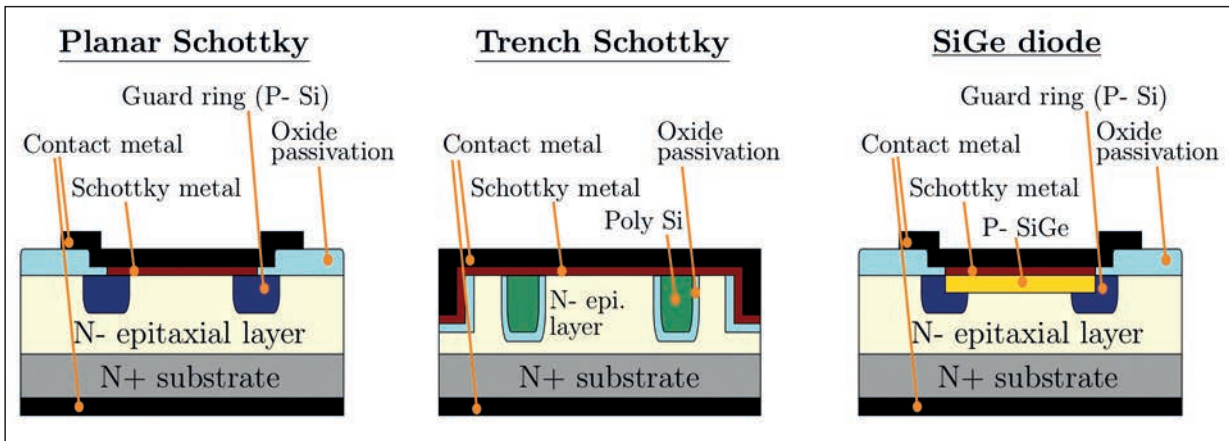
In order to compare the switching characteristics, the reverse recovery current for each diode was measured under different operating conditions such as varying switching speeds, turn-off currents, case temperatures and DC-link voltages. An exemplary set of measurements illustrates the



Advanced clip-bonded FlatPower (CFP) SiGe diode packaging



Extended safe operating area of SiGe diode



Cross sections: Planar Schottky diode (left), Trench Schottky diode (mid) and SiGe diode (right)

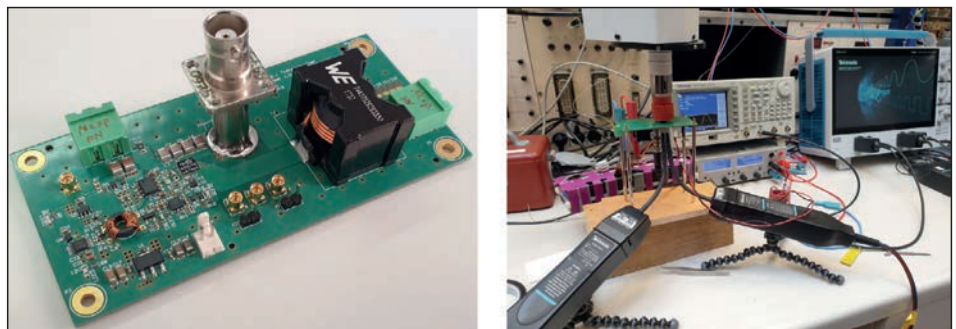
forward current i_F during the transition from forward bias into reverse direction for case temperatures $T_c = 25^\circ\text{C}$ and 85°C , a DC-link voltage of 48 V and a turn-off current of 3 A. The key factor is the very high current slope of $di_F/dt = 1 \text{ A/ns}$ which is 5-10 times higher compared to usual datasheet test conditions.

Two observations are standing out. First is the strongly oscillating current of the PN diode. The high snappiness of the current, which parasitically couples into the gate voltage V_{gs} , leads to a "rip off" in positive direction, reaching a positive peak current of around 26 A followed by a significant oscillation. Considering that all the diodes are tested under the same conditions and the fact that the PN technology itself is also inherent to the rather stable Nexperia PN diode, this oscillatory behavior could be led back to the diode model itself. This behavior decreases in amplitude with higher temperature and higher softness of the PN diode.

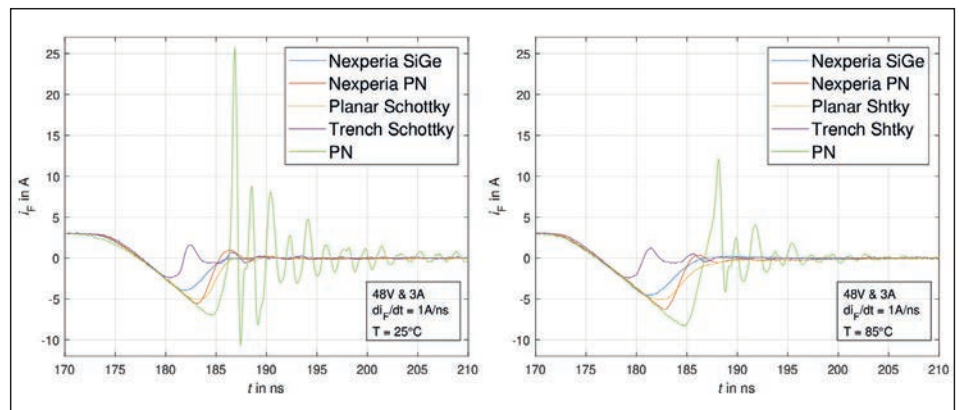
Second is the unexpected high reverse recovery charge Q_{rr} of the Planar Schottky diode, which is various times higher than the junction capacitance charge given in the datasheet. A possible explanation is the mentioned guard ring, which introduces a PN-junction typical reverse recovering behavior and therefore additional charge to the process, especially when the diode is operated with very high negative di_F/dt . These observations reveal that at high dynamics diode design induced processes start to significantly influence the performance up to a point where datasheet ratings become unreliable.

As for the Nexperia SiGe diode, the current i_F shows the softest behavior with almost no oscillation. Hence, a reduced impact on EMI is expected by using a SiGe diode. In terms of Q_{rr} and maximum reverse recovery current I_{rrm} at $T_c = 25$ and 85°C it outperforms all the diodes besides the Trench Schottky diode. However, the Trench Schottky diode shows a rather snappy behavior and a significant oscillation during the switching process. First comparisons considering different di_F/dt values show a consistency in the above mentioned ranking and relation of the diodes. Nevertheless, with a lower dynamic, the parameters tend back towards expected datasheet values.

The Table shows Q_{rr} and I_{rrm} which were derived from the measurements. The Trench Schottky diode shows the best Q_{rr} and I_{rrm} absolute values which is



Measurement PCB and the complete measurement setup



Forward current for a fast switching process at temperatures 25°C (left) and 85°C

clearly compliant with the absence of PN-junctions. The thermal influence is negligible for both parameters of the Trench Schottky diode as well as for the I_{rrm} of the Planar Schottky diode. Disregarding the PN Diode, the SiGe diode shows the highest dependence on operating temperature with a rise in Q_{rr} of 38 % and a rise in I_{rrm} of 15 % while still maintaining the second best absolute values

between all the diodes.

Literature

"Benchmarking of a Novel SiGe Diode Technology for the Usage in High Frequency 48V/12V Converter Applications", Nexperia, University of Hamburg/Germany PCIM 2020

www.nexperia.com

	$Q_{rr}^{T_c=25^\circ\text{C}}$ [nC]	$Q_{rr}^{T_c=85^\circ\text{C}}$ [nC]	$I_{rrm}^{T_c=25^\circ\text{C}}$ [A]	$I_{rrm}^{T_c=85^\circ\text{C}}$ [A]
Trench Schottky	6.53	6.83	2.4	2.42
Nexperia SiGe	18.05	24.9	3.96	4.56
Nexperia PN	23.41	30	5.58	6.29
Planar Schottky	25.75	32.9	5.03	5.06
PN	-	-	-	-

Q_{rr} and I_{rrm} derived from the measurements

200 V AEC-Q101 Approved SiGe Rectifiers

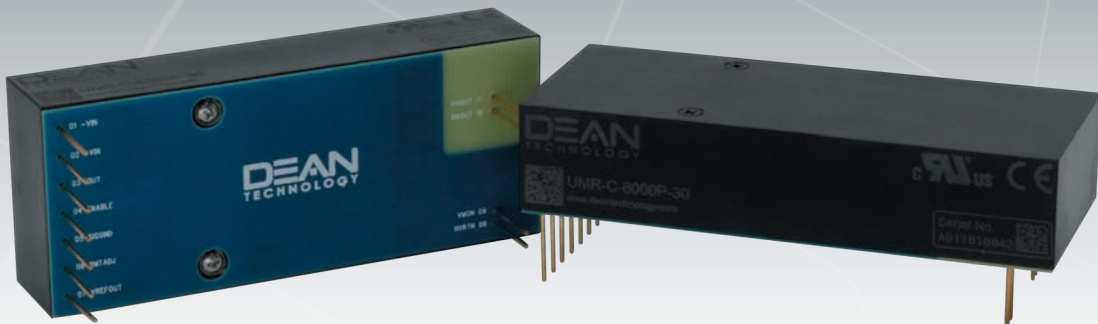
Nexperia has just announced a range of new SiGe rectifiers with 120 V, 150 V, and now 200 V reverse voltages that combine the high efficiency of Schottky devices with the thermal stability of fast recovery diodes.

Targeting automotive, communications infrastructure and server markets, the new 1 -3 A SiGe rectifiers are of particular benefit in high-temperature applications like LED lighting, engine control units or fuel injection. By boosting a low forward voltage and low reverse recovery charge, the SiGe rectifiers have an advantage of 10-20 % lower conduction losses. Simple pin-to-pin replacements of Schottky and fast recovery diodes are possible when switching to SiGe technology. The first four qualified 120 V SiGe rectifiers are already in mass production. A further eight 150 V and 200 V devices are sampling now.

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PCIM 2020 Goes Virtual

As a response to the spread of Covid-19, the PCIM Europe community will be meeting virtually. The "PCIM Europe digital days" will be held from 7 – 8 July 2020 on a virtual platform. Visitors can expect numerous presentations on-demand and virtual round tables. In live chats, they will have the opportunity to talk to exhibitors and speakers from industry and academia directly. In addition, a matchmaking tool will give you the opportunity to make contacts with attendees, exhibitors and speakers.

According to organizer Mesago, besides the sessions also the invited keynotes including verbal presentation and slides will be available.

Ahmed Elasser, GE Global Research Center (USA), will give a keynote on "Battery Energy Storage Systems: Past, Present and Future". In this talk, the speaker will draw on his extensive experience as a key member of the GE Global Research Center Renewable Reservoir team that worked for three years (2017-2019) to conceive, design, prototype, and productize the GE 4 MWh Li-Ion Battery Energy Storage System (BESS) dubbed the Renewable Reservoir. In addition to being a key member of the power electronics team that extensively tested the various power conversion components, the speaker worked closely with the co-located GE Energy Storage Team on the testing of the prototype 1 MWh energy storage boxes, and on the commissioning and energization of a 12 MVA test bed for testing the 4 MWh energy storage boxes. The speaker also worked with GE Solar to design, commission, and energize a solar PV array that is used to charge the batteries. In this talk the speaker will talk about the history of BESS systems from a research and industrial perspective, address the present situation of AC and DC coupled BESS. In particular DC coupled BESS that enables solar and storage integration will be discussed from a practical point of view. Topics like architecture type, dc/dc converters topologies, short circuit testing, integration with solar arrays using dc/dc optimizers, as well as overall safety, reliability, economical benefits, cost, and deployment will also be addressed. Other topics such as container requirements, battery technology, digital tools, unit controller, and

grid requirements will also be discussed. Finally, the speaker will address the challenges facing BESS and the various hurdles to its extensive deployment and adoption by utilities and commercial customers. The challenges at the battery, power conversion, and grid level will be highlighted.

Two other keynotes will cover - "Electric Cars" by Robert Plikat, who will introduce Audi's first electric drive train, and "The Future of Work".

The fourth keynote by Roland Hümpfner, Huawei Technologies (Germany) is entitled "Innovative Data Centers Power Infrastructure Solutions". Driven by Digitalization the demand for Data Centers will increase significantly in the next few years. The power demand of information and communication technology will grow substantially into the double digit percentage range. High availability Data Centers have a sophisticated power and cooling infrastructure substantially supported by power electronics. Looking into the historical evolution, considering the state of the art and have an outlook in to potential future solutions. Power Usage Effectiveness (PUE) is a traditional measure to evaluate energy efficiency, integration of renewable and providing grid services, sustainability and eco design will be in the future more and more interesting.

WBG for e-mobility

The accelerating adoption of electric vehicles, pushes SiC manufacturers to innovate and invent highly efficient and reliable MOSFET devices. With higher bandgap energy SiC enables higher and robust operating voltages as the



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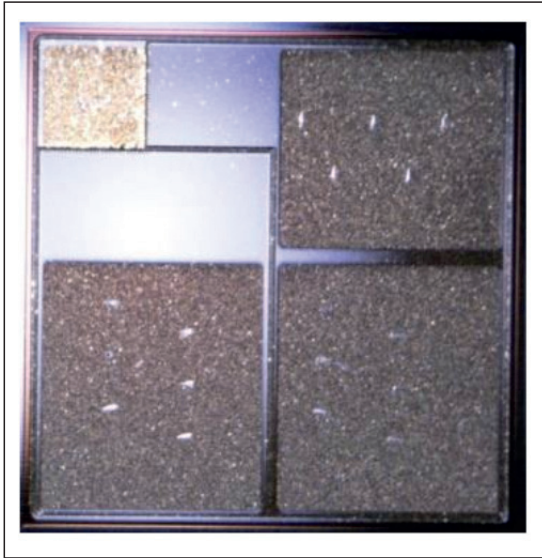
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electrical breakdown strength is 10 times higher than Silicon, enabling 7-10 times lower switching losses. Additionally, the higher field strength allows

SiC majority carrier MOSFETs to replace Silicon bipolar IGBTs, so the knee voltage is no longer present at light load, enabling lower conduction losses. This combination of lower conduction losses and lower switching losses can be used to extend the driving range of electric vehicles and/or reduce the size and weight of the vehicle.

The most common bus voltage in battery Electric Vehicles (EVs) is the so-called 400V bus which can typically range from 360V to 470 V, not including



Top-view image of Wolfspeed's 5 mm x 5 mm SiC die incorporating a conventional planar 750 V - 10.5 mΩ MOSFET

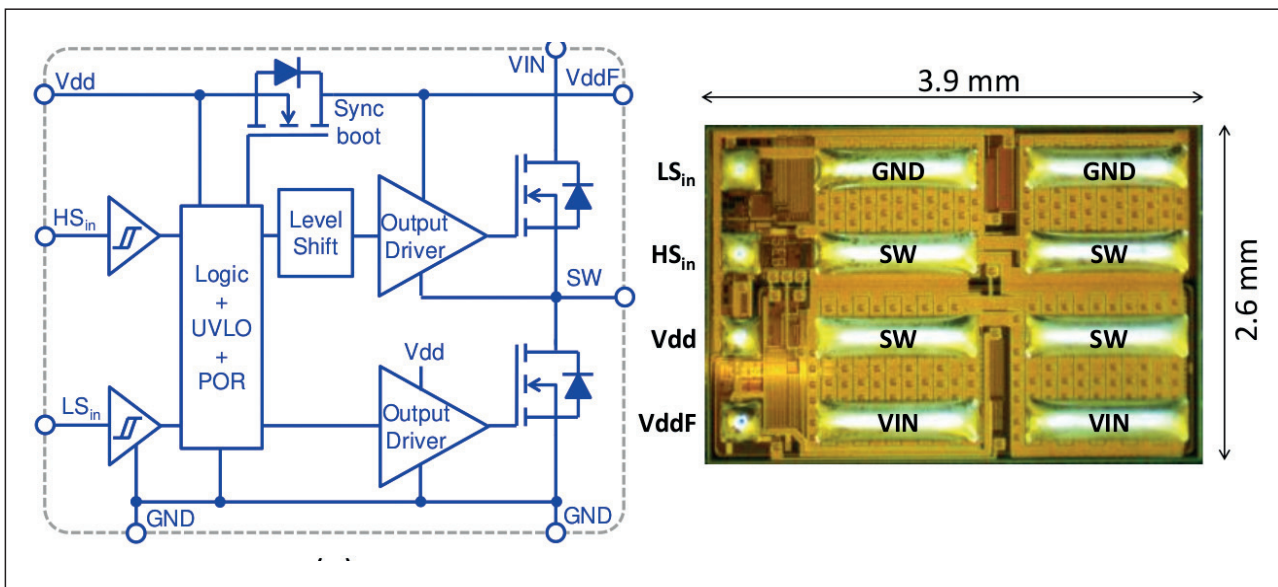
overshoot during switching events. Previously, 650V SiC and GaN have been reported for this application. Wolfspeed (www.wolfspeed.com) introduces a 750V SiC MOSFET with Ni:Pd:Au metal for sintering on top and bottom, eliminating top-side wirebonds which are commonly an early failure point in modules. "The 750 V rating has a mean measured breakdown voltage distribution > 960V, with good margin for overshoot and cosmic ray FIT rate requirements. The 750 V rated parts with the >960 V breakdown voltage are more rugged than typical 650V rated devices reported elsewhere," states presenter Jeffrey Casady. The compact 5 mm by 5 mm die incorporates a conventional planar 750V 10.5mΩ MOSFET. The gate pad is in the upper left corner, with equally sized source pads covering the rest of the chip. Thin Au is the top metal followed by thicker layers of Pd and Ni, suitable for top side sintering. The input capacitance was measured to be 6908 pF at V_{ds} of 750 V, V_{gs} of 0 V and 100 kHz. Output capacitance (C_{oss}) is 354 pF at 750 V and 35 pF (C_{oss}) at 750 V. At 75 A, E_{on} is measured to be 0.771 mJ and E_{off} is 0.552

mJ. The results can be scaled down to show the switching losses in 400 V automotive bus, which results in E_{on} of 0.656 mJ and E_{off} of 0.469 mJ. Additionally, the 750V SiC MOSFET demonstrates small changes in switching losses at high temperature which will be reported in the full paper.

SiC-based 1.2 kV power MOSFETs are promising candidates to replace Si IGBTs in numerous applications such as the main inverter for hybrid- (HEVs) and fully electric-vehicles (EVs). Here, reducing the specific $R_{DS(on)}$ is key along with ensuring reliable switching behavior of all devices involved, especially when parallel operation is required. While the technical advantages of SiC power MOSFETs, i.e. higher on-state current densities at high frequencies for a given power dissipation limit of the package, are well known, their widespread adoption is still slowed down by several barriers such as not fully proven reliability. In particular significant improvements are still needed regarding the MOS interface in order to improve the low inversion channel mobility and the poor threshold voltage (V_{th}) stability, especially for applications with parallel connection of many components. Both issues are closely connected to four types of interfacial charges namely oxide traps, interface traps, mobile ions and fixed charges. So-called near interface traps (NITs) are an important class of interface trap states, which can be found inside the oxide very close to the interface of SiC MOS structures and are responsible for the high concentration of neutral defect states near the conduction band edge ($E_c - E_t < 0.2$ eV).

In the paper "Threshold Voltage Stability Study on Power SiC MOSFETs Using High-k Dielectrics" ABB's (www.abb.com) Stephan Wirths, ABB Power Grids Switzerland, will present the first threshold voltage stability study on power SiC MOSFETs using high-k dielectrics. He investigate and compare the hysteresis of transfer characteristics of commercially available devices with SiC power MOSFETs using high-k dielectrics as function of sweep speed and $V_{GS,start}$. Moreover, the hysteresis effect during turn-on is discussed.

A low-voltage BLDC Motor Drive Inverter using a monolithic eGaN IC Power Stage will be introduced by EPC's (www.epc-co.com) Michael de Rooij. BLDC motors are popular choices and are finding increasing application in robotics and drones. Such applications have special requirements such as lightweight, small size, low torque ripple, and precision control. To address these needs, inverters powering the motors need to operate at higher frequency but require additional filtering to prevent excessive losses, EMI generation, and excess mechanical wear related to high frequency common mode and induced current flow. GaN FETs and IC's offer the ability to operate at much higher frequencies in hard-switching topologies without incurring significant losses. The block diagram of the monolithic GaN IC power stage includes input buffers, a logic interface with Power-On-Reset (POR) and Under-Voltage-Lockout (UVLO) functions. The main FETs are controlled by gate drivers within the IC that includes a high-voltage, high dv/dt capable control signal level-shifter and synchronous bootstrap that ensures proper high side voltage for the high side gate driver. The BLDC motor drive inverter uses the GaN IC power stage. Included are current shunts with amplifier for each phase



Block diagram of the and chip photo of EPC's monolithic GaN power stage

and supply and phase voltage measurement.

The monolithic GaN half-bridge ePower Stage IC is capable of 1 MHz switching and up to 15 ARMS load current per phase. This tiny IC greatly reduces PCB size. The system size, however, is further diminished because the very high frequency reduces filtering requirements, thus reducing size and weight. One application example is an eScooter with a 400 W BLDC motor that has been discussed in PEE2/20 "Integrated Power Stage for eMobility".

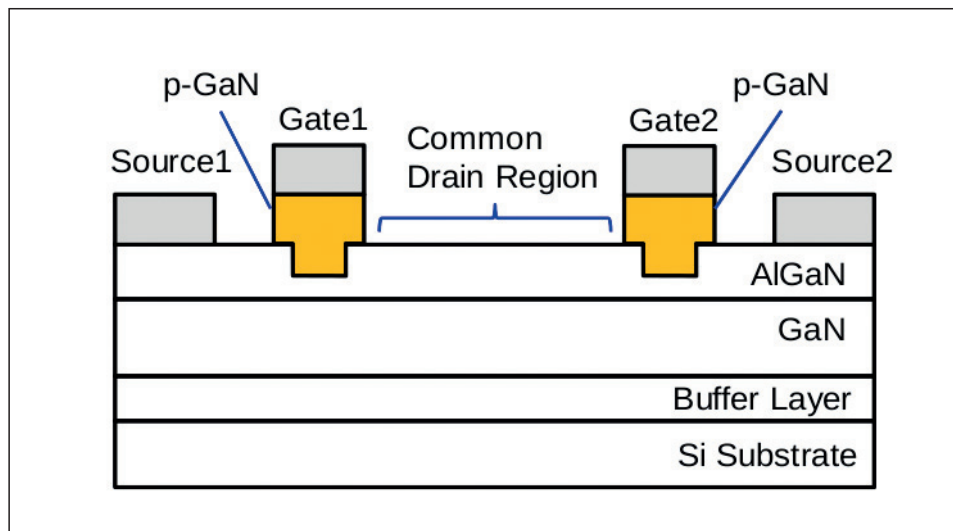
GaN bidirectional switch for circuit breaker

The DC power systems such as photovoltaic power system, electric transporter and DC power supply for data centers have been paid much attention due to their higher conversion efficiency. Circuit breakers used in such DC power systems are important components from the view point of safety. Although mechanical circuit breakers (MCBs) have been used in DC power systems, slow switching speed and short lifetime due to arcing damage have been significant drawbacks. DC circuit breakers using semiconductor devices have been investigated recently to overcome the limitation in conventional MCBs.

A GaN bidirectional switch with two gate terminals based on gate injection transistor (GIT) technology and conventional common-drain will be introduced by Panasonic (www.panasonic.com). For the conventional switch, two unidirectional transistors are connected in anti-series to realize bidirectional switch. This technique leads its on-state resistance (Ron) to be twice the value of one transistor. On the other hand, the GaN bidirectional switch enables to reduce both Ron and device size due to sharing channel region which has a role to maintain applied voltage. The parallel connection technique is effective method to reduce Ron of the semiconductor switch for further reduction of conduction loss in such applications. The Ron of 9.3 mΩ and the maximum current of 390 A are attained by 3-parallel connected GaN bidirectional switches. The fabricated SSCB interrupts the current of 306 A within 1.2 μs successfully by appropriate gate driving.

After the first publications by Uemoto et al. related to AlGaIn/GaN heterojunction field effect transistors (HFETs) with a p-type gate (gate injection Transistors, GIT), much effort has been spent to analyze the reliability of these devices. However, the major part of this publications is focused on reverse bias tests and investigations on the current-collapse. The topic of the paper

"Reliability of GaN GIT Devices in Power Cycling Tests with RDS(on) (T) and VGS (T) for Junction Temperature Calculation" by Chemnitz University of Technology is the reliability of GaN GITs under power cycling tests and the estimation of the junction temperature. The junction temperature has been measured with two temperature sensitive electrical parameters (TSEPs) simultaneously to calculate the junction temperature swing during the test. All tested devices reached their end of life condition by exceeding the initial forward voltage drop by more than 5 %. In the final paper a detailed failure analysis will be presented after removal of the mold compound.



The paper "Comprehensive Comparison of 99 % Efficient Totem-Pole PFC with Fixed (PWM) or Variable (TCM) Switching Frequency" by Maximilian Nitzsche from the University of Stuttgart presents a comprehensive comparison of a GaN-transistor based power factor correction (PFC) in a totem-pole configuration - modulated on the one hand with pulse width modulation (PWM) and on the other hand with triangular current mode (TCM). The basis for this comparison is a 180 W front end with an AC input voltage of 230 V, 50 Hz and a DC output voltage which is varied between 360 V and 400 V. The experimental results demonstrate an efficiency at nominal power of 99 % and greater.

SiC for traction

Demand of power semiconductors to be commonly used for power control and

In the paper "Experimental Evaluation and Analysis of Dynamic On-Resistance in Hard- and Soft-switching Operation of a GaN GIT" by the Technische Universität Berlin (), the dynamic on-resistance of a GIT is investigated. With the focus on the comparison between hard- and soft-switching, the impacts of various operation parameters are studied. Meanwhile, this work aims to separate the variation of on-resistance resulting from temperature, off-state and switching transitions. Extensive measurements are carried out in double-pulse, multi-pulse and continuous operating modes under hard- and soft-switching conditions, respectively. The results indicate that switching transitions aggravate the trapping effect especially in the high-frequency region, and soft-switching can significantly mitigate the degradation of on-resistance.

In a phase shifted converter applying low-voltage normally-off GaN transistors, the dynamic increase of the on state resistance shows a nearly constant value at low currents but increases unexpectedly at higher currents. The increase has a particular negative effect on the power losses of the transistors. The paper "Impact of the Dynamic On-State Resistance Increase in a Phase-Shifted GaN Low-Voltage Converter" by Tino Kahl from Technical University of Berlin investigates the effect of the increased on state resistance in continuous converter operation and discusses the influence of load steps.

Power engineers have proven that systems with GaN power transistors demonstrate high efficiency and power density due to GaN's superior switching performance. One characteristic that continues to draw attention from both academia and industry is dynamic RDS(on) performance of GaN devices. In the paper "The Effect of Dynamic On-State Resistance to System

Losses in GaN-based Hard-Switching Half-Bridge Applications" by Ruoyu Hou from GaN Systems (www.gansystems.com) the Boost converter continuous test is discussed in detail. A system-level loss breakdown is conducted to show the percentages of each loss for GaN power transistors, for both hard-switching and soft-switching devices in a half-bridge. The reliability test HTRB (high-temperature reverse bias) is a standard device reliability test. In this presentation, the dynamic RDS(on) result on the device post 1000 hours HTRB is put into the continuous running test setup. Compared to fresh devices the HTRB aged device presents even lower dynamic RDS(on) values.

The commercial Wide Bandgap based devices have the capability of fast switching and low on-state resistance. The paper will "High Frequency Investigation of Wide Bandgap-Based PFC and LLC Converters in PSU" by Jimmy Liu from GaN Systems provide a detailed comparison between GaN and SiC for a high frequency power applications, which consists of CCM Bridgeless Totem Pole Power Factor Correction AC-DC stage in conjunction with LLC resonant DC-DC stage. The power density and thermal performance with high switching frequency will be provided in this paper.

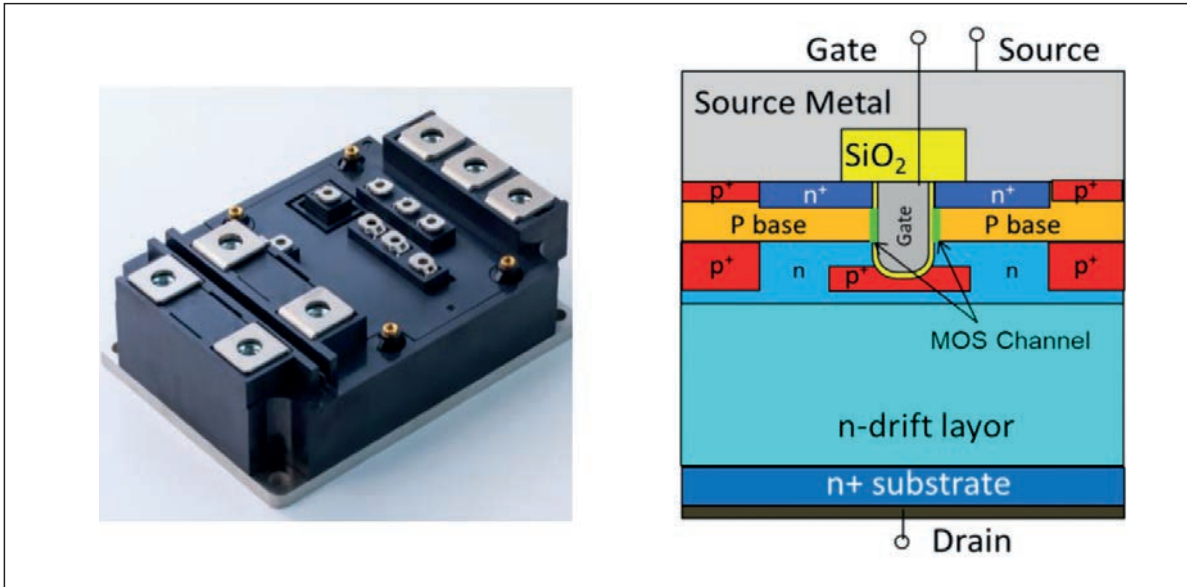
The paper "Comprehensive Comparison of 99 % Efficient Totem-Pole PFC with Fixed (PWM) or Variable (TCM) Switching Frequency" by Maximilian

Nitzsche from the University of Stuttgart presents a comprehensive comparison of a GaN-transistor based power factor correction (PFC) in a totem-pole configuration - modulated on the one hand with pulse width modulation (PWM) and on the other hand with triangular current mode (TCM). The basis for this comparison is a 180 W front end with an AC input voltage of 230 V, 50 Hz and a DC output voltage which is varied between 360 V and 400 V. The experimental results demonstrate an efficiency at nominal power of 99 % and greater.

SiC for traction

Demand of power semiconductors to be commonly used for power control and

LEFT: Cross section of Panasonic's bidirectional switch



Fuji's HpnC package and trench SiC MOSFET structure

conversion systems have rapidly increased in the recent years. Nowadays, SiC devices are expected as one of the most powerful alternative to Silicon devices and planar gate SiC MOSFETs have been already in mass production at Fuji electric until now. In order to realize further power density enhancement, applying trench gate structure must be needed for the purpose to decrease conduction losses.

Due to the fast switching speed of All SiC devices, a suitable low inductance package is generally required for the sake of suppress high surge voltage. Fuji provides the newly HpnC package, which is capable up to 3.3 kV, for traction applications. This package realizes 10 nH of internal

inductance. This is 76 % decrease compared to 42 nH for the conventional HPM traction module.

In addition, traction application needs higher reliability compared to industrial for Isolation, partial discharge, fire protection and power cycle. Therefore, HpnC is compliant to traction standard requirements EN50124-1, EN45545-2. And Delta Tc power cycle capability realize 40 % increasing compared to HPM. "We believe that All SiC modules will contribute greatly to weight reduction for traction power conversion systems by enhanced power density in the future," states Fuji's presenter Yusuke Sekino.

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SiC MOSFET Technology with Silicon-Like Reliability

The performance potential of SiC is indisputable. The key challenge to be mastered is to determine which design approach achieves the biggest success in applications. Advanced design activities are focusing on the field of specific on-resistance as the major benchmark parameter for a given technology. However, it is essential to find the right balance between the primary performance indicators like resistance and switching losses and the additional aspects relevant for actual power electronics designs, e.g. sufficient reliability. **Dr. Peter Friedrichs, Infineon Technologies, Neubiberg, Germany**

One of the most important acceptance criteria is the reliability of the device under the operating conditions of its target applications. The major difference to the established silicon device world is the fact that SiC components operate at much higher internal electric fields. Related mechanisms need to be analyzed carefully. What they have in common is that the total resistance of a device is defined by the series connection of contact resistances at drain and source, including the highly doped areas close to the contact, the channel resistance, the resistance of the JFET area, and the drift zone resistance (see Figure 1). In high-voltage Silicon MOSFETs, the drift zone clearly dominates the total resistance; in SiC devices, the part can be designed with a significantly higher conductivity.

Regarding the key MOSFET element, the SiC-SiO interface, the following differences

as compared to Silicon have to be considered:

- SiC has a higher surface density of atoms per unit area compared to Si, resulting in a higher density of dangling Si- and C- bonds; defects located in the gate oxide layer near the interface may appear in the energy gap, and act as traps for electrons.
- The thickness of thermally grown oxides strongly depends on the crystal plane. SiC devices operate at much higher drain-induced electric fields in the blocking mode compared to their Si counterparts (MV instead of kV), which requires measures to limit the electric field in the gate oxide to maintain reliability of the oxide in blocking stage. See also Figure 2 for TMOS, the critical point is the trench corner, and for DMOS, the center of a cell.
- SiC MOS structures show for a given

electric field a higher Fowler-Nordheim current injection compared to Si devices due to a smaller barrier height. Consequently, the electric field on the SiC side of the interface must be limited.

The above-mentioned interface defects result in a very low channel mobility. Therefore, they cause a high contribution of the channel to the total on-resistance. Thus, the advantage of SiC versus Silicon in the form of a very low drift zone resistance is diminished due to the high channel contribution.

Gate oxide field stress

An observed way to overcome this dilemma is to increase the electric field applied across the oxide in on-state, either higher gate source (V_g) bias for turn-on or comparably thin gate oxides. The applied electric fields exceed the values usually used in Silicon-based MOSFET devices (4

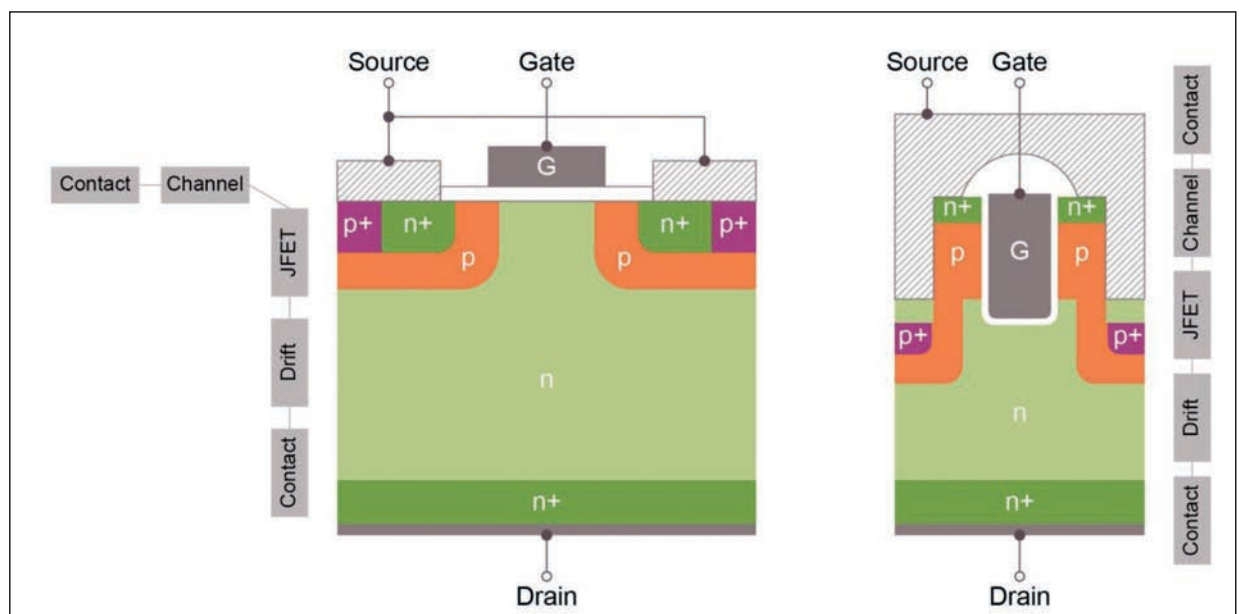


Figure 1: Planar DMOS SiC MOSFET (left), and vertical trench TMOS SiC MOSFET with the corresponding location of resistance-relevant contributions

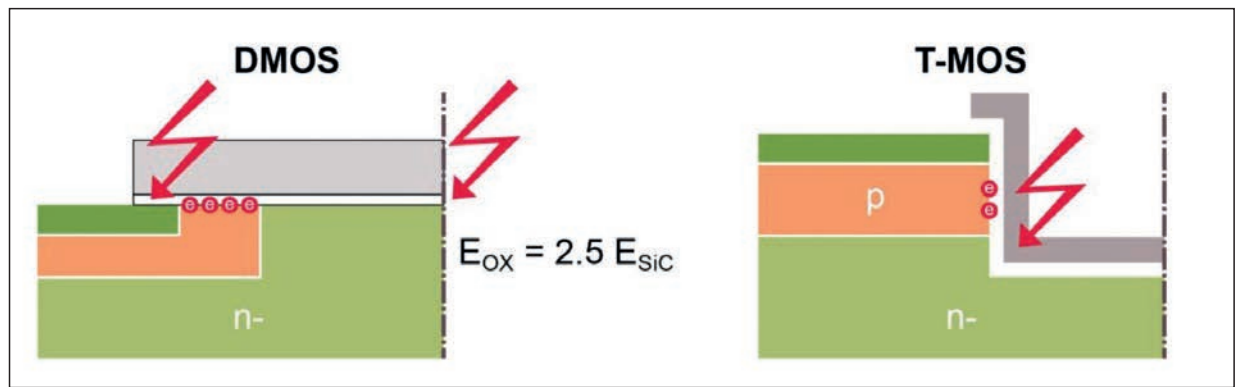


Figure 2: Typical structure of a planar MOSFET (half-cell) revealing two sensitive areas with respect to oxide field stress (left) and typical structure of a trench MOSFET (half-cell), critical issue is the oxide field stress at the trench's corners

to 5 MV/cm vs. 3 MV/cm max. in Silicon). Such high fields in the oxide in the on-state can potentially accelerate wear, and limit the capability of screening remaining extrinsic oxide defects.

Based on these considerations, it is clear that planar MOSFET devices in SiC actually have two sensitive areas with respect to oxide field stress, as sketched in the left part of Figure 2. First, the stress in reverse mode in the highest electric field area close to the interface between drift region and gate oxide, and secondly, the overlap between gate and source which is stressed in on-state.

A high electric field in on-state is seen as more dangerous, since no device design measures are in place which could reduce the field stress during on-state as long as the on-resistance performance has to be guaranteed. Infineon's overall goal is to combine the low $R_{DS(on)}$ offered by SiC with a working mode in which the part operates in the well-known safe oxide field-strength conditions. Hence, it was decided to focus on trench-based devices from the beginning. Moving away from the planar surface with its high-defect density towards other more favorable surface orientations enables a low channel resistance at low oxide fields. These boundary conditions are the baseline for transferring quality assurance methodologies established in the Silicon power semiconductor world in order to guarantee FIT rates expected in industrial and automotive applications.

The CoolSiC MOSFET cell design was developed to limit the electric field in the gate oxide in on-state as well as in off-state (see Figure 3). At the same time, an attractive specific on-resistance for the 1200 V class is provided, achievable even in mass production in a stable and reproducible way. The low on-resistance is ensured driving voltage levels of only $V_{GS} = 15$ V combined with a sufficiently high gate-source-threshold voltage of 4.5 V typically, being a benchmark in the

landscape of SiC transistors.

Special features of the design include the orientation of the channel at a single crystallographic orientation via a self-aligned process. This ensures highest channel mobility and narrow threshold voltage distributions. Another feature is the deep p-trenches intersecting the actual MOS trench in the center in order to allow narrow p+ to p+ pitch sizes for effective screening of the lower oxide corner.

Dynamic performance

Being a unipolar device, the dynamic performance of the SiC-MOSFET is largely governed by its capacitances. The device was designed to have a small gate-drain reverse capacity C_{gs} compared to the input

capacity C_{gs} . This is beneficial for suppressing parasitic turn-on, which can prevent the use of sophisticated gate driver circuitry when operated in a half-bridge configuration. Many CoolSiC

MOSFET products can be turned off safely even with 0 V at the gate, since in addition to the favorable capacitance ratio the threshold voltage is sufficiently high. The total device capacitances as a function of temperature are summarized in Figure 4 (left).

Figure 4 (right) displays the typical switching losses of a half bridge with single devices mounted in a 4-pin TO-247 housing as a function of drain current. The turn-off energy E_{off} depends only slightly on the load current, since it is dominated by capacitances, whereas the turn-on energy E_{on} increases linearly with current, and dominates the total losses E_{tot} . Based on the status from mid-2019, it should be emphasized that the CoolSiC MOSFET shows the lowest E_{on} among the commercially available 1200 V SiC MOSFETs. E_{on} and E_{off} are practically independent of temperature.

Important to note is the actual housing design that has a significant impact on switching losses, mainly on turn-on losses. Especially effective is the use of Kelvin contacts, which practically separate the load path from the control path in terms of current, and thus, help to prevent di/dt induced feedback loops to the gate signal increasing the dynamic losses.

In general, it is essential to implement fast-switching SiC transistors with low capacitances and gate charges in certain packages only. Major criteria include good thermal performance due to the high-loss power density (absolute losses are reduced with SiC of course, but the remaining ones are concentrated in very small areas). Another criterion is a low stray inductance for managing high di/dt slopes without critical voltage peaks. Finally, especially in the case of multichip packages with more die in parallel, a

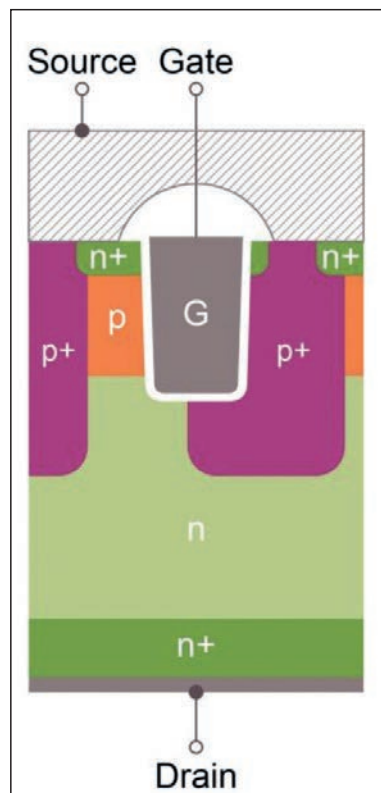


Figure 3: Sketch of the CoolSiC MOSFET cell structure

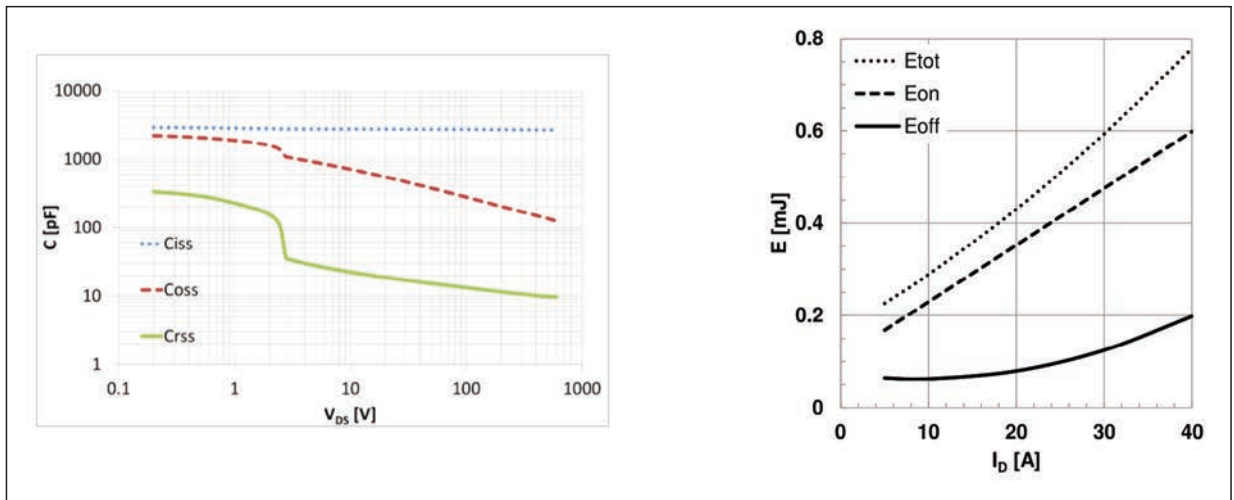


Figure 4: Typical device capacitance vs. drain-source voltage for a 45 mΩ CoolSiC (left) and related switching energies (right) as a function of drain current (for $V_{GS} = 15/-5$ V, $R_{Gext} = 4.5$ Ω, $V_{DS} = 800$ V, $T_{vj} = 175^\circ\text{C}$)

symmetric inner module design based on the strip line concept is mandatory. Current module packages offering such features are the EASY platform for modules, or the TO247 family, respectively TO263-7, for discrete housing.

Gate-oxide reliability

Besides performance, reliability and ruggedness are the most discussed topics for SiC MOSFETs.

Ruggedness is defined as the capability of a device to withstand certain extraordinary stress events, for example, short-circuit performance or pulse-current handling capability. Reliability covers the stability of the device under nominal operating conditions over the targeted application lifetime.

The effects relevant to reliability include the drift of certain electrical parameters or catastrophic failures. For hard failures, the quantification is usually done in the form of FIT rates, which actually state how many devices of a certain type are allowed to fail over a certain period. FIT rates in high-power silicon devices are mostly governed today by cosmic ray effects.

In the case of SiC, an additional influence from gate-oxide reliability needs to be considered due to the oxide field stress. Thus, the total FIT rate is the sum of cosmic ray FIT rates and oxide FIT rates. For cosmic ray stability, a similar approach can be applied such as the one typical in the Silicon sector. Here, FIT rates are obtained experimentally for a certain type of technology, and based on the results, in combination with the application targets, a design can be implemented that meets the FIT rates, usually achieved by optimizing the electric field distribution in the drift zone. For the oxides FIT rates, a screening process needs to be applied to reduce the FIT rates, as defect densities in

SiC are still quite high compared to Silicon (in the case of Infineon's Si power devices, the screening of gate oxides still takes place as a quality assurance measure).

The challenge of the gate-oxide reliability of SiC MOS devices is for example to guarantee a maximum failure rate of less than 1 FIT under given operation conditions in industrial applications (as is available today for IGBTs). Since the intrinsic quality and properties of SiO₂ on SiC and on Si are almost identical, Si MOSFETs and SiC MOSFETs of the same area and oxide thickness can withstand roughly the same oxide field for the same time (same intrinsic lifetime). Of course, this is only valid if the devices do not contain defect-related impurities, i.e., extrinsic defects. In contrast to Si MOSFETs, SiC MOSFETs exhibit a much higher extrinsic defect density in the gate oxide.

Infineon has invested a significant amount of time and material samples to develop a complete picture regarding the MOS reliability for SiC MOSFETs. We have tested the on-state reliability of electrically screened SiC MOSFETs for 100 days at 150°C using three individual stress runs at different positive and negative gate-stress biases. Each sample group consisted of 1000 pieces.

Using the initial processing conditions, at twice the recommended gate bias of 30 V, less than 10 out of 1000 devices failed. The implemented technology progress reduced this number to only one fail at 30 V, and zero fails at 25 V and -15 V. This one remaining failure is still an extrinsic failure, but it is not critical, as it will occur far beyond the specified product lifetime under the nominal gate-bias use conditions.

To verify the off-state reliability of the CoolSiC MOSFETs, we have stress-tested

over 5000 1200 V devices for 100 days at 150°C, $V_{GS} = -5$ V and $V_{DS} = 1000$ V. These conditions correspond to the most critical point of the mission profile for industrial applications. A further acceleration is very difficult due to restrictions in the applied drain voltage with respect to the breakdown voltage of the device. Running the tests at even higher drain voltages will falsify the results, as other failure mechanisms such as cosmic-ray induced failures would become more likely. The result was that none of the tested devices failed during this off-state reliability test. As the 650 V device follows the same design criteria as the 1200 V device, the same reliability is expected.

Conclusion

The CoolSiC MOSFET features superior performance in terms of switching behavior and total losses. One of the highlights is the possibility to turn off the device with zero gate bias, which makes the transistor concept the only true "normally-off" device at the moment. We are in an advanced stage of rolling out the 2nd CoolSiC generation which will increase the power handling capability by 25 – 30 % and enhance the safe operating area (SOA) without compromising quality.

Literature

Infineon Technologies White Paper "High-performance CoolSiC MOSFET technology with silicon-like reliability", January 2020

www.power-mag.com

SiC Wafer Cost Reduction

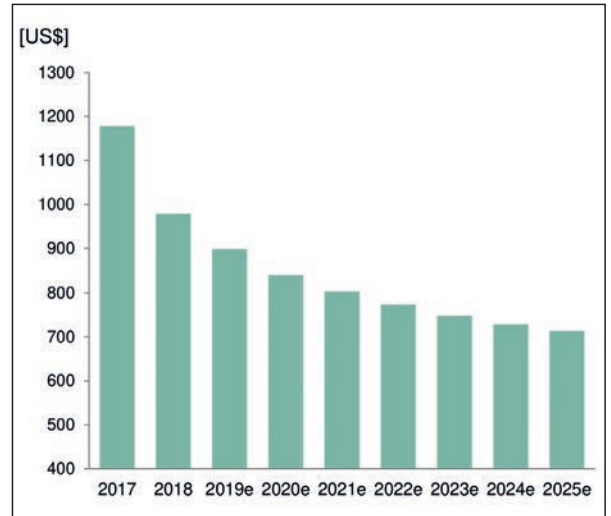
According to a SiC update in May 2020 by Peter Friedrichs SiC raw wafers remain the major cost driver, though the price curve is declining. A special technology saves a lot of the valuable material during processing.

In November 2018 Infineon acquired Siltrix for 124 million Euros, a start-up based company in Dresden. They have developed an innovative technology (Cold Split) to process crystal material efficiently and with minimal loss of material. Infineon will use the Cold Split technology to split SiC wafers, thus doubling the number of chips out of one wafer.

Focus of Cold Split is to split crystalline materials with minimal loss of material compared to common sawing technologies. This technology can also be applied with SiC, for which rapidly rising demand is expected in the coming years. SiC products are already used today in very efficient and compact solar inverters. In the future, SiC will play a more and more important role in electro-mobility. The Cold Split technology will be industrialized at the existing Siltrix site in Dresden and at the Infineon site in Villach, Austria.

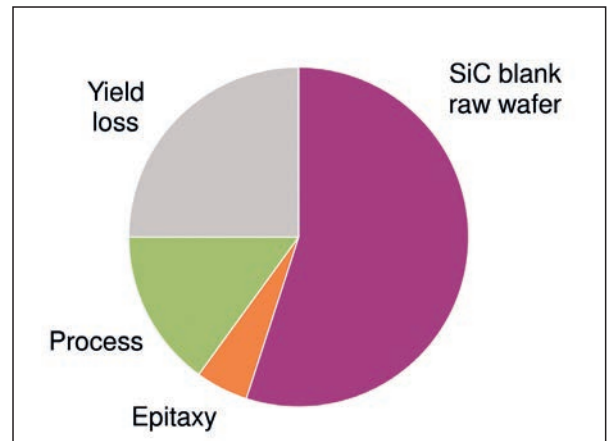
Siltrix's proprietary process is a high-output, low-cost wafering and thinning technology for substrates like SiC and GaAs, as well as GaN, Sapphire and Silicon. The laser-based technique employs a chemical-physical process that uses thermal stress to generate a force that splits the material with exquisite precision along the desired plane, and produces virtually no kerf loss. The "no kerf loss" capability delivers breakthrough advantages. First, it extracts more wafers per boule than conventional wafering technologies. This drives up output. Second, it dramatically reduces consumables costs.

According to Friedrichs design and production of semi-automated process tool park is completed in Dresden, and the clean room is ready for manufacturing by end of calendar year 2020. Wafers for splitting are already available to increase the number of usable wafers by a factor of 2. Boule splitting is planned for 2023 increasing wafers by a factor of 2.0 in a first step, with potential for a factor of 2.6. "Combining boule splitting and wafer splitting will make the most efficient process," Friedrichs pointed out. And the manufacturing lines in Villach are already capable of processing 200 mm diameter SiC wafers!



SiC 150 mm raw wafer price development

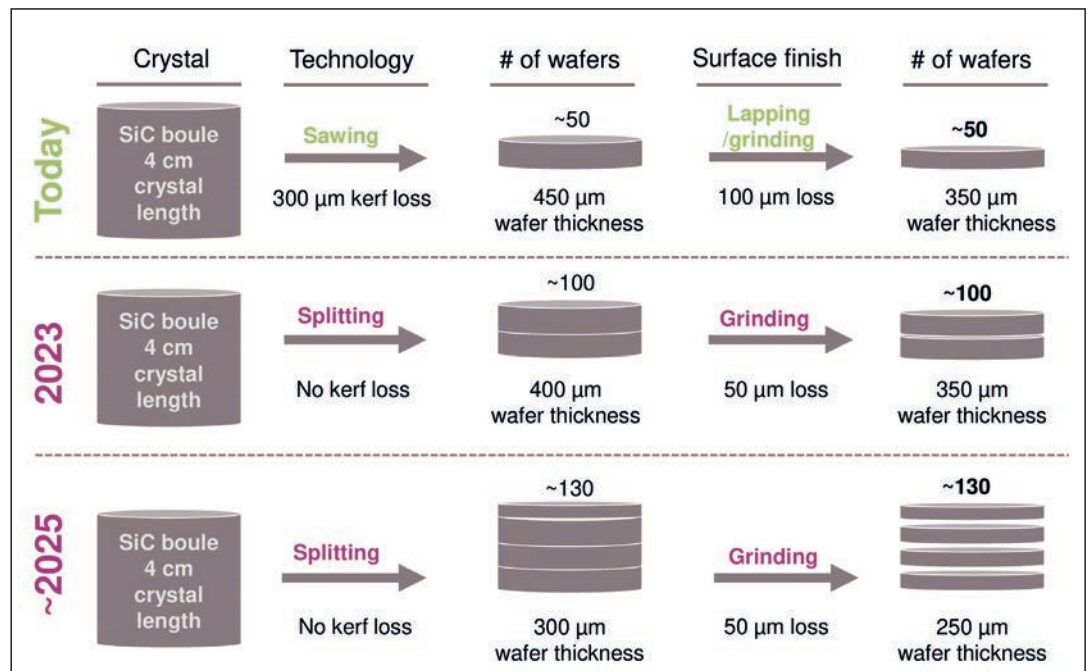
Source: Omdia/Infineon



Average SiC MOSFET frontend cost breakdown

Source: Yole/Infineon

RIGHT: From wafer splitting to boule splitting with Cold Split



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Modular Evaluation Platform for Discrete CoolSiC MOSFETs

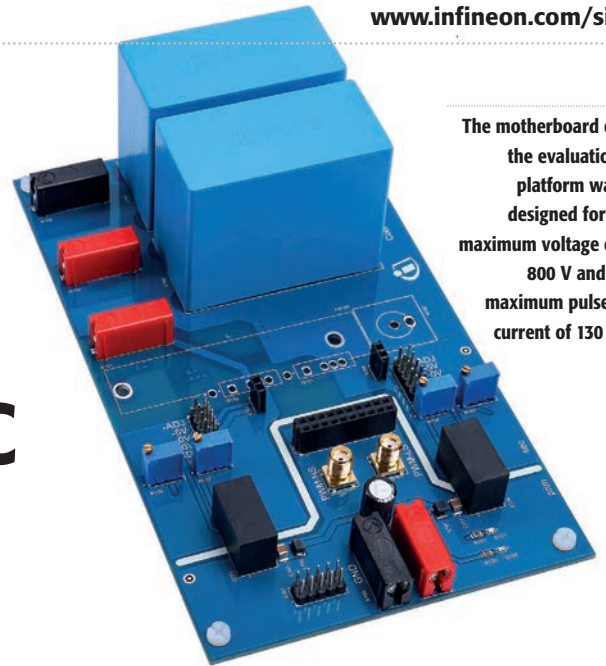
Double pulse testing is a standard procedure for designers to learn about the switching behavior of power devices. To facilitate the testing of drive options for the 1200 V CoolSiC MOSFET in TO247 3-pin and 4-pin packages, Infineon introduced a modular evaluation platform.

The modular SiC evaluation platform comprises a motherboard with interchangeable drive cards. The drive options include a Miller clamp and a bipolar supply card; additional variants will be launched in the near future. In shortening time-to market for a variety of applications, this portfolio will help paving the way for Silicon Carbide to become mainstream.

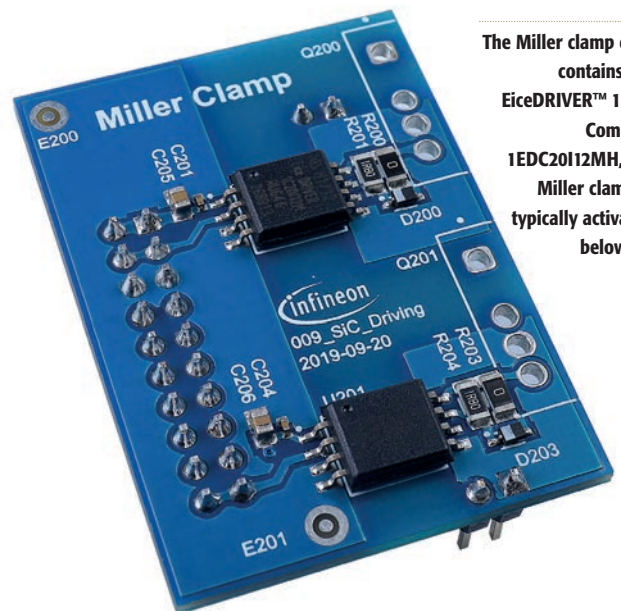
The motherboard of the evaluation platform is split into two sections, the primary supply side and the secondary side. On the primary side, the 12 V supply and the PWM will be connected. On the secondary side is the secondary supply of the driver, the half bridge with connections for the shunt for current measurement and the external inductance. The positive operating voltage of the drivers can be adjusted between +7.5 and +20 V, while the negative voltage can be regulated between +1 V and -4.5 V. The motherboard was designed for a maximum voltage of 800 V and a maximum pulsed current of 130 A. For measuring at higher temperatures of up to 175°C, the heatsink can be used together with a heating element.

Serving as a reference design for two drive options, the cards feature driver ICs from the EiceDRIVER™ family suitable for high frequency switching of SiC power devices. The first modular card contains the 1EDC Compact 1EDC20I12MH with an integrated active Miller clamp, which is typically activated below 2 V. The second drive card includes the 1EDC Compact 1EDC60H12AH allowing a bipolar supply, where VCC2 is +15 V and GND2 is negative. With these two driver cards, the portfolio already covers a large part of the options preferred by designers for driving SiC MOSFETs.

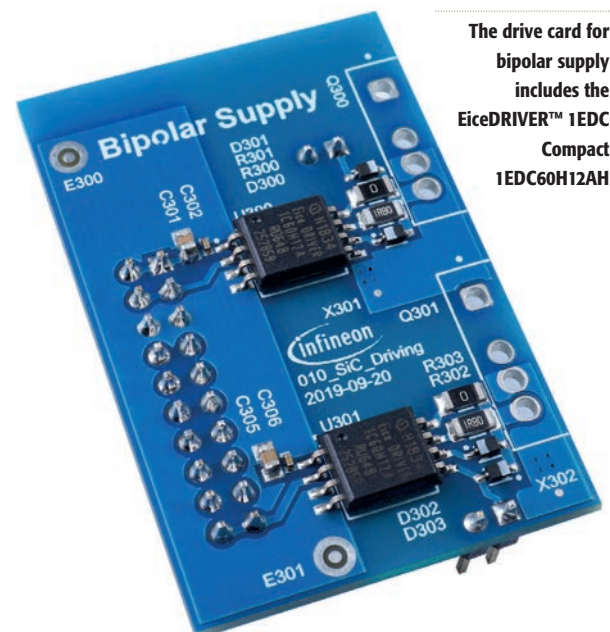
All three components of the modular evaluation platform – motherboard, Miller clamp and bipolar drive cards – can be ordered now. An additional drive card for short circuit detection will be added to the portfolio during summer 2020, a card for SMD package testing will follow during the second half of this year. www.infineon.com/tools



The motherboard of the evaluation platform was designed for a maximum voltage of 800 V and a maximum pulsed current of 130 A



The Miller clamp card contains the EiceDRIVER™ 1EDC Compact 1EDC20I12MH, the Miller clamp is typically activated below 2V



The drive card for bipolar supply includes the EiceDRIVER™ 1EDC Compact 1EDC60H12AH

Factorized Power Accelerates Coral Reef Restoration

According to the latest figures over 70% of the world's coastlines are eroding, with 200 million people worldwide reliant on the protection that coral reefs offer. With 99% of remaining reefs projected to disappear by 2040, communities and livelihoods are at risk in areas such as Mexico, Indonesia and numerous smaller island habitats around the world. CCell uses renewable energy sources such as solar, wind and wave energy to power their reef growing systems. To drive a precisely calculated current through the seawater, Vicor recommended its FPA for efficiently converting wide-range, renewable energy into precision power delivery for the point of load.

Henryk Dabrowski, Vicor VP Sales EMEA

The mission of CCell Renewables

(www.ccell.co.uk) is to combat coastal erosion and enhance marine ecosystems by restoring damaged coral reefs and growing new ones on a large scale. The technique, invented by Dr. Wolf Hilbertz and based on the electrolysis of seawater, is revolutionary. In just five years it can produce incredibly strong limestone rock that would normally take hundreds of years to form. Where Herbitz grew small restorative reefs, CCell is building much larger structures which are expected to have a far-reaching positive impact on the coastal ecosystem.

Research shows that total wave energy is growing by 0.4 % per year due to rapid warming of our oceans. If reefs could be restored or created and could reduce the energy of waves by 5 – 8 %, it would be possible to revert the impact of waves hitting the shore to levels from nearly 20 years ago. As a result, coastline erosion would be stopped or even reversed.

To achieve this, the limestone structure on which coral grows must be created on a large scale without impurities, with a strong molecular structure and grown at an optimum rate. The electrolysis process must be precise. It cannot be too fast or too slow: too slow and nothing will grow, too fast and the limestone will not be tenable.

Precision and power challenges

The challenges are numerous in growing sustainable reefs on a large scale in remote locations and several hundreds of meters offshore. CCell use renewable energy sources such as solar, wind and wave energy to power the reef-growing systems. Selecting the best approach usually depends on the reef's distance from the shoreline. To effectively combat

erosion, ocean waves need to be dissipated around 300 m from the shore.

To grow 360 m² of coral reef requires approximately 2 kW of power. While on paper wave energy devices can be expensive when compared to solar panels, the farther offshore the devices are located, the more efficient wave energy converters become. In several projects the converters will be alongside reefs that are over 700 m from the shore. As well as using its system to patch up existing reefs, the company is planning a 300 m long reef with residents that will be only 70 m from the shore. This will be powered partly by solar and partly by the wind.

All of these renewable power sources

have one thing in common: their power generation creates a widely varying output voltage due to constantly changing environmental conditions.

The primary power source

The CCell primary power generator is based around an innovative wave-energy converter that uses a sturdy paddle to drive a hydraulic system for producing electricity. This power source delivers a wide-range and varying voltage created by the wave energy that must then be regulated precisely to grow tenable coral. As well as having to manage a highly variable source voltage, the electrolysis process is governed by the seawater

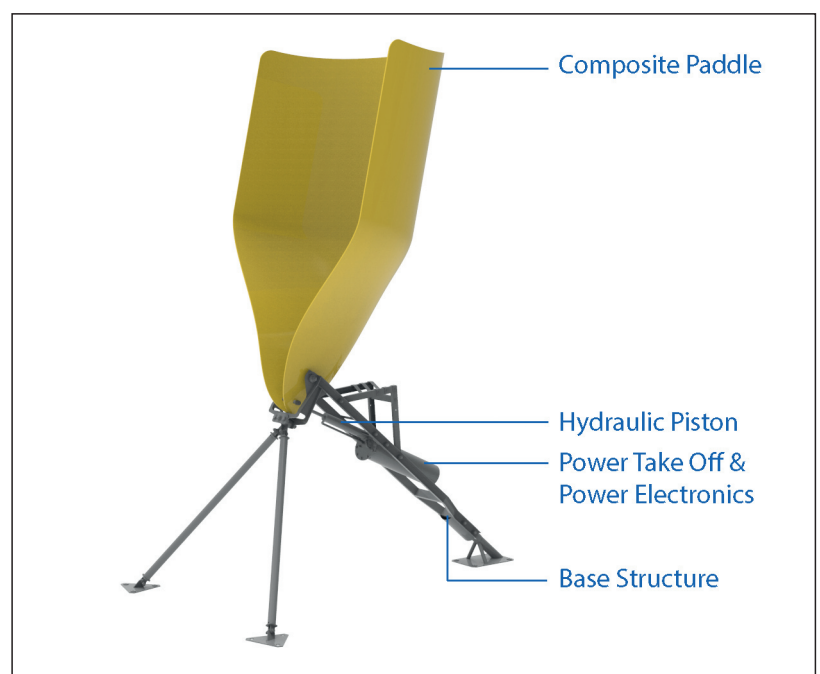
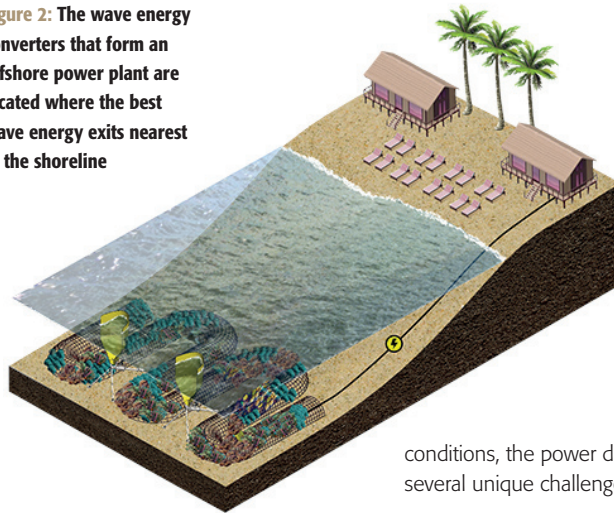


Figure 1: Primary power generator is based around an innovative wave-energy converter that uses a sturdy paddle to drive a hydraulic system for producing electricity

Figure 2: The wave energy converters that form an offshore power plant are located where the best wave energy exits nearest to the shoreline



composition, water temperature and flow rate over the electrodes (anode and cathode) formed by the steel frame. All of these variables have to be closely monitored, measured and controlled to ensure that the potential difference between the anodes and cathodes drives a precisely calculated current through the seawater between the electrodes. This is necessary to achieve the optimum electrolysis process to grow strong, sustainable limestone (calcium carbonate) deposits from minerals found in the sea water.

Growth is managed precisely by controlling this potential difference (electric field) between the electrodes within a 'goldilocks zone,' which for the Ccell system is between 1.2 and 4 V, depending on all the environmental conditions mentioned previously.

The power delivery network

To grow 360 m² of coral reef requires approximately 2 kW of power. The wave energy converters that form an offshore power plant are located where the best wave energy exits nearest to the shoreline. The output voltage of the wave converters can vary between 35 and 70 V.

The power delivery network (PDN) consists of a front-end conversion and regulation stage followed by a downstream point-of-load (PoL) regulation stage for the systems monitoring and control electronics. Power is delivered via a long cable to the electrolysis system which is placed very close to the steel frame located on the ocean floor where the reef will be rebuilt or created.

With a power level of 2 kW and a goldilocks zone of 1.2 – 4 V for the potential difference between electrodes, the electrolysis power system must be capable of delivering up to 1,666 A at the lower end of the voltage range. With these

conditions, the power delivery network has several unique challenges:

- Conversion and regulation of a wide 36 – 70V input voltage for the control system onshore and the electrolysis system out on the reef;
- delivering high power (2kW) to the offshore electrolysis system up to 700m offshore;
- delivering high current (up to approx. 1700 amps) and maintaining voltage regulation at a controlled level. The voltage range is 1.2 – 4V between the steel cage electrodes, and system needs to be able to change voltage and current delivery rapidly under ever-changing conditions.

Vicor recommended its proven Factorized Power Architecture (FPA), confident that it would meet all of the power delivery needs and also achieve high current density to minimize the power system size deployed in the ocean. The FPA incorporates a current multiplier which also has a fast transient response.

The FPA solution

Advanced processors are now requiring higher currents as their load voltages drop below 1 V.

Density and low noise at the point of load are becoming even more critical to

processor performance. The continuing challenge for system designers is to accommodate lower voltages with faster transient response and better power system efficiency in an ever-shrinking board area.

Factorized Power Architecture solves these problems – it takes the DC/DC converter functions of regulation and conversion and factorizes it into its two constituent parts. This allows for complete optimization of each function, a high efficiency regulator coupled with a high density current delivery device for various low voltage high current loads. FPA consists of a Pre-Regulator Module (PRM) and a Voltage Transformation Module (VTM)/Current Multiplier. These two devices work in partnership with one another, each fulfilling its specialized role efficiently to add up to the complete DC/DC conversion function.

The PRM supplies a regulated output voltage, or 'factorized bus' from an unregulated input source.

This bus feeds one or more VTMs which transform the factorized bus voltage to the level needed by their load, while providing isolation as well. So, a PRM VTM chip set provides the full, regulated, isolated DC/DC converter function. Factorized Power means more space at the point(s) of load, one-half the power dissipation and the regulation function can be remotely located.

Thus the Factorized Power Architecture does what it says, which is to factorize the DC/DC function into two separate modules, a PRM regulator and a VTM current multiplier.

The PRM uses a patented Zero-Voltage Switching (ZVS) buck-boost regulator control architecture to give high-efficiency step-up and step-down voltage regulation and soft start; maximum efficiency is achieved when $V_{in} = V_{out}$, with 99.3 % peak being achieved with the latest PRMs (Figure 3).

The VTM current multiplier (Figure 4) is

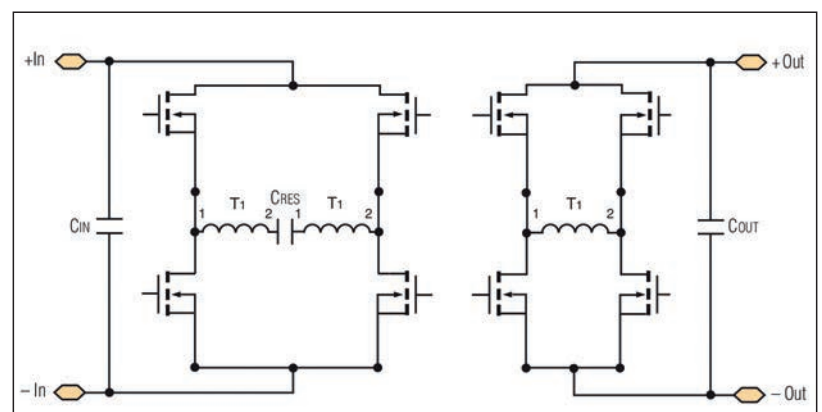


Figure 3: Simplified schematic of the Pre-Regulator Module

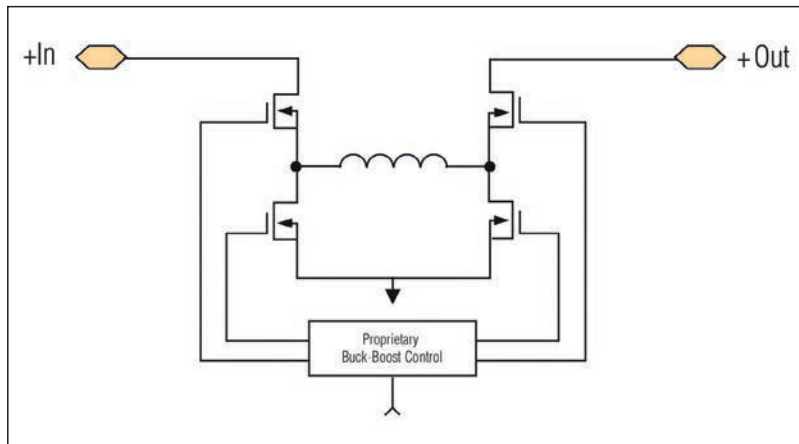


Figure 4: Simplified schematic of the Sine Amplitude Converter

a high-efficiency voltage transformation module using a proprietary Zero-Current Switching / Zero-Voltage Switching (ZCS / ZVS) Sine Amplitude

Converter (SACTM). It operates on a pure sinusoidal waveform with high spectral purity and common-mode symmetry. These characteristics mean that it does not generate the harmonic content

that the typical PWM type conversion has and generates virtually minimal noise. The control architecture locks the operating frequency to the powertrain resonant frequency, allowing up to 97 % efficiency and minimizing output impedance by effectively cancelling reactive components. This very low, non-inductive output impedance allows it to respond almost

instantaneously to step changes in the load current.

The VTM responds to load changes regardless of magnitude in less than one microsecond with an effective switching frequency of 3.5 MHz. The VTM's high bandwidth obsoletes the need for large point-of-load capacitance. Even without any external output capacitors, the output of a VTM exhibits a limited voltage perturbation in response to a sudden power surge. A minimal amount of external bypass capacitance (in the form of low ESR/ESL ceramic capacitors) is sufficient to eliminate any transient voltage overshoot.

The architecture and topologies of each device are perfect for solving the CCell power delivery challenges.

First, the PRM buck-boost regulator is capable of operating over a wide input voltage range. Due to its ZVS topology, it has very high efficiency and power density and is easily paralleled to deliver higher power. The power delivery to the reef is so far offshore it requires almost 2 kW, but the higher voltage allows reduced cable size and a cost saving. The PRM not only operates over a wide input voltage range but is optimized for delivering higher regulated voltages for the downstream VTM.

The VTM's transformation ratio is called the K factor. The VTM operates like a DC/DC transformer such that if the K factor was 1:8, the output would be 1/8th of the input and the current multiplication from input to output would be 8. The two modules work seamlessly together with the PRM handling the tightly regulated voltage required for the reef, and the VTM handling the conversion and current delivery to the electrodes. For the CCell application the following power delivery decisions were made.

Taking into account the measured voltage drops in the power cables to the reef, the PRM (Figure 5) would regulate the 36 – 70 V input from the wave energy converter to deliver between 9.6 and 32 V on the input of the VTM modules, which have K factors of 1:8, to provide a 1.2 – 4 V output. As environmental conditions are constantly changing, the PRM is regulating the input to the VTM to maintain the desired output voltage.

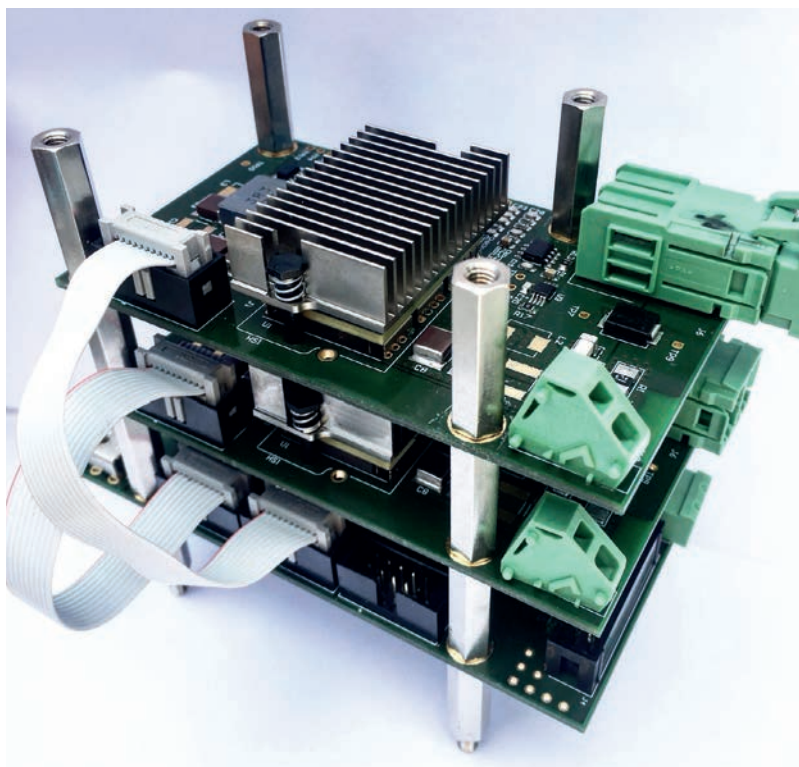


Figure 5: The PRM regulates the 36 – 70 V input from the wave energy converter to deliver between 9.6 and 32 V input of the VTM modules

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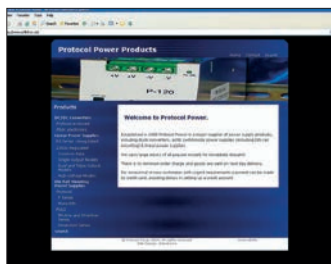
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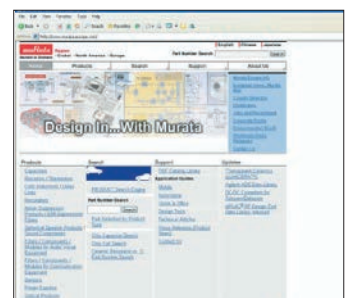
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