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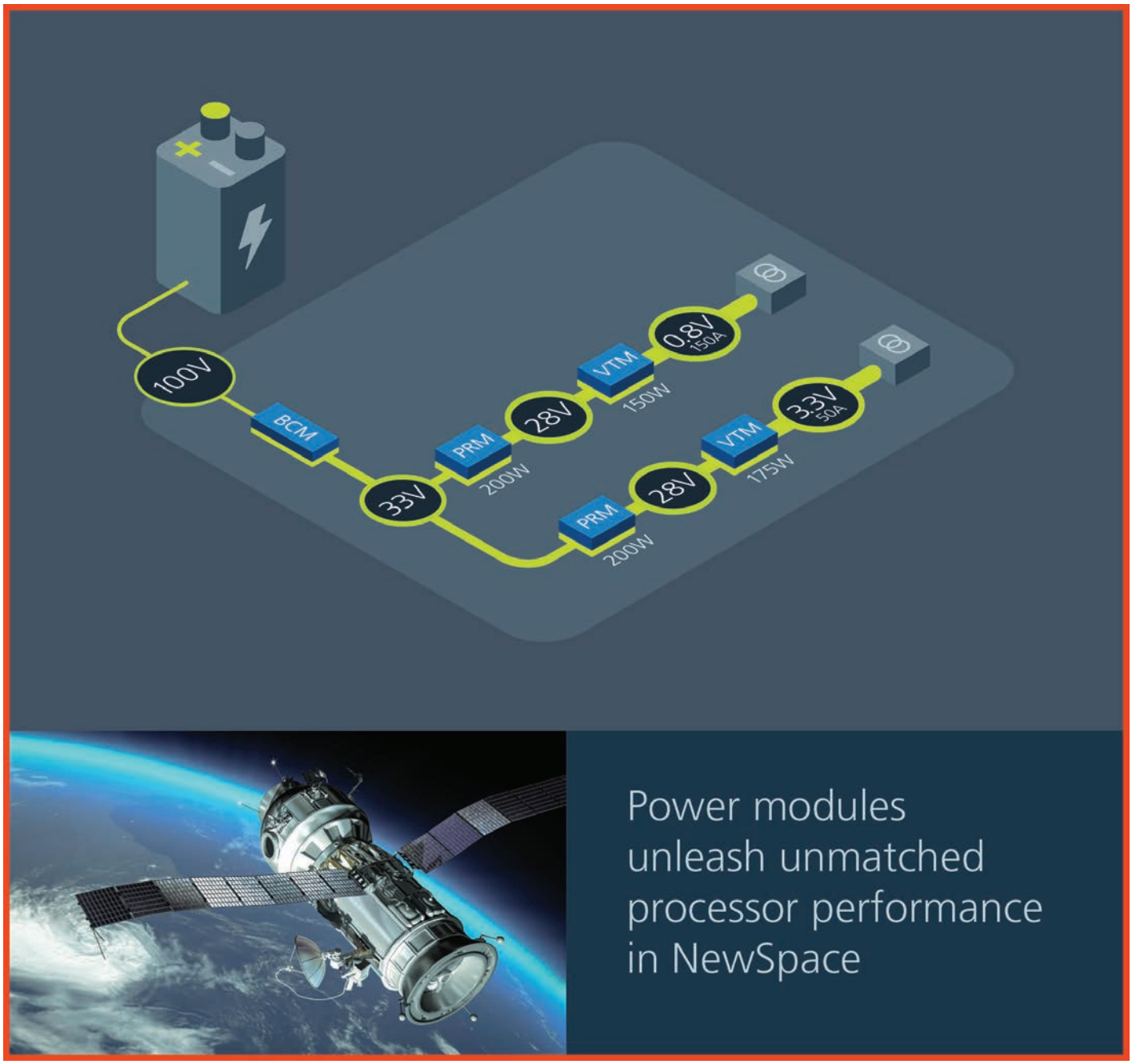

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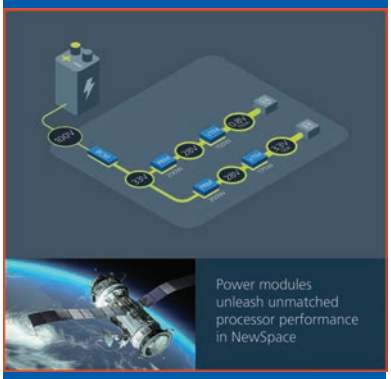
FEATURE STORY



NewSpace demands low voltage, high current power for performance and longevity

Matt Renola, Senior Director, Global Business Development – Aerospace & Defense

More details on page 16.

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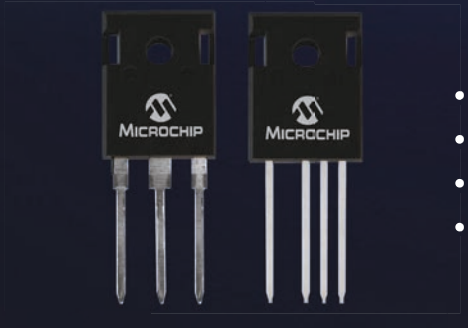

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Good Times for WBG

According to market researchers the rapid evolution of the WBG compound semiconductor market has positioned both SiC and GaN as key materials within the power device market. There has been a remarkable shift of interest in SiC for automotive applications and in power supplies as well as GaN for mainstream consumer applications and more recently for automotive. Since the first commercialization of SiC diodes, the power SiC device market has been driven by power supply applications. Nevertheless, automotive is becoming the killer application, following SiC's notable adoption for Tesla's main inverters in 2018. And as such many leading semiconductor manufacturers are increasing their SiC investments, from raw materials to chips.

Although Silicon is the most familiar technology, its smaller bandgap limits operating temperature, its low breakdown electric field restricts its use to lower voltages, and its low thermal conductivity limits power density compared to wide bandgap materials, like gallium nitride (GaN) and Silicon Carbide (SiC). GaN's high electron mobility is the property that enables its well-known and unmatched efficiency at very high switching frequencies - GaN offers the lowest switching loss.

In our feature "Finding the Right Technology to Solve Datacenter Power Challenges" Wolfspeed compared their 60-mΩ SiC device with a 50-mΩ GaN device in a totem pole PFC simulation to find that although GaN had slightly lower switching losses over the entire power range, any gains were offset by the increased conduction losses with power and consequently junction temperature increase. This requires GaN devices to be made oversized to compensate for higher conduction losses regardless of switching frequency.

For the efficiencies needed in datacenter power supplies, it is important to compare switching and conduction losses. Conduction loss, which is the device's I?R loss, is lower when the ON drain-to-source resistance (RDS(ON)) is low and changes less with temperature. It is interesting to note that both GaN and SJ devices boast a lower RDS(ON) below 25°C, which are temperatures not quite practical for datacenter power supplies. As datasheets for GaN and SJ devices often specify RDS(ON) at 25°C, it can mislead engineers into assuming that specification at the much higher operating temperatures for which systems are normally designed.

The GaN testing had to be stopped at 3 kW due to power limitations of the device. The study clearly demonstrated that SiC results in significantly lower total losses, especially at the high power levels at which WBG semiconductor use is most compelling, such in as datacenters. At first glance, GaN's benefits are the lowest reverse recovery charge Qrr for the lowest switching loss in continuous conduction mode (CCM) synchronized rectifier, the lowest time-related output capacitance Coss(tr) for low dead time, and high frequency and efficiency, and the lowest energy-related output capacitance Coss(er) for minimum switching loss in hard-switched topologies. Notice that SiC trails close behind GaN in these attributes, while Si lags significantly. Silicon wins include the lowest junction-to-case thermal resistance Rthjc, which confers better thermal performance, and the highest threshold voltage Vth, which offers better immunity to noise and makes Si devices easier to drive. GaN has an extremely low Vth.

Compared with Si-based H-bridge, SiC-based CCM totem pole PFC can have not only higher efficiency but higher power density at similar or lower cost. A comparison of efficiency between technologies clearly shows that while both SiC- and GaN-based CCM totem pole PFCs can achieve >99 % efficiency, GaN has the efficiency advantage only at very light loads. SiC provides an efficiency similar to that of GaN at half load and better efficiency at full load.

An automotive application describes our cover story from EPC. A 48 V mild hybrid is estimated to provide 70 percent of the benefit of a high-voltage hybrid at 30 percent of the cost while boosting electrical power available in the vehicle from 2.5 kW to 10 kW. These systems will require a 48 V – 12 V bidirectional converter, with power range between 1.5 kW and 6 kW. The design of a 2 kW, two-phase 48 V/12 V bi-directional converter using GaN FETs in QFN packages, achieving 96% efficiency is targeted for the 48 V mild hybrid system. The solution is scalable; two converters can be paralleled for 4 kW, three converters for 6 kW or only one phase can be used for 1 kW. GaN FETs suitable for 48 V applications typically have 4 times better figure of merit compared to equivalent MOSFETs. For the same gate voltage of 5 V, GaN FETs have at least 5 times lower gate charge than MOSFETs. Other important advantages of GaN FETs include lower COSS, faster voltage transition, zero reverse recovery and they are physically smaller. At full load, EPC eGaN FETs can operate with 96 % efficiency at 500 kHz switching frequency, enabling 1 kW/phase compared to silicon-based solutions, which are limited to 600 W/phase due to the limitation on the inductor current at 100 kHz maximum switching frequency.

With that the potential users have a guideline on choosing the right technology.

I have written this opinion in a hospital. I am looking forward to be back for electronica!

Achim Scharf
PEE Editor

SPONSORED FEATURE

Why gate drivers are key to successful electric vehicle designs

By Allegro MicroSystems

Power-conversion technology plays a key role in every electric vehicle. In a typical vehicle, the on-board charger (OBC) alone has as many as three power-conversion stages in addition to further high-power-conversion stages to drive the traction motors.

When embarking on the design of a new electric vehicle, gate drivers probably are not the first components that come to mind. Yet, choosing the right gate driver technology can cut costs and help designers create more-reliable, more-efficient vehicles.

Gate drivers are key to the design of power conversion systems, whether in electric vehicles or other applications. They enable the flow of large currents through power transistors, which are increasingly moving from silicon insulated gate bipolar transistors (IGBTs) to different transistor structures in materials such as silicon carbide (SiC) MOSFET and gallium nitride (GaN) enhanced mode transistors.

SiC transistors can handle higher voltages—up to 1700 V—and higher currents at higher temperatures than silicon IGBTs, while GaN devices support higher switching speeds—up to 2 MHz—enabling smaller system designs. All these power devices, and there can be many of them at each level of conversion in a design, need to be very robust and reliable to meet strict safety standards in an electric vehicle.

All these switches need different control voltages to be provided from the gate drivers as efficiently and accurately as possible. The gate drivers need to match the requirements of the power switches, and this is key to the performance of the system. The quickness of the switching of the devices and the quality of the output impact the performance of the whole power conversion.

The gate driver also needs to cope with a wide variety of conditions. Gate drivers can be situated on the low-voltage side of a bridge, or on the high-voltage side of the bridge, in the hostile environment of an inverter or in a charger.

As a result, a gate driver's performance is evaluated along multiple criteria: the ability to minimize the cost, size, and weight of the power-conversion modules while maximizing reliability and efficiency. Component count and design complexity influence all of these characteristics in a power-conversion module.

Choices for gate drivers are extensive, and choosing the driver is just where the work begins. Designers also need to provide a source of power to drive the gates of the switches. This can be a challenge. Supplies must frequently be isolated from the controlled ground, and multiple supplies are often required, which can create a new set of design challenges and trade-offs. Therefore, choosing the right gate driver technology can have a big impact on the success of a vehicle in the marketplace. However, it is not easy to find the right solution for a gate driver and its power sub-system.

Delivering reliable gate-drive signal and energy to the gate of any device is the first job of any gate driver, and this needs to be achieved with a low propagation time from the system controller to the FET gate. Low propagation time gives more flexibility for the management of the dead time between the ON and OFF cycles of the power devices, improving system efficiency.

Switch types, such as SiC MOSFETs and GaN transistors, have begun to exhibit improved switching transition speeds in recent years. This means the common mode transient immunity (CMTI) of the gate driver needs to be up to the challenge. Failure to meet this requirement will mean unexpected transitions on the transistor gate and potential destructive events in a system.

Conventional designs drive the gates of

Figure 1: Gate drivers are an increasingly important part of the design of on-board chargers and traction inverters for lithium ion battery systems in electric vehicles.

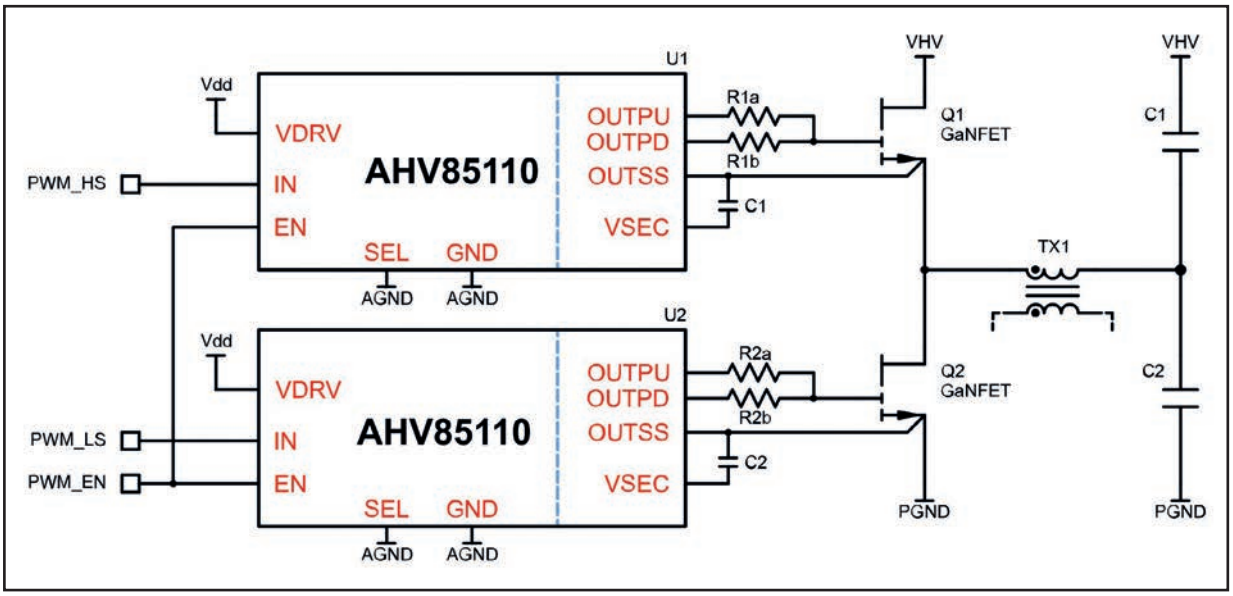

Figure 2: A typical half-bridge application that uses the Allegro MicroSystems AHV85110 gate driver with Power-Thru technology and eliminates the high-side bootstrap.

the power-module semiconductor switches using external DC-DC bias supplies. These designs are both complex and high in component count, and some require as many as eight or nine separate bias supplies, which typically include transformers and other bulky components.

In addition to the added cost, size, and weight that come with these bias supplies, the added component count and circuit complexity affect reliability. Even in designs where care has been taken to minimize the loading and stress on components, every component remains a potential point of failure. The bias supplies included in conventional designs add potential points of failure and must also be sized for the highest operational switching frequency, which results in less-efficient operation at lower frequencies.

ELIMINATING THE BIAS SUPPLY

Power-conversion technologies that require fewer components than conventional technologies have fewer points of failure, which directly improves reliability and leads to fewer potential warranty claims and enhanced product reputation.

One new approach to transfer power to gate drivers, is to use a novel magnetic coupling device within the integrated circuit to eliminate the need for bias supplies, which is what the Power-Thru technology from Allegro MicroSystems does: It transfers the gate on/off logic signal with the power needed to drive the gate of the switch, eliminating the need for external auxiliary power. The reduced component count and complexity cuts engineering time by making modules much easier to design and to qualify. This also allows the gate driver to track the power consumption of the gate control with the switching frequency, enabling automatic optimization of efficiency.

This technology reduces the size and weight of the gate driver and brings additional benefits. Smaller gate driver assemblies enable shorter signal paths with reduced parasitic capacitance and inductance, which reduces the risk of damage caused by ringing and voltage spikes. Smaller gate drivers also leave more space for the power stages, enabling the use of more-efficient designs.

The Power-Thru technology also removes the need for a bootstrap circuit to create the floating voltage required for controlling the high-side switches. This, in turn, eliminates all the trade-offs and complexity in choosing the optimal combination of components to use in this bootstrap circuit.

The Power-Thru technology consists of a tiny magnetic-based isolation structure that enables efficient power transfer across the boundary from the low-voltage signal to the high-voltage system. This boundary carries not only the gate drive signal information but also all the drive power required to drive the external FET switch. The magnetic coupling provides complete electrical isolation, so Power-Thru drivers are equally suitable for use in high-side, low-side, and isolated applications.

By eliminating the need for auxiliary power supplies, the Power-Thru gate drivers can free up time to concentrate on core design challenges.

In one example, nine separate bias rails were able to be merged into a single rail. The reduced component count can reduce BOM costs, system size, and build complexity. This reduced complexity can improve the likelihood of early success in testing and validation and can increase reliability in application as there are less parts that might fail.

The Power-Thru gate drivers also only require a single capacitor to be specified, which speeds design time and improves the likelihood of early design success.

Gate driver operation

For power-on, it is more important to think in terms of charge transfer than simply charging the input capacitance, C_{ISS}, of the FET. FET capacitances are also highly nonlinear, and the capacitance depends largely on the FET V_{DS}.

The high rate of change of voltages and currents in power-switching circuits can create inductor currents and capacitor voltage drops. One example is the false power-on of a FET due to a dv/dt event.

For example, after the power-off of the low-side FET and the elapse of a suitable dead time, power-on of the high-side FET occurs. This produces a rapidly changing switch-node voltage at the drain of the low-side FET. The resulting capacitor current flowing in the gate-drain capacitance, CGD, and driver output cause the voltage on the gate of the low-side FET to rise. If this voltage spike peaks beyond the threshold voltage, V_{TH}, the FET will conduct. Because the high-side FET is also conducting, a potentially destructive shoot-through event can result. As the typical FET capacitors are highly nonlinear and a function of V_{DS}, the effect of iCGD gate drive current can be more pronounced at lower values of V_{DS}.

This inevitable iCGD current must be managed correctly and emphasizes the importance of a strong driver pull down

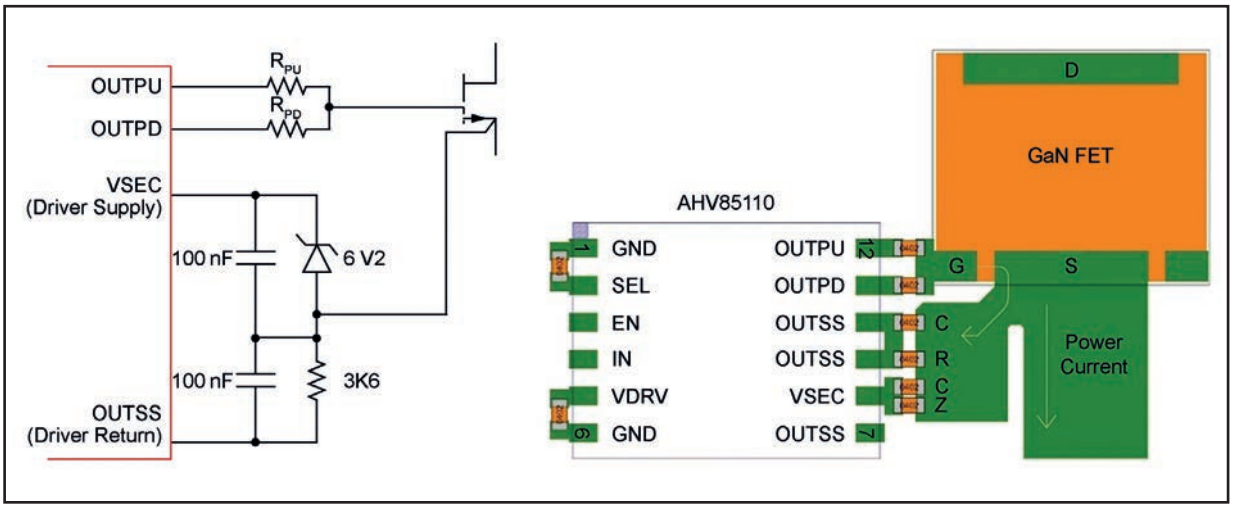

Figure 3: Avoiding false power-on events in a gate driver design.

and correct choice of gate resistor. The Allegro AHV85110 driver has independent pull-up and pull-down outputs, allowing independent choice of both resistors.

A popular method to further mitigate the effects of a false power-on event is through use of a bipolar output drive. Here, a suitable choice of driver supply voltage and Zener diode generates a voltage to prevent the false power-on event.

In any electronic circuit, there are many parasitic components that do not appear on the schematic. FET and IC bond wires and packaging along with PCB traces result in unwanted parasitic inductances. FET internal structures and overlapping PCB traces and power planes add circuit node capacitances. In most cases, these parasitic components have little or no impact on circuit performance. However, in power-switching circuits, they can have a severe effect and should be carefully considered. The internal structure, packaging, and pinout of the AHV85110 gate driver have been optimized to minimize such parasitics. The most effective way to reduce the external circuit parasitics is through good PCB layout.

The AHV85110 driver pinout easily facilitates the bipolar drive circuit without compromising on the key PCB layout guidelines.

PCB layout

Increasing the switching frequency can help to reduce the size of the magnet used in the power system, and it is now common to see switching frequencies greater than 500 kHz and even beyond 1 MHz in higher-power converter applications. This increase is further supported by the introduction of high-power, low $R_{DS(ON)}$ and low gate capacitance MOSFETs and GaN FETs.

The gate driver also needs to maximize the effectiveness of these FET switches. Faster switching edges both in the gate drive loop and the commutation loop are a continuous design challenge and the effects of PCB parasitic parameters can play a significant role in circuit operation.

PCB tracking and layout are fundamental parts of the operation of an electronic circuit. The PCB tracks introduce inductances and capacitances into the circuit, which can often be overlooked.

In power-switching circuits, these parasitic components can introduce voltage and current ringing on circuit nodes, which can greatly inhibit circuit performance and introduce undesired effects such as poor circuit operation and increased electromagnetic interference (EMI). A solution is often to add, after the fact, components such as snubbers and filters. A better approach is to eliminate or minimize the effects through good PCB layout practices.

Allegro drivers have the unique advantage in that they require the minimum of external components, particularly on the output side, which is the most critical from a PCB layout point of view. The drivers do not require a separate isolated or bootstrap diode—all of that functionality is included in the drivers using the Power-Thru technology.

The pinout of the device has been carefully designed for ease of PCB layout and optimal performance. The 12-pin, low-profile, surface-mount package (Allegro part number suffix LH) measures 10 mm × 7.66 mm × 2.53 mm. Several protection features are integrated, including undervoltage lockout on primary and secondary bias rails, internal pull-down on IN pin and OUTPD pin, fast response-enable input, and OUT pulse synchronization with first IN rising edge after enable, which avoids asynchronous pulses.

Good quality decoupling capacitors should be used for decoupling the primary, V_{DRV}, and secondary, CSEC, voltages, and the pinout of gate drivers such as the AHV85110 has been designed for the optimal positioning of these capacitors.

The FET drive on pin (OUTPU pin) and the FET drive off pin (OUTPD pin) can be implemented with direct connection to the FET gate or with series resistors to control the FET rise and fall times. Having these functions separated but adjacent on the module allows for independent control of the power-on and power-off times without the need for external parallel diode or transistor circuits, while still allowing the driver to be as close as possible to the driven FET.

The gate drive current return to the module is through the OUTSS pins, which are positioned to minimize the loop area for the gate current.

An example PCB layout is shown for the AHV85110 used with a commercially available GaN FET and following the recommended layout for the FET. The ever-increasing switching frequencies of power converters results in faster voltage and current transition edges—higher dv/dt and di/dt.

This higher-frequency operation, reduced dead time, and sharper switching edges means EMI considerations are also increasingly important yet are often the last considerations in a system design, which can make finishing a design difficult and time consuming. The reduction of components and circuits in and around the gate drive design helps dramatically reduce the EMI challenge in a system design through lower common-mode capacitance (Ccm). This reduces the circulating currents, reducing any EMI and reducing test time.

Good PCB layout practices can significantly reduce second-order effects, such as EMI, and can reduce or eliminate

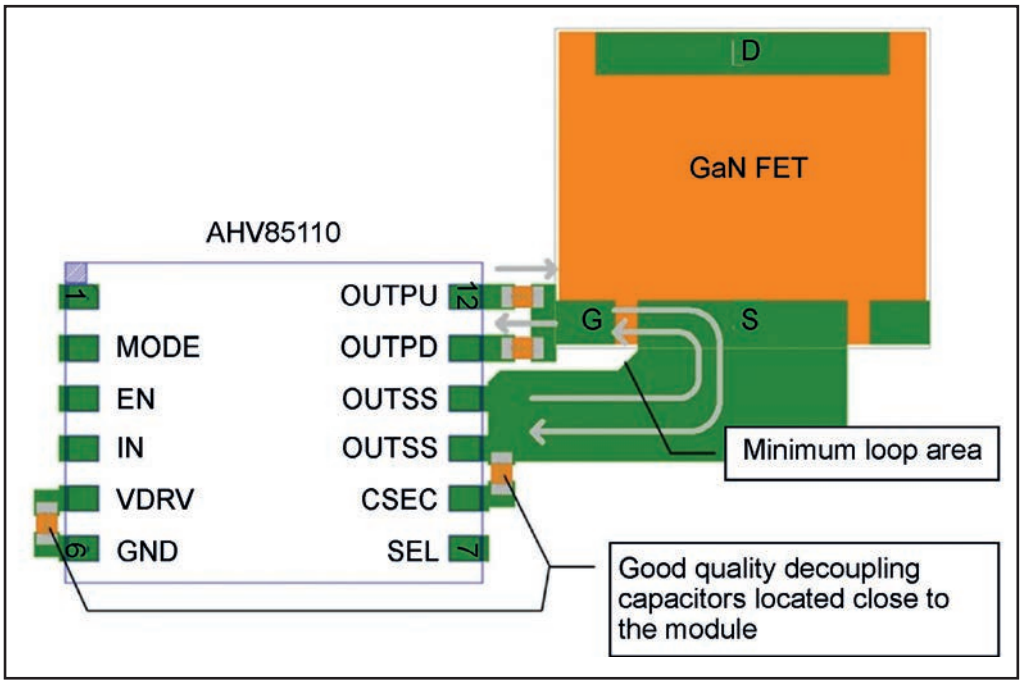

Figure 4: How the gate driver pinout reduces current loops in the PCB.

the need for circuits such as snubbers or filters required to manage these phenomena. Allegro has developed the AHV85110 and AHV85111 isolated GaN and MOSFET drivers with Power-Thru magnetic isolation to make this process easier, resulting in more effective gate drive designs.

Evaluation

The Allegro APEK85110 Half-Bridge Driver Switch Board is a demo board containing two AHV85110 gate drivers and two GaN FETs in a half-bridge configuration. This can be used to perform double pulse tests or to interface the half bridge to an existing LC power section. The isolated AHV85110 driver does not require secondary-side power or bootstrap components. Gate drive power is supplied to the secondary side from the primary-side supply voltage, V_{DRV}, and the amplitude of the gate drive can be varied by varying V_{DRV} between 7 and 15 V.

The evaluation board uses a bipolar gate drive arrangement, which is useful to mitigate against the effects of gate-drain capacitor currents. The secondary supply voltage is a function of the primary supply voltage and the Zener diode regulates the positive power-on voltage of the GaN FET. During the power-off period, the gate voltage is negative to allow more margin before the threshold voltage can be reached.

Ensuring availability

To keep production lines running, availability of devices is also key amidst a shortage of components for automotive designs. Car makers around the world have suffered from shortages of components such as gate drivers, and designers are increasingly aware of the supply chain issues of the devices they use.

The innovative magnetic isolation of the Allegro Power-Thru devices is built on standard 180 nm CMOS technology from dual-sourced tier one fabs, allowing flexibility of sourcing. Industry-leading packaging vendors and a range of second-source strategies are also used to ensure a secure supply of devices for some of the smallest high-voltage and high-efficiency power systems available.

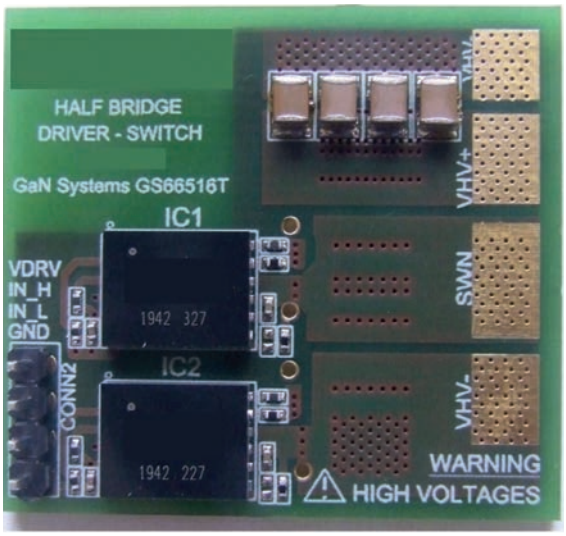

Figure 5: The APEK85110 half-bridge driver switch board.board.

Conclusion

The choice of gate driver is a key decision in the development of the power system of an electric vehicle. Whether this is a car, scooter, mining dump truck or tractor, the gate driver is there, controlling the power transistors in any power-conversion system.

The move to SiC and GaN transistors means there are many more factors for a designer to consider. The higher power, higher temperatures, and higher frequencies used with these devices are putting more focus on reliability of the design, which in turn is driving a reduction in the number of components. Smaller weight and size are also driving down the size of designs. All of this is driving up the levels of integration and the demands on the gate driver devices.

The Power-Thru magnetic isolation in the Allegro gate drivers enables higher levels of integration that can help to address issues such as EMI and parasitic effects on the board, reducing the time needed to design, test, and certify a system.

All these factors—along with the secure supply of the components in the design—must be considered when designing a power system for an electric vehicle.

Wolfspeed grows to meet supply challenge and launches high performance Gen 3+ die

Silicon Carbide (SiC), known for long as the ideal semiconductor technology for power devices, has with design and manufacturing innovation not only increased its share of the existing market but enabled new applications, such as electric vehicles (EVs), by offering higher power density, better high-speed switching performance, higher breakdown field, higher thermal conductivity, higher chip temperatures, and lower leakage currents than are possible with Silicon (Si). **Anri Mikirtichev, Product Marketing Engineer, Wolfspeed, Amy Romero, Power Die Applications Engineer, Wolfspeed**

Wolfspeed has led the SiC industry with the first commercial wafers in 1991, diodes in 2001, and MOSFETs in 2011. The company's technology development has supported its relentless march toward larger wafer diameters and lower costs, higher quality, and greater device performance. The company has more than 35 years of SiC development experience and over 7 trillion device field hours.

This widely recognized success is evident from its recent selection by General Motors (GM) as their strategic SiC power device supplier [1]. GM is participating in the Wolfspeed Assurance of Supply Program (WS AoSP) for domestic, sustainable, and scalable materials in EV production.

It comes as no surprise that the same success was recently responsible for a rapid, wafer-shortfall-inducing growth in SiC demand from EV, solar and datacenter applications.

Yole Devéloppement forecasts the EV market the biggest opportunity for SiC, worth over $5 billion in 2027, while the charging infrastructure market continues growing at 90% CAGR through 2025. Yole expects SiC to gain market share in the long term as companies like Wolfspeed overcome all challenges, including those related to supply, cost, and performance (Figure 1).

Resolving supply & cost challenges

Commanding nearly 60% of the N-type SiC substrate market in 2018-2019 as estimated by Yole, Wolfspeed is naturally the supplier to resolve supply challenges due to growing market confidence in SiC. The company is investing $1 billion in a new 200-mm wafer-capable Mohawk Valley Fab (MVF) [2] and converting its existing facility into a materials mega-factory.

While competitors are still using 150-mm fabs, Wolfspeed is leveraging vertical integration and internal "cycles of learning" to address demand and cost with 200-mm wafers from the new automotive-qualified automated facility.

The MVF construction is complete, the first 200-mm wafers demonstrated, and the fab is undergoing qualification for mass production.

Figure 2: Wolfspeed is leading the industry in taking 200-mm Silicon Carbide

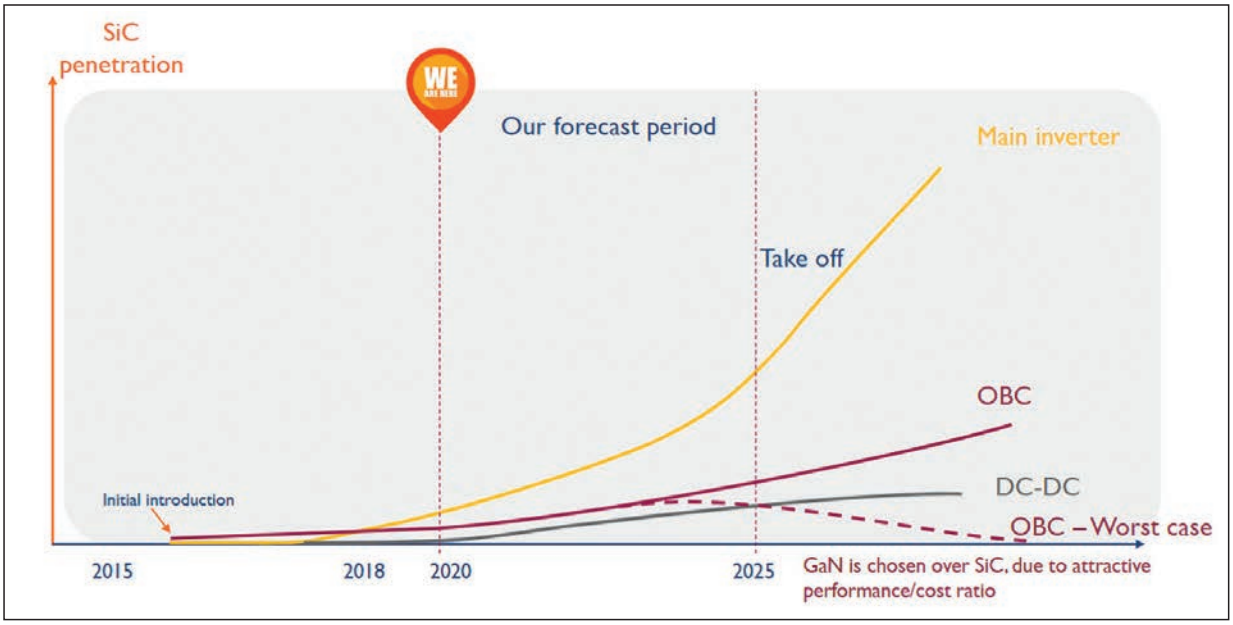

Figure 1: EV/HEV market outlook to 2030. **Source: Power SiC Materials, Devices and Applications, Yole Devéloppement**

Figure 2: Wolfspeed is leading the industry in taking 200-mm Silicon Carbide wafers from prototype to production. The new Mohawk Valley Factory fabrication facility is shown above.

wafers from prototype to production. The new Mohawk Valley Factory fabrication facility is shown above.

Upping the performance ante

Among key performance parameters that help meet EV requirements are the SiC MOSFET drain-to-source ON resistance, RDS(ON), and rated junction temperature, T_j, with the former responsible for conduction losses and thermal waste and the latter the device reliability and its ability to withstand heat.

Wolfspeed has continued innovation to address these concerns with a new Gen 3+ 750 V bare-die MOSFET (Figure 3) that has already won several contracts. Coming

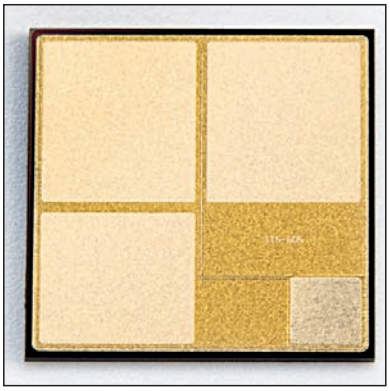

Figure 3: The Gen 3+ 750 V MOSFET sets new standards for low $R_{(DSON)}$ and temperature qualification.

in a 5mm x 5mm-layout and 180-µm thickness, it features low internal gate resistance R_g to optimize current rise-time and switching losses. Importantly, the new device boasts low on-state resistance ($R_{DS(ON)}$) and high maximum junction temperature (T_J).

Gen 3+ 750 V Characteristics

Compared with Wolfspeed's 650 V, 15 mΩ MOSFET die with T_j rated to 175°C, the Gen 3+ product improves on $R_{DS(ON)}$ per unit area as well as total area to reach 10 m . The 750 V rating improves the FIT rate and the MOSFET also elevates the T_j rating to above 175°C (200°C data shown) for peak condition operation during the vehicle mission profile. The temperature-stable $R_{DS(ON)}$ increases overall efficiency as well as system temperature limits (Figure 4).

Gen 3+ technology offers similar stability for the gate threshold voltage, V_{th}, giving designers enough headroom to switch aggressively while avoiding spurious turn-on (Figure 5). Combined with a high capacitance ratio, the stable V_{th} allows for safe operation without shoot-through concerns at elevated temperatures.

Moreover, Wolfspeed uses an Ni/Pd/Au metallization stack-up on both die sides to allow double-sided soldering/sintering. This new metallization used on Wolfspeed's automotive die opens the option for more advanced packaging solutions that can lead to better performance from the die and better reliability of the package. Examples of this include sintering copper clips or films to the top of the die and using copper wire bonds for higher current

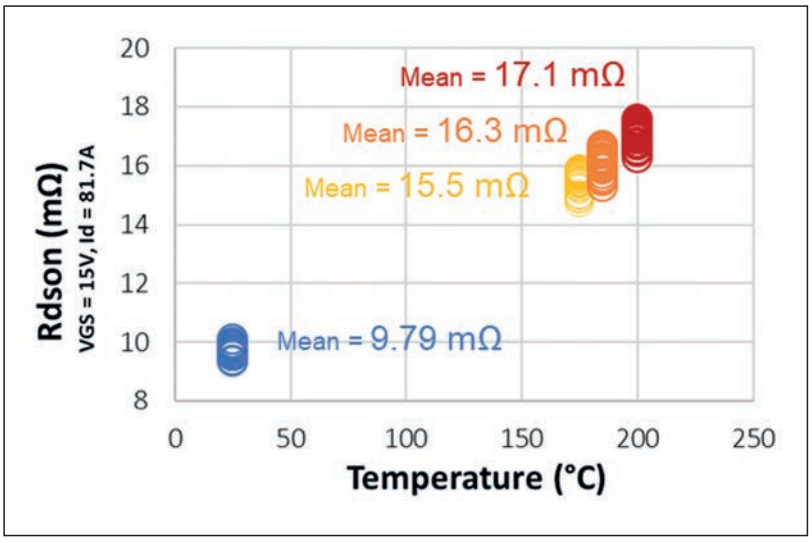

Figure 4: The Gen 3+ 750 V MOSFET $R_{DS(ON)}$ (blue) remains low and stable over 25°C-to 200°C range against the competition.

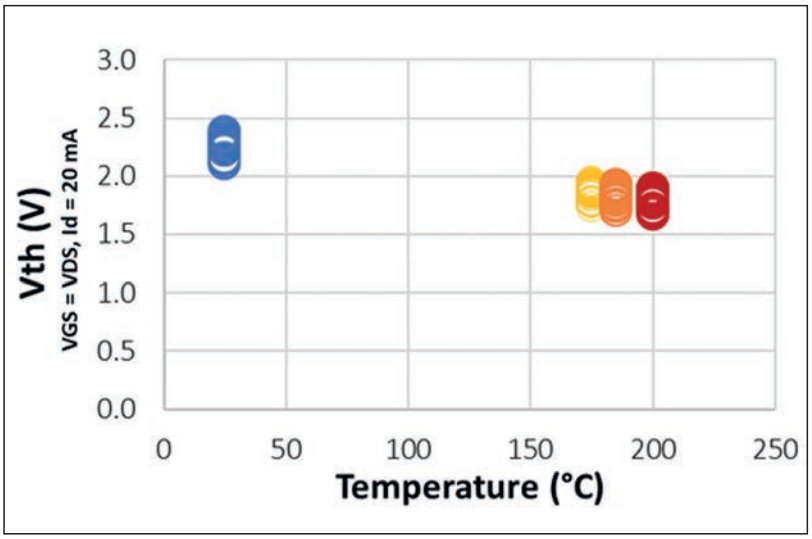

Figure 5: The new device offers a temperature-stable V_{th} (blue) for greater freedom in avoiding spurious turn ONs.

carrying and thermal capabilities (Figure 6).

Figure 6: The double-sided Ni/Pd/Au plated metal stack-up double-sided copper soldering/sintering for higher current and thermal performance.

Robust performance for automotive apps

The AEC-Q101-qualified MOSFETs are robust enough to withstand failure modes like short circuit and surge, which are important factors to consider in automotive applications where high robustness is necessary. [3]

This die has high energy capabilities of 1.2 J in short circuit conditions and >2.6µs withstand time at a junction temperature of 175°C. This short circuit withstand time (tested under worst case conditions) offers an adequate safety margin for gate driver technology to handle the fault. The devices have also been tested to withstand surge currents of up to 340 A or, depending on application conditions, >3x rated current. This surge current capability is important for active short circuit modes or other high current events.

The die is also capable of withstanding high temperature excursion events up to 200°C for a limited time without affecting device reliability. This functionality was demonstrated with extended high temperature AEC-Q101 tests at 200°C for 168 hours.

Switching performance tests under standard conditions demonstrated 30 V/ns and 4 A/ns switching speeds, without exceeding the voltage rating during transients. The device also exhibited consistent switching losses over temperature, with only a 150 µJ increase in total switching losses in a device tested from 25°C to 175°C. The fast switching capability of these devices and stable operation over temperature leads to overall lower switching losses in the system.

Summary

Wolfspeed has shared new details of its 200 mm expansion and new automotive-qualified 750 V MOSFETs designed for use in electric vehicle powertrain applications. Robust operation to 200°C, strong short-circuit energy (1.2 J) and time (> 2.6 µs) capabilities, surge currents up to 340 A, and low (10 m) conduction losses have enabled the 750 V, 10 m SiC MOSFETs to be successfully designed into new battery electric vehicles.

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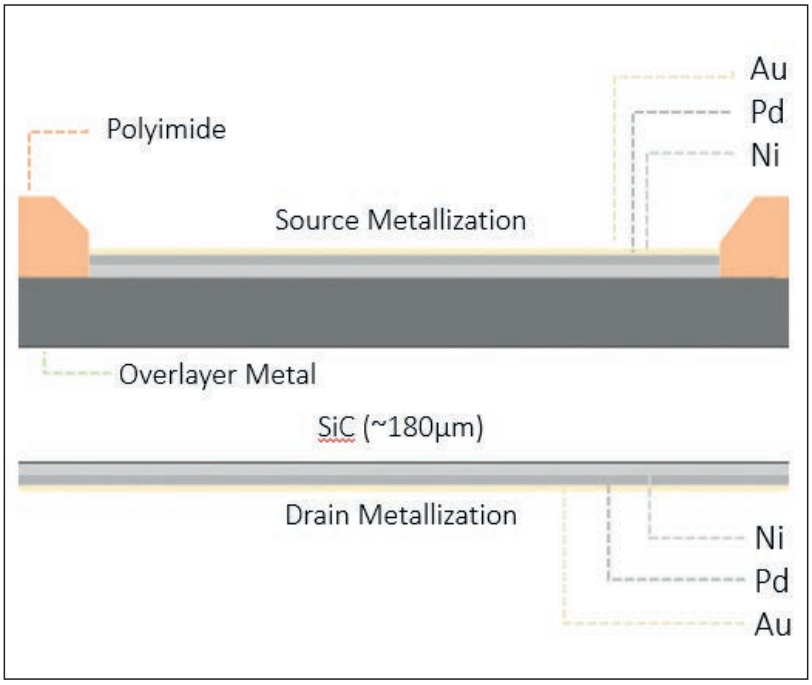


Figure 6: The double-sided Ni/Pd/Au plated metal stack-up double-sided copper soldering/sintering for higher current and thermal performance.

GaN Power Behind Mild Hybrid Vehicle Electrification

The hybrid vehicle market has more than doubled from 2017 from 2.0 to 5.1 percent [1] and by 2025, one of every 10 vehicles sold worldwide is projected to be a 48 V mild hybrid. 48 V systems boost fuel efficiency, deliver four times the power without increasing engine size, and reduce carbon-dioxide emissions without increasing system costs. A 48 V mild hybrid is estimated to provide 70 percent of the benefit of a high-voltage hybrid at 30 percent of the cost while boosting electrical power available in the vehicle from 2.5 kilowatts (kW) to 10 kW [2]. These systems will require a 48 V – 12 V bidirectional converter, with power range between 1.5 kW and 6 kW. The design priorities for these systems are size, cost, and high reliability.

Michael de Rooij and Yuanzhe Zhang, Efficient Power Conversion Corporation (EPC), USA

This article discusses the design of a 2 kW, two-phase 48 V/12 V bi-directional converter using GaN FETs in QFN packages, achieving 96% efficiency that is targeted for the 48 V mild hybrid system. The solution is scalable; two converters can be paralleled for 4 kW, three converters for 6 kW or only one phase can be used for 1 kW. Furthermore, the heatsinking capability can be considered infinite given the ultimately function will be inside a vehicle with the unit mounted to the chassis having a significantly larger heat flux capability compared to the losses generated.

Design of the 48V/12V Bi-directional DC/DC Converter

A simplified block diagram schematic of the bi-directional DC-DC converter is shown in Figure 1. The synchronous buck/boost converter is the simplest bi-directional converter, wss selected as the base topology. Other supporting circuitry includes current sensors, temperature sensor, digital controller, and housekeeping power supply.

GaN FETs suitable for 48 V applications typically have 4 times better figure of merit (die area · times $R_{DS(on)}$) compared to equivalent MOSFETs [3]. For the same gate voltage of 5 V, GaN FETs have at least 5 times lower gate charge than MOSFETs. Other important advantages of GaN FETs include lower C_{OSS}, faster voltage transition, zero reverse recovery and they are physically smaller.

The GaN FET chosen for this design is the EPC2302 [4]. It has a low inductance 3 x 5 mm QFN package with exposed top for excellent thermal management. With 1.8 mΩ $R_{DS(on)}$, the rated peak DC current is 101 A. Therefore, the two-phase approach is selected so that the FET current requirement is reduced, i.e., at 14 V 2 kW output, the DC current in each phase is 70 A. This also reduces the current rating requirement for the inductors.

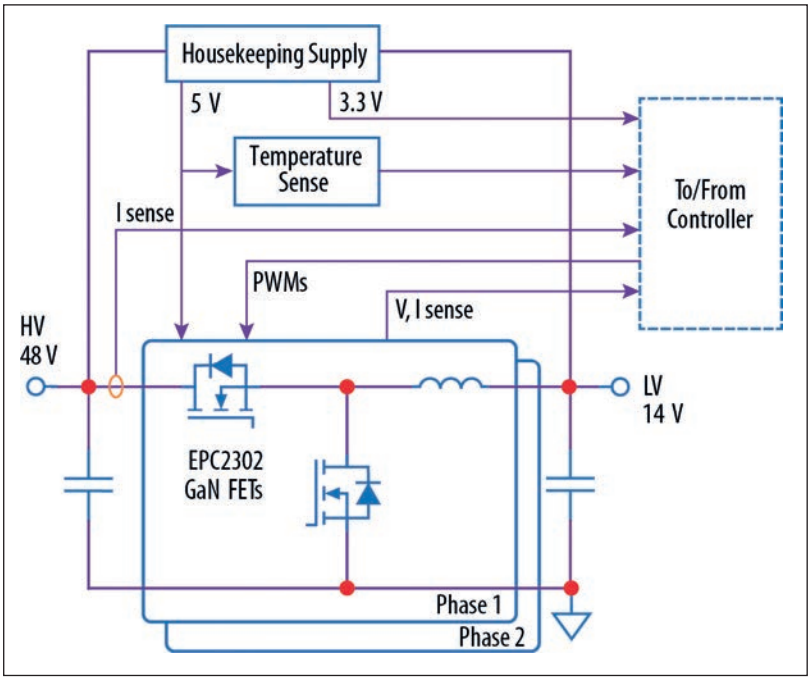


Figure 1: **Simplified schematic diagram of the multi-phase bi-directional converter**

The MPQ1918-AEC1 [5] gate drivers in this design are AEC-Q100 qualified and use bootstrap technique with voltage clamping for driving the high side FET. These drivers also have fast propagation times and excellent propagation delay matching of less than 1.5 ns typical.

Vishay IHTH-1125KZ-5A series inductors [6] offer high current ratings for the inductance. In this design, the 1.0 µH inductor and 500 kHz switching frequency was selected, resulting in 80 A peak inductor current.

To ensure accurate phase current balancing, current sensing using precision shunt resistor is preferred over inductor DCR current sensing. However, shunt resistors that are rated for above 70 A usually have large footprints, and therefore high parasitic inductance. This inductance can result in high noise that saturates the current sense amplifier and voids the measurement. A simple solution is to add an RC filter network with a matched time constant. MCP6C02 current sense amplifier is used in this design, with a maximum bandwidth of 500 kHz and 50 V/V gain. This results in 10 mV/A total current sensing gain for 0.2 mΩ shunt.

Symmetrical layout between the two phases is also critical in phase current

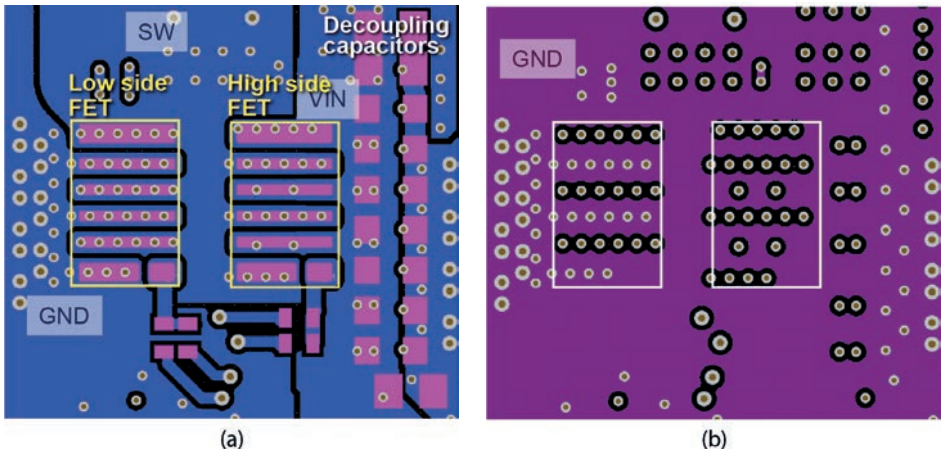
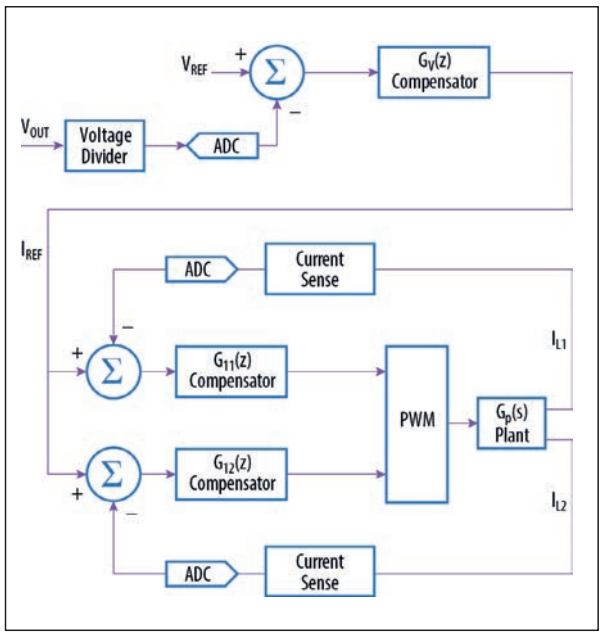
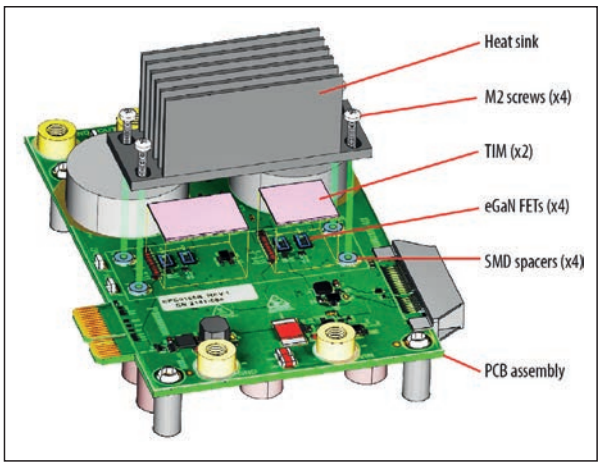


Figure 2: Example layout of the top two layers of the printed circuit board around GaN FETs; (a) top layer consisting of ground (GND), switching node (SW) and input (VIN) nets, and (b) middle layer 1 of solid ground plane



LEFT Figure 3: Digital average current mode control diagram



ABOVE Figure 4: Heatsink installation view, showing the metal spacer, thermal interface material

balancing and minimizing other effects from mismatch, such as gate drive delay, switching transition speed, overshoot, etc. Figure 2 shows the layout example around the GaN FETs in this design, which utilizes the internal vertical layout technique [3] by placing the decoupling capacitors close the FETs with a solid ground plane underneath.

Digital control

A dsPIC33CK256MP503 [5] digital controller from Microchip is used in this design. It is a 16-bit processor with a maximum CPU speed of 100 MIPS. The pulse- width modulation (PWM) module can be configured in high-resolution mode, resulting in 250 ps resolution in duty cycle and dead times, allowing accurate adjustment of dead times to fully exploit the high performance of GaN FETs.

Digital average current mode control is implemented for both buck and boost modes. The current sensing circuitry consists of sense resistors and differential amplifiers. In this design, low loss 0.2 mΩ sense resistors and low-noise amplifiers MCP6C02 are used. The control block diagram is shown in Figure 3. The same current reference IREF is used for the two independent current loops. As a result, the current in both inductors will be regulated to the same value. The bandwidth of the two inner current loops are set to 6 kHz, and the outer voltage loop bandwidth is set to 800 Hz.

Thermal management

At full output power of 2 kW, a heatsink is required for the GaN FETs. A standard commercially available 8th brick heatsink is used. Four metal spacers are installed on the PCB to provide the appropriate clearance for the heatsink mounting. A thermal interface material (TIM) is required between the FETs and heatsink. Usually, the material needs to have a) mechanical compliance due to compression, b) electrical insulation and c) good thermal conductivity. In this design, a TIM with 17.8 W/mK is used. Figure 4 shows the 3D heatsink installation view.

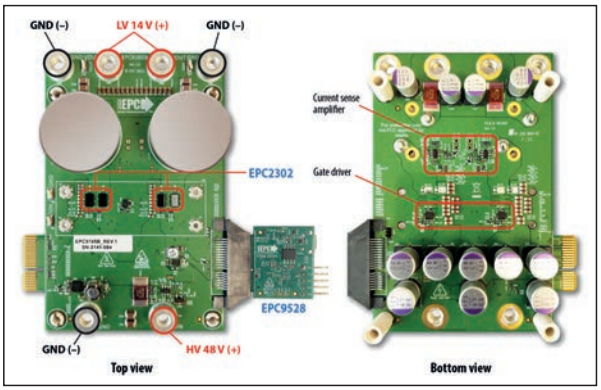
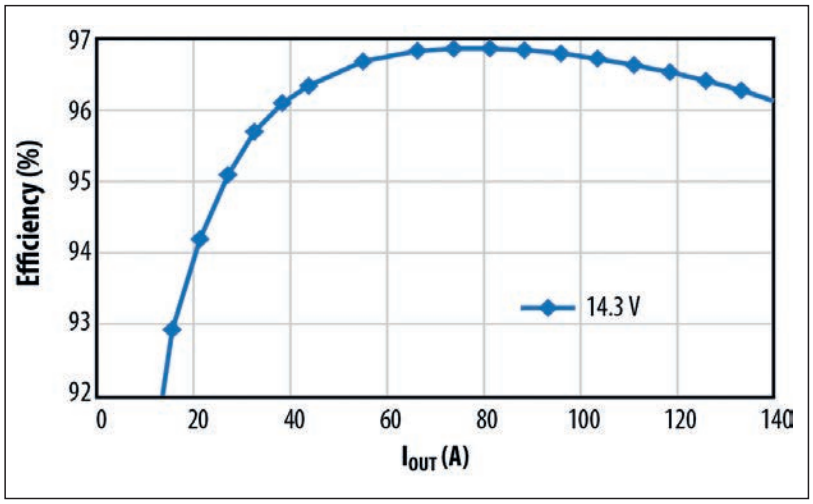
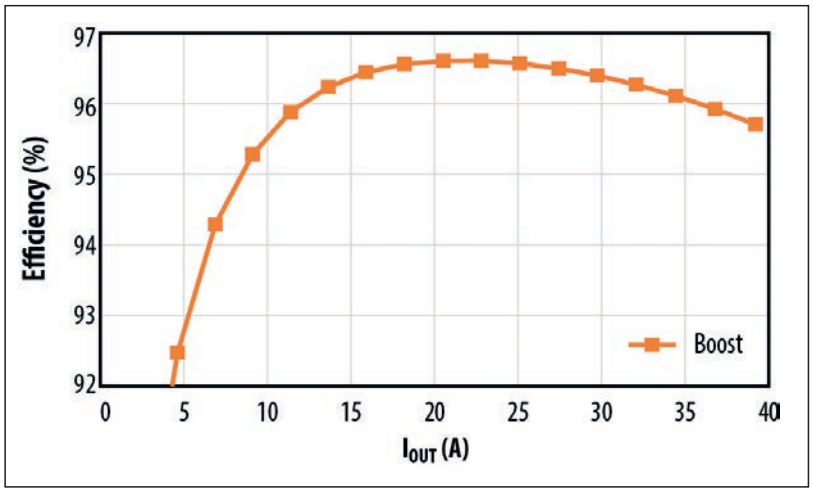


Figure 5: Photo image of the EPC9165 converter with the EPC9528 dsPIC33CK controller module attached



LEFT Figure 6: Measured converter efficiency at 500 kHz, 48 V input and 14.3 V output



LEFT Figure 7: Measured converter efficiency at 500 kHz, 14.3 V input and 48 V output

Design validation results

Figure 5 shows a photo of the EPC9165 [6] converter without the heatsink mounted. The dimensions are 4.3x2.8x1.6 inches (108 mm x 70 mm x 40 mm) excluding the edge connectors.

With the heatsink installed and 1700 LFM airflow, the converter was operated at 48 V input, 14.3 V output and tested at 500 kHz, and the efficiency results are shown in Figure 6. At 500 kHz, using a 1 µH inductor, the converter achieved a peak efficiency of 97 %. The converter was also tested at 14.3 V input and 48 V output for boost mode operation, as shown in Figure 7.

At full load, EPC eGaN FETs can operate with 96 % efficiency at 500 kHz switching frequency, enabling 1 kW/phase compared to silicon-based solutions, which are limited to 600 W/phase due to the limitation on the inductor current at 100 kHz maximum switching frequency.

Conclusions

With increasing legislation aimed at higher fuel efficiency standards, vehicle manufacturers are searching for cost-effective solutions to meet these demands while still providing the power required for ever-increasing electronically driven functions. This article introduced a bi-directional high power converter for mild-hybrid cars and battery power backup units using four EPC2302 GaN FETs. When converting between 48 V and 14.3 V, the efficiency exceeds 96 % with 500 kHz switching frequency. This scalable solution can be used to meet the power requirements of the latest 48 V mild hybrid systems.

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NewSpace demands low voltage, high current power for performance and longevity

Matt Renola, Senior Director, Global Business Development – Aerospace & Defense

Satellite operators are offering increasingly sophisticated on-board processing capabilities necessitating the use of the latest ultradeepsubmicron FPGAs and ASICs. These have demanding, low-voltage, high-current, power requirements and OEMs are being challenged to offer more functionality from smaller payloads and platforms. Cost and time-to-market are also key drivers!

Relatively, smaller satellites harvest less energy and with operators increasingly using faster and more on-board processing, there is a requirement that as much of the possible power budget is available for the payload. Traditional power-distribution architectures comprising an isolated DC-DC to step-down the external bus input, followed by localized POLs to produce the required load voltages, are becoming too inefficient because of large I2R drops. To deliver the next generation of New Space missions, improvements are needed in conversion loss, power density, physical size and a transient response compatible with the switching speeds of the latest ultradeepsubmicron devices.

Instead of the conventional, intermediate power-distribution comprising an isolated DCDC followed by buck bricks, Vicor Corporation's patented Factorized Power Architecture (FPA™) uses a modular approach to minimize I^2R distribution losses, maximize efficiency and improve transient response.

The FPA comprises two stages: voltage regulation followed by transformation. First, a buck-boost topology is used to generate a 48V intermediate rail from an external source, which is significantly higher than the lower legacy buses typically input to POLs. For example, a 48V output bus requires four times less current than a 12V intermediate bus for the same power ($P = VI$) and PDN losses are the square of the current ($P = I^2R$), which reduces by sixteen. Placing a regulator first to produce 48V achieves the highest efficiency, allowing smaller satellites to avail of more of the harvested energy.

The second stage of the FPA uses a transformer to convert the 48V intermediate rail to the desired load voltage, e.g. 1V. The output is a fixed fraction of the input (K-factor) defined by the turns ratio. Stepping down the voltage increases the current by the same amount, e.g. a 1A input current would be multiplied to an output of 48A:

A Pre-Regulation Module (PRM™) and a Voltage-Transformation Module (VTM™) current multiplier combine to realize the FPA, with each device fulfilling its specialized role to enable complete DC-DC conversion. The PRM generates a regulated 'factorized bus' from an unregulated input followed by the VTM, which transforms (steps down) the 48V to the desired load voltage.

The VTM's high bandwidth avoids the need for large point-of-load capacitance. Even without any external output capacitors, the output of a VTM exhibits a limited voltage perturbation in response to a sudden power surge. A minimal amount of external bypass capacitance (in the form of low ESR/ESL ceramic capacitors) is sufficient to eliminate any transient voltage overshoot. Without imposing the bandwidth limitations of an internal control loop struggling to maintain regulation, the VTM offers a unique capacitance-multiplication feature. For example, the effective, shunt output capacitance is 2304 times the input capacitance when a K factor of 1/48 is used, i.e. $C_{SEC} = C_{PRI} * K^2$. This means that significantly less decoupling is needed downstream of the VTM and only a small amount of capacitance at its input offers the same energy storage as the bulky tantalums typically added to the 1V output of a traditional buck brick as illustrated in Figure 1.

Low impedance is a key requirement for powering low-voltage, high current loads efficiently and the use of a VTM also reduces the effective resistance seen from the secondary side by K^2. This allows the VTM to be placed at the load, either laterally or vertically, resulting in a lower-loss PDN. The FPA's lower-current, higher-voltage intermediate bus means that the PRM can be located physically away from the VTM without impacting efficiency. This

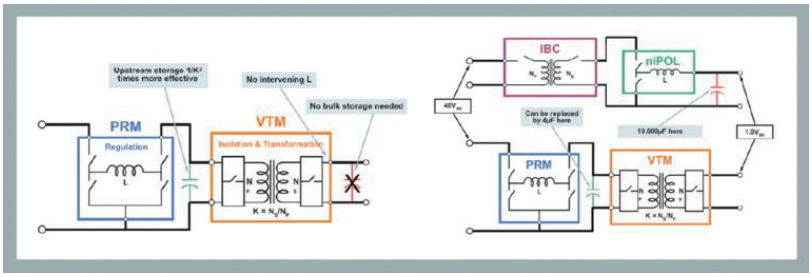

Figure 1: These diagrams show how the FPA compares to a traditional, intermediate architecture.

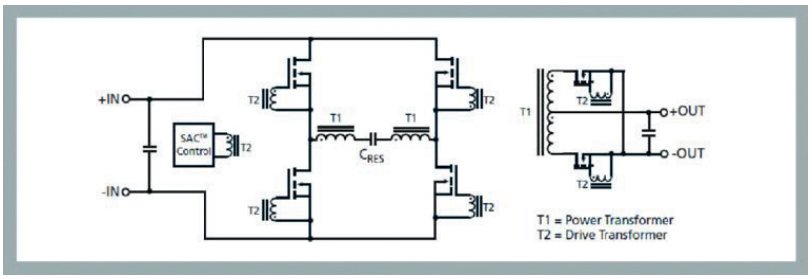

Figure 2: The full-bridge, SAC series-resonant topology offers advantages over existing space-grade DC-DCs.

gives you more flexibility when deciding where to place the PRM, less worries about area congestion at the load and more freedom to size power planes for maximum current density. This floor-planning is very different to the traditional brick approach, which requires the isolated DC-DC and POLs to be close together to minimize I^2R distribution losses.

Present space-grade, isolated DC-DCs and buck POLs are PWM-based devices with the output power proportional to the duty cycle of the switching frequency. These hardswitched converters use a square wave to drive an inductor or transformer with the MOSFET dissipating energy as it is turned on and off. A square wave contains lots of harmonics that must be filtered or they will conduct or radiate throughout the system. The VTM's topology uses a sinusoidal current in the primary winding, producing a cleaner output noise spectrum requiring less filtering. Existing space-qualified buck regulators and forward/flyback DC-DCs specify efficiencies in the range of 67 – 95% and 47 – 87% respectively.

Today, there are 12 suppliers of space-grade switching POLs offering almost 30 nonisolated convertors. Input voltages range from 3 to 16V, load voltages and currents from 0.785 to 9.6V and 4 to 18A respectively, with switching frequencies from 100kHz to 1MHz. Previously, I described the theory of conversion for the buck topology, what criteria to consider when selecting space-qualified parts, and how to choose values for the inductor, input, and output capacitance.

There are seven vendors of space-qualified isolating DC-DCs offering over 30 families of parts generating single, double, or triple standard voltages, or in some cases, adjustable, regulated, stepped-down intermediate outputs. Power ratings range from 2.5 to 500W. Previously, I described the theory of conversion for the forward and flyback topologies.

To meet the power-distribution and low-voltage, high-current needs of future NewSpace constellations, Vicor is qualifying its novel, Sine Amplitude Converter (SAC™) topology for space applications. This patented, ZCS/ZVS technology offers higher efficiencies, larger power densities, and lower EMI emissions than existing space-grade DC-DCs. SAC is a transformer-based, series-resonant, forward architecture that operates at a fixed frequency equal to the resonance of a primary tank circuit as shown in Figure 2.

The FETs in the primary side are locked to the natural resonant frequency of the series tank circuit and switch at zero-voltage crossing points, eliminating power dissipation and increasing efficiency. At resonance, the inductive and capacitive reactances cancel minimizing the output impedance, which becomes purely resistive reducing droop. The resulting very-low output impedance allows the VTM to respond almost instantaneously ($< 1\mu s$) to step changes in the load. The current flowing through the tank is a sinusoid that contributes less harmonic content, resulting in a cleaner output noise spectrum, requiring less filtering of the load voltage.

The SAC has a forward topology with the input energy passing to the output. The leakage inductance of the primary is minimized since it is not a critical storage element. The unique operation of the SAC forward topology enables a higher switching frequency and the use of smaller magnetics with lower intrinsic losses. The resulting increase in efficiency means less power is wasted during conversion, easing thermal management and allowing for more output current and a larger power density from a smaller package. Faster operation transfers energy to the output more often, improving the transient response to dynamic load changes to a few cycles.

Vicor is planning to bring to orbit a range of DC-DCs. Parts have already been de-risked and designed-in by **Boeing for an O3b satellite** offering space-based internet. Initially four rad-tolerant DC-DCs will be offered:

- A 300W, 9A, 849W/in³, isolating, ZVS/ZCS, SAC bus converter module (BCM3423PA0A35C0S), which accepts a DC source from 94 to 105V and outputs a fixed load voltage 1/3 of the input, ranging from 31 to 35V. Its maximum ambient efficiency is specified at 94% in a package size of 33.5×23.1×7.4mm weighing 25.9g.
- A 200W, 7.7A, 797W/in³, non-isolating ZVS buck-boost regulator, (PRM2919P36B35B0S), which accepts an input from 30 to 36V and outputs an adjustable load voltage from 13.4 to 35V. Its maximum ambient efficiency is specified at 96% in a package size of 29.2×19.0×7.4mm weighing 18.2g.
- A 200W, 50A, 1204W/in³, isolating, ZVS/ZCS, SAC DC-DC (VTM2919P32G0450S), which accepts a line voltage from 16 to 32V and outputs a fixed load voltage of 1/8 of the input, ranging from 2 to 4V. Its maximum ambient efficiency is specified at 93% in a package size of 29.2×19.0×4.9mm weighing 11g.
- A 150W, 150A, 903W/in³, isolating,

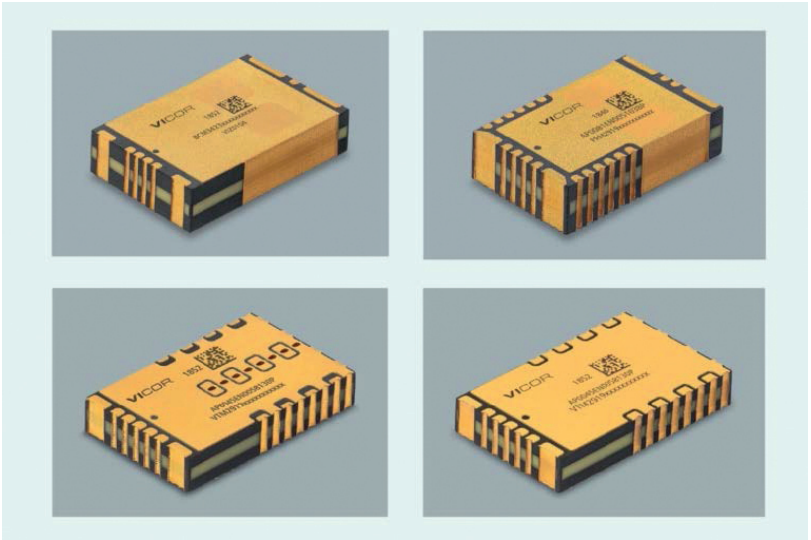

Figure 3: Vicor will offer these new BCM, PRM, and VTM rad-tolerant DC-DCs.

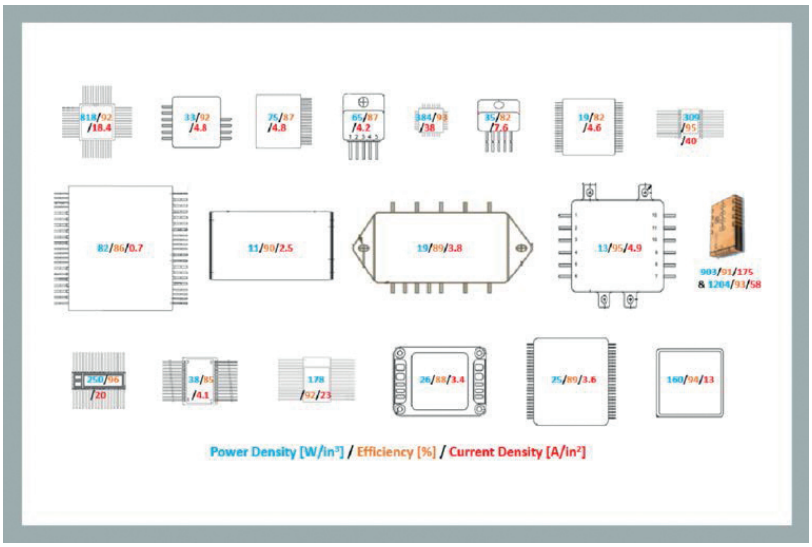

Figure 4: This diagram compares space-qualified switching POLs with the VTM2919 DC-DCs.

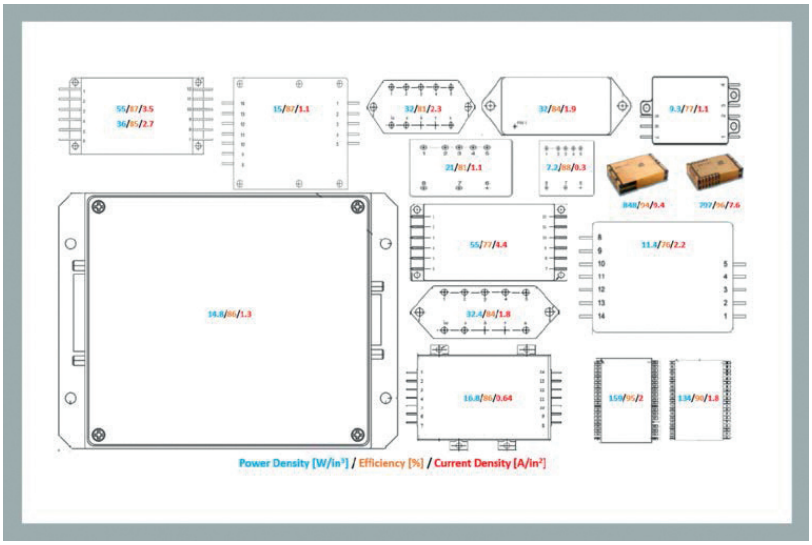

Figure 5: This diagram compares space-qualified isolated DC-DCs with the BCM and PRM DC-DCs.

ZVS/ZCS, SAC DC-DC (VTM2919P35K01A5S), which accepts a line voltage from 13.4 to 35V and outputs a fixed load voltage 1/32 of the input, ranging from 0.42 to 1.1V. Its maximum ambient efficiency is specified at 91% in a package size of 29.2×19.0×4.9mm weighing 13.3g.

The four DC-DCs have been designed using a redundant system architecture containing two identical parallel powertrains with fault tolerant control to meet single-event-effect (SEE) requirements. To reduce manufacturing costs, the parts have been packaged in a plated, epoxy-moulded resin BGA with excellent thermal conductivity, branded as **SMChiP™**, compatible with standard surface-mount, pick-and-place, and reflow assembly processes (Figure 3). The DC-DCs are EAR99, specified from –40 to 125°C and offer various overvoltage, short-circuit current, undervoltage, and thermal protection features. The target total-dose is 50kRad (Si) with SEE and other reliability data to be released later this year. Datasheets are available and bespoke input/output options can also be ordered.

To highlight the superior densities offered by the new rad-tolerant DCDCs, Figures 4 and 5 compare their relative sizes with existing space-grade switching POLs and isolated DCDCs respectively. The power density of each convertor in W/in³, its efficiency in % and current density in A/in², have been annotated in blue, orange, and red respectively. A range of efficiencies are typically specified for different load conditions and the maximum values from each datasheet are displayed below.

The new, rad-tolerant, COTS SAC DC-DCs are an innovative and enabling technology for NewSpace applications. When compared with existing qualified converters, they deliver major increases in output power, density, and efficiency in a smaller volume and lighter form-factor. Regulated voltages are significantly cleaner with less bulk decoupling. Parts will have heritage from next year and evaluation boards are available to help you de-risk future mission needs.

The FPA is a major advance to reduce the I2R distribution losses handicapping existing intermediate power architectures. A low-current, factorized bus allows much more freedom to place the BCM® and PRM away from the typically-congested load area.

A modular, 100V PDN solution now exists offering SWaP benefits to supply the latest, ultra-deep-submicron, space-grade semiconductors. The VTMs provide high-performing ratiometric DC-DCs and when combined with a PRM, enable a complete closed-loop FPA exploiting the efficiency advantages of a high-voltage factorized bus (Figure 6).

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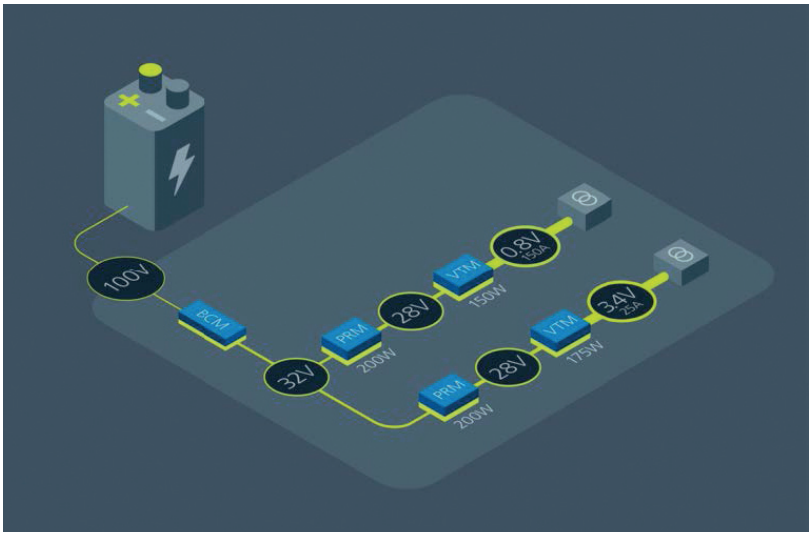


Figure 6: A modular 100V power-distribution solution now exists for spacecraft avionics.

How to Design a Thermally Balanced Current-Sharing System for Multi-Phase Power Designs

The car of tomorrow is envisioned to be an audiovisual wonderland on wheels, including wraparound screens and dozens of speakers. Driving on the road in the future will immerse passengers in an incredible sensory experience with content streamed via ultra-fast 5G. To achieve this content-rich, connectivity-heavy paradigm of future mobility, emerging digital cockpit systems continue to demand exponentially greater computing capability. These increasing computing requirements consequently result in a demand for higher power. This article proposes a novel, cost-effective approach to achieve a high-power, offline battery (12 V) power management stage that multi-phases two buck controllers.

Xavier Ribas, Applications Engineer, MPS, USA

As such, interleaved topologies are gaining popularity because they can supply higher load currents while improving EMC. However, engineers must optimize the balance between thermals, board size, and cost when designing these automotive power management systems. In particular, it is vital to achieve optimal current sharing between phases to avoid overheating the MOSFETs in one phase, as this can degrade the entire system. The proposed solution combines a simple yet elegant thermal-balancing circuit with two interleaved MPQ2908A-AEC1 devices, which are 4 V to 60 V input, current-mode, synchronous step-down controllers. This system effectively improves current sharing between phases while adeptly addressing the higher power dilemma.

Power stage

As the power demand of new automotive designs continues to rise, power electronic engineers face the challenge of designing circuits that can deliver more power without increasing PCB size and cost. In addition, these circuits must maintain low EMI below the regulated values.

Multi-phase topologies provide a simple solution to overcome this design challenge. In a multi-phase topology, multiple power converters are placed in parallel to increase the available load current of the entire power supply unit (PSU), which increases the amount of deliverable power. Moreover, if all of the converters run synchronously with each other but in different locked phases, then the EMI generated by the overall system is decreased. Lastly, the current demanded by the load is shared by all of the converters, which optimizes thermal behavior.

The automotive power management system presented in this article uses a dual-phase power supply that steps down the 48 V common in new automotive designs to the 12 V that is demanded by many advanced driver assistance systems (ADAS). To incorporate high 20 A load currents, this design uses two MPQ2908A-AEC1 devices. In addition to this controller's wide input range, which can step down from the 48 V specification, this device can be implemented in dual-phase topologies using its SYNCO pin, which outputs a 180° out-of-phase clock.

Figure 1 shows the system's block diagram for the original 240 W power stage. First, there is a 48 V car battery. Second, a system with reverse polarity protection and over-voltage protection (OVP) is added to protect the system from damage in the event of undesired events (e.g. incorrect cable connections). Lastly, an EMC filter reduces the conducted emissions, while the dual-phase interleaved buck converter steps down the voltage from 48 V to 12 V. Since the power managed by the system is quite high, a frequency spread spectrum (FSS)

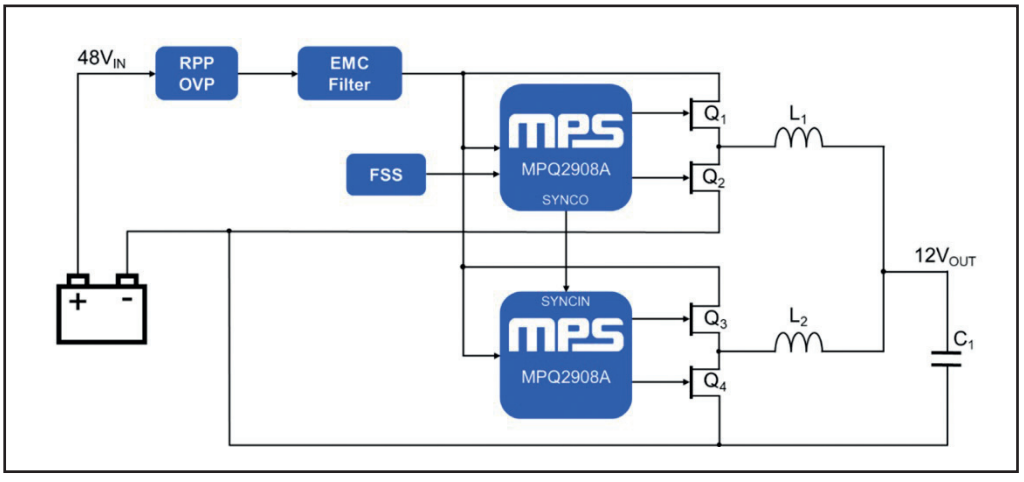


Figure 1: Original 240 W power stage

modulator is added to achieve low EMI in the overall system.

Design challenges and proposed solutions

Designers face two key design challenges due to the increasing power demands in the automotive sector. First, the power supplies for automotive applications must meet standardized EMC requirements, such as CISPR 25 Class 5. This means that the PCB layout should incorporate all EMC design recommendations. Furthermore, to ensure that this 240 W system can stay within the regulated EMC limits, certain complementary solutions are utilized (including an interleaved topology, EMC filter, and FSS modulator).

Designs must also manage board thermals. It is recommended to choose the appropriate circuit components to achieve high efficiency levels. By increasing efficiency, designers can reduce power loss, which minimizes temperature rise. In particular, designers should carefully select the MOSFETs and inductor(s) in their system. Figure 2 shows the efficiency of the original 240 W power stage at four different input voltages: 24 V, 36 V, 48 V, and 60 V.

There are other ways to improve the automotive power management system thermals beyond selecting optimal components. For example, the MPQ2908A-AEC1 allows the designer to select the converter's switching frequency (fSW). In general, f_{SW} should be as low as possible to reduce switching losses. A lower frequency increases efficiency while reducing thermal overheating for the board. For this example, with fSW set to 225 kHz, the higher EMI peak is placed at 450 kHz (2 x f_{SW}) to reduce the switching losses without impacting EMC.

Apart from the thermal and EMC constraints, interleaved topologies typically require excellent thermal distribution to equalize MOSFET degradation and prevent parts of the board from overheating. To overcome this thermal constraint, it is vital to select an appropriate PCB layout and optimize current sharing between the two controllers. With an optimal current-sharing scheme, the load current is equally distributed between all of the converters in the system. Therefore, all of the MOSFETs have the same thermal rise.

Consider a system without thermal balancing. For a system in steady state with a 20 A load current, there is a 1 A difference between the averaged current of each phase (denoted as the light blue and green traces in Figure 3). This results in an unbalanced temperature for both phases. If there is suboptimal thermal distribution between the phases (phase temperatures denoted as the dark blue and pink traces in Figure 3), then the hotter phase may experience faster degradation.

Thermal-balancing system

For this article, we designed a simple and easy circuit that equalizes the temperature for both phases via accurate temperature-sensing. This circuit is incorporated into the original 240 W system, then it senses and compares the temperatures of the two phases. As a result, the load current supplied by each converter can be changed accordingly (see Figure 4).

For example, if $T_1 > T_2$, the thermal-balancing system modifies phase 2's compensation signal to increase its output voltage (V_{OUT2}). Since the total output current is fixed by the load, the phase 2 current (I_{PHASE2}) increases while the phase 1 current (I_{PHASE1}) decreases. Thus, the power dissipation and temperature of phase 1 decreases until T_1 is equal to T_2.

Furthermore, this circuit reduces the BOM cost and minimizes the MOSFET and inductor size. If the current is shared unequally between the two phases, then the designer must use physically larger circuit components, such as the MOSFETs and inductor(s), to withstand the larger currents and power caused by current measurement tolerances. When current is

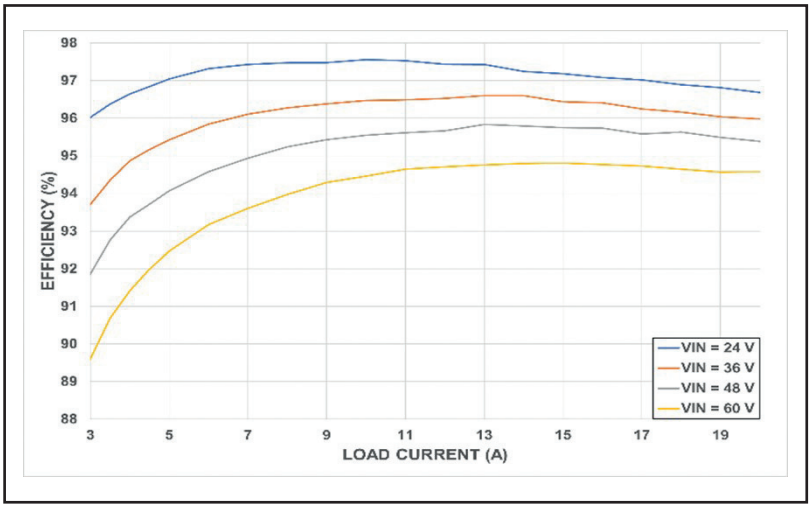


Figure 2: System efficiency

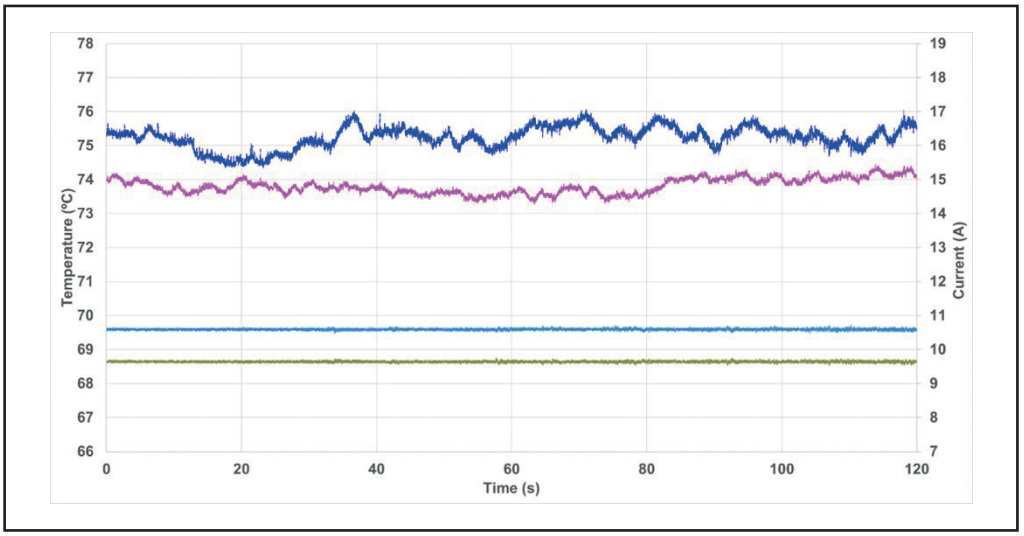


Figure 3: Current sharing without a thermal-balancing system

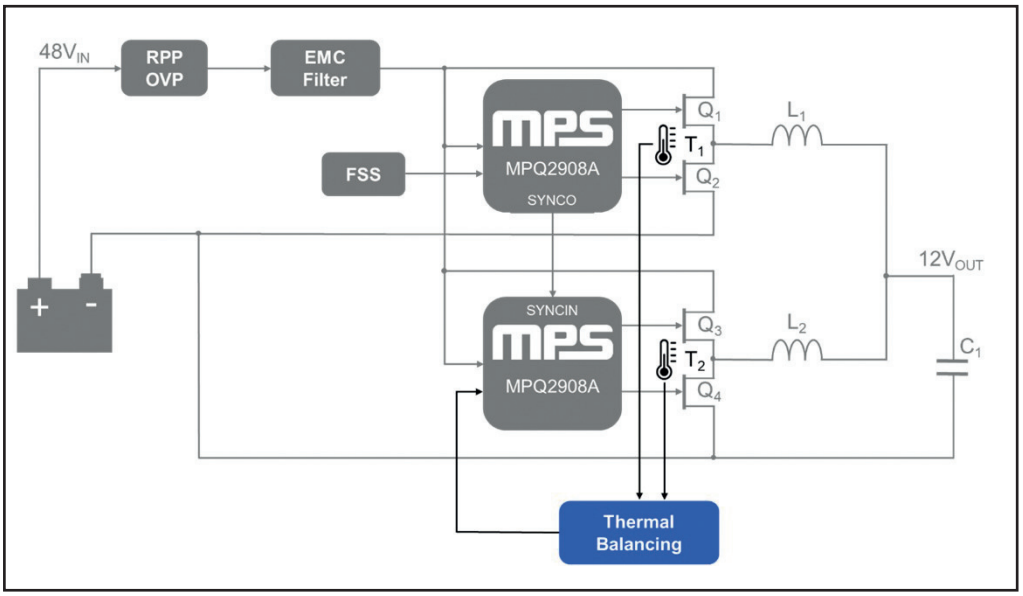


Figure 4: 240W Power stage with thermal-balancing system

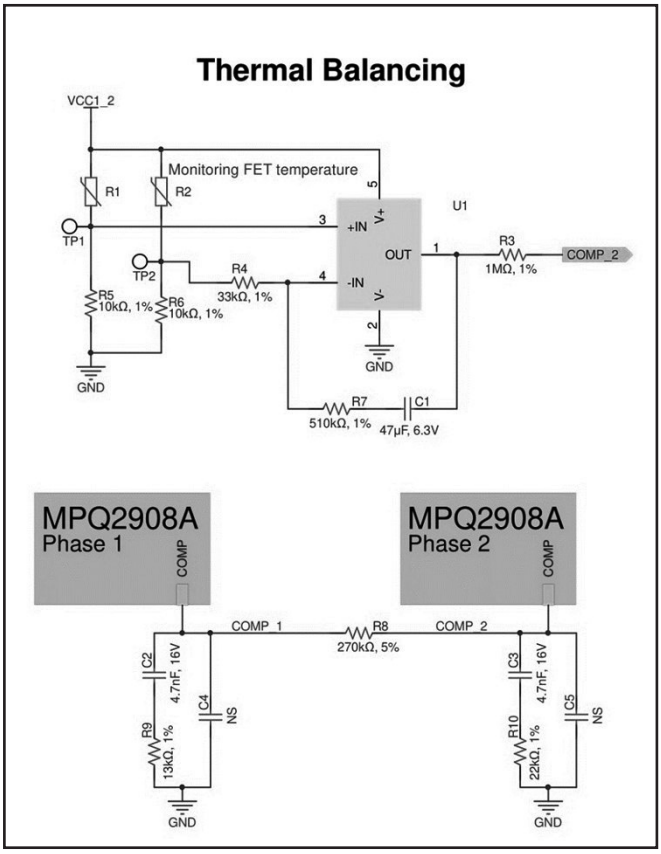


Figure 5: Thermal balancing schematic design

shared equally between phases, the design can be optimized for physically smaller MOSFETs and inductor(s), thereby reducing BOM cost.

In this circuit, the temperatures of the two phases are sensed via two negative temperature coefficient (NTC) thermistors. Then the temperature difference is fed to a proportional-integral (PI) control circuit that outputs a signal to phase 2's compensation (COMP) pin. If $T_2 < T_1$, then the voltage on phase 2's COMP pin increases along with the current (or vice versa if $T_2 > T_1$).

Phase 1 is not connected to the thermal-balancing circuit. The output current (I_{LOAD}) is the combination of both phase currents ($I_{PHASE1} + I_{PHASE2}$) and is set by the load, independent of the current distribution in the phases, as demonstrated with Equation (1):

$$I_{LOAD} = I_{PHASE1} + I_{PHASE2} \quad (1)$$

Because of this, if I_{PHASE2} decreases due to thermal balancing control, then automatically increases (and vice versa). As a result, phase 1 is influenced by the thermal-balancing circuit despite not being directly connected to it. Figure 5 shows the thermal balancing schematic design.

A resistor (R8) placed between phase 1 and phase 2's COMP pins ensures that that the current difference between the two phases does not reach critical or dangerous levels. The experimental results identified 270 kΩ as the optimal value for R8.

The simplified circuit only requires correctly sizing the PI circuit components to achieve temperature control. The PI's circuit transfer function (H(s)) can be calculated using Equation (2),

$$H(s) = \frac{V_{OUT}(s)}{V_{IN}(s)} = -\left(\frac{R_7}{R_4} + \frac{1}{R_4 \times C_1 \times s}\right) \quad (2)$$

where C1, R4, and R7 are the components of the PI compensation loop.

The proportional gain of the PI circuit (KP) can be calculated using Equation (3):

$$K_P = \frac{R_7}{R_4} \quad (3)$$

The integral gain of the PI circuit (KI) can be calculated using Equation (4):

$$K_I = \frac{1}{R_4 \times C_1} \quad (4)$$

Results

By using a thermal-balancing system, drastic improvements in current sharing and temperature equalization can be observed. Specifically, the temperature difference shown in Figure 3 (about 2°C) drops to less than 0.5°C (denoted as the dark blue and pink traces in Figure 6).

Conclusion

New automotive designs are adopting 48 V power management systems to reduce weight and power loss in the vehicle's

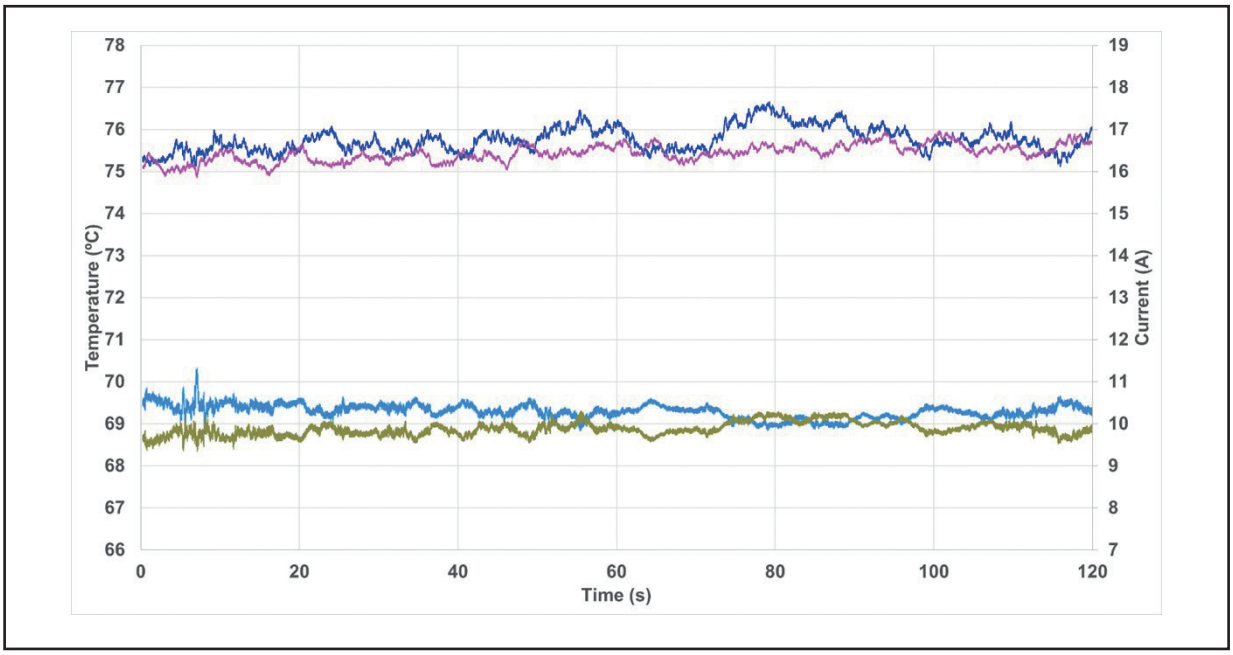


Figure 6: **Current sharing with a thermal-balancing system**

cable harnesses. Moreover, to withstand high loads, the use of interleaved topologies is important for the increase in required power.

When using interleaved topologies, excellent thermal distribution is necessary to balance the MOSFET degradation. This article presented a simple and easy thermal-balancing circuit combined with the MPQ2908A-AEC1, which improves current sharing and temperature distribution in multi-phase designs, and meets standardized EMC requirements, such as CISPR 25 Class 5. The temperature difference between the multi-phase converter phases can be effectively reduced from 2 K to 0.5 K using well-known and commonly used components.

Solving the Current Sensor Footprint Problem when Designing Compact EV Traction Inverters

Electric vehicles (EVs) are said to be the future of transport as the trend for electric mobility moves forward. This article is focused on the challenges of current sensing in high-power integrated traction inverters and highlights the benefits of using compact magnetic core-based sensors. **Sofiane Serbouh, Product Manager of Large Drives, LEM, Switzerland**

Globally, according to the International Energy Agency's Global EV Outlook 2022 report, the number of electric cars on roads by the end of 2021 was around 16.5 million and EV sales around the world in just the first five months of 2022 are reported to have exceeded 3.2 million.

Challenges of current sensing in high-power integrated traction inverters

Of course, with this increased popularity of EVs comes greater demand on their reliability, most notably their ability to be driven longer distances between charges. To achieve this, components such as high-power integrated traction inverters – which are essential to the vehicle's battery range and the whole driving experience – have needed to become as compact and efficient as possible. A traction inverter converts DC current from the EV's battery into AC current which powers the vehicle's propulsion system. Another of the inverter's functions is to capture energy from regenerative braking and send it back to the battery.

The solution to the requirement for high-power integrated traction inverters has been to develop reliable power module packages and take advantage of the ability to slash the footprint of such components as capacitors, inductors, transformers and filters using the benefit of Silicon Carbide MOSFETs to switch faster and increase battery voltage.

Engineers involved in the design of EV traction inverters understand that a key component is the current sensor and for it to meet the requirements of the e-mobility market it must offer a combination of high accuracy, affordability, high integration and the ability to operate in a demanding and rugged environment.

Integration of coreless current sensors in EV not yet mature

Coreless current sensors represent a promising solution for the future, because they will enable smaller and lower cost components to be used, but there are still many challenges with this technology before it can be widely adopted by the market.

For example, the strong variation of the magnetic field in space makes it necessary to place the coreless sensors on the busbar with high accuracy and with no option to move them following assembly and calibration. A tenth of a millimetre variation can quickly lead to a degree of error that is not acceptable in high-power traction inverters. Tolerances on assembly, mechanical handling, vibrations and thermal expansion are all potential causes of displacement. Together with the need to overcome skin effect to achieve high bandwidth, these factors mean that significant efforts in mechanical design need to be carried out in order to achieve reliable current measurement.

Furthermore, with traction inverters getting more compact, conductors are getting closer with a complex magnetic field distribution. Coreless sensors with their differential measurement are immune to homogeneous external fields but not to field gradient, which can introduce an extra degree of error in the measurements. Overall, significant constraints on the mechanical design to achieve the desired accuracy, combined with time-consuming calibration steps at the inverter level, reduce the attractiveness of the coreless sensor solution - for the moment.

Meeting the challenges with magnetic core current sensors

Until these technical barriers are overcome, fully calibrated current sensors with a magnetic core will remain the preferred means of achieving highly accurate current measurements in EV traction inverters. Not only does this technology have many years ahead of it but there is still massive potential for development and innovation in this area.

In operation, the magnetic core concentrates and amplifies the magnetic field to sense with a reduced output noise, while also shielding the measurement from external disturbing fields. As a result, there is a high signal-to-noise ratio (SNR) over a wide bandwidth. Also, reliable and stable measurement is made possible even under tough vibration scenarios due to the tightly controlled assembly and calibration of the magnetic core, the Hall-effect based ASIC and the busbar.

The problem is that open loop core-based sensors tend to be bulky and present challenges in terms of integration at inverter level. That's why LEM has focused on developing compact and affordable current sensors with magnetic cores, to offer reliable current

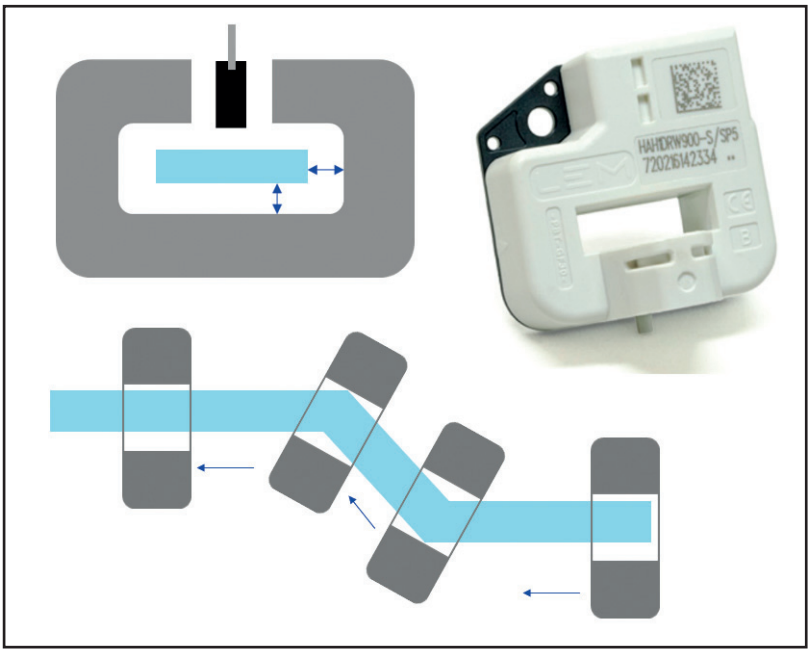


Figure 1: **HSTDR single-phase current sensor with integrated busbar**

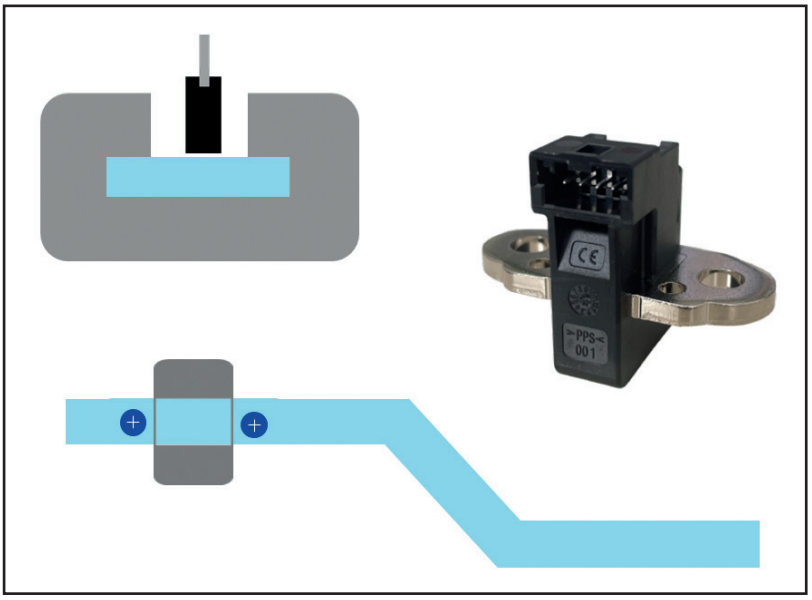


Figure 2: **HSTDR single-phase current sensor for 1500 A that incorporates core, busbar and sensing element in a single package**

measurement over the widest range of applications. The sensors are part of the company's portfolio that are designed specifically for use with EV traction inverters. This allows customers to select highly reliable off-the-shelf products for their inverter requirements which enables EV component manufacturers to achieve a rapid time-to-market turnaround.

When looking at solving customers' problems that existing current sensors could not tackle, the R&D department at LEM came up with a solution in the form of the HSTDR single-phase current sensor with integrated busbar, that is considerably smaller than any traditional current sensor with an opening hole. Designed for DC-Link voltage measurement and 3-phase current measurement, but also for DC/DC converters, the HSTDR's small footprint offers a greater flexibility to designers working within the constrained space availability of a traction inverter box. The HSTDR also offers protection against external fields and high SNR thanks to its magnetic core with a small air gap (Figures 1 and 2).

Busbars tend to be isolated from the magnetic core in traditional designs but LEM's approach of having the core located directly on the busbar, which has a restriction, means the core can be much more compact. Typical current sensors with an opening hole tend to require a large aperture for sliding on to busbars that can be of a complicated design (resulting in a large sensor), whereas there are no limitations on where to fit sensors with integrated busbars. This makes it possible to minimize the aperture of the magnetic core – and therefore reduce the overall size of the core by up to 40 % – while increasing the current measuring range by 60 % compared to the previous generation HSNDR. This again offers superior flexibility to EV component designers because the sensor is capable of being

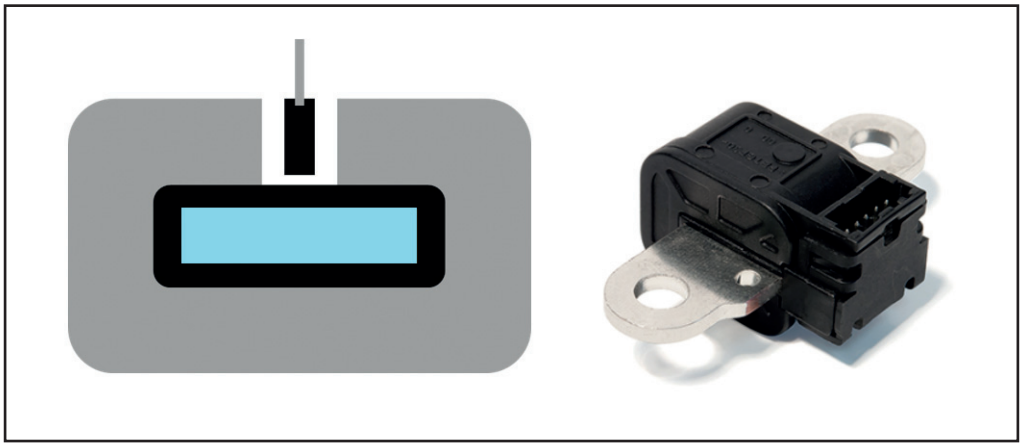


Figure 3: **HSTDR 1000 A single-phase current sensor**

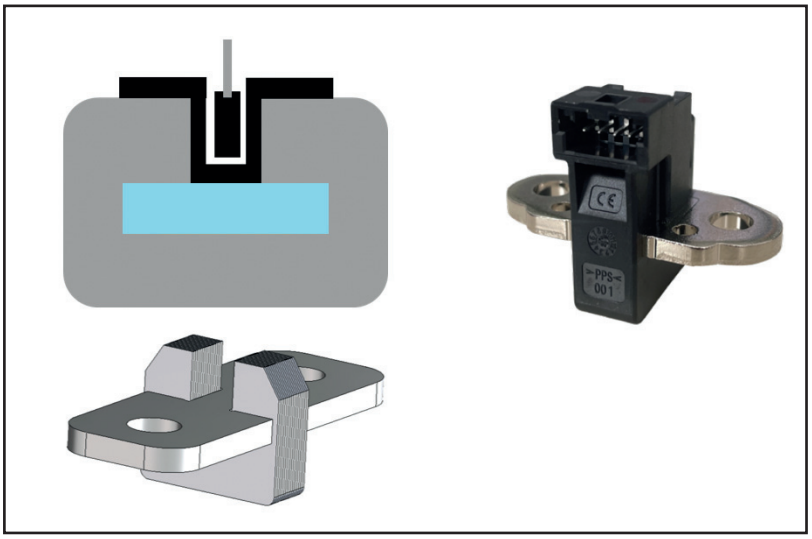


Figure 4: **HSTDR 1500 A single-phase current sensor including restrictions**

placed anywhere in the traction inverter.

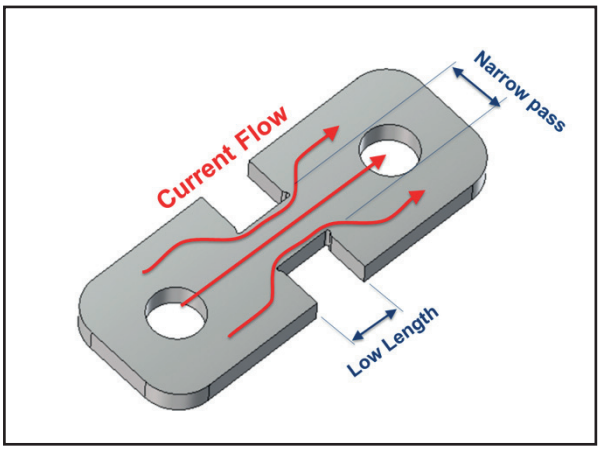
Of course, a smaller magnetic core also means that the overall weight of the sensor can be reduced by around 50 %. As a consequence, the sensor can handle vibrations of up to 10 g, which is now a standard requirement in automotive environments. Another benefit of a smaller magnetic core is that it reduces the amount of raw materials required in the sensor build, keeping costs down. Also, there are considerable time-saving and productivity advantages associated with having a fully calibrated sensor that incorporates core, busbar and sensing element in a single package (see Figure 3 and 4).

Key design considerations for the new sensor

When LEM's engineers designed the HSTDR single-phase current sensor with the EV traction inverter market firmly in mind, they had three key considerations.

Firstly, the restriction mentioned earlier on the integrated busbar should be large enough to ensure mechanical stability while preventing additional power loss and heat dissipation in an already extremely hot environment. As a result, resistance introduced by the restriction on the busbar is negligible at no more than 20 µΩ (see Figure 5). Secondly, with the magnetic core directly mounted on the busbar, it was important to design an isolation barrier between the electronic and the magnetic core, to ensure enough clearance and creepage distance for 800V battery systems. Finally, it was important that – because the sensor would be operating in harsh and noisy environments – its output would remain immune to high switching speeds (dV/dt) – see Figure 6.

One other point of note is that, in terms of accuracy, the HSTDR current sensor delivers a global error over temperature and lifetime of less than 3.5 % over a dynamic range up to 1500 A. Also, because the unit offers consistent performance over a range of frequency levels with minimal part-to-part phase shift dispersion, it is capable of ensuring accurate torque control which is an essential factor in EV motor drive applications.

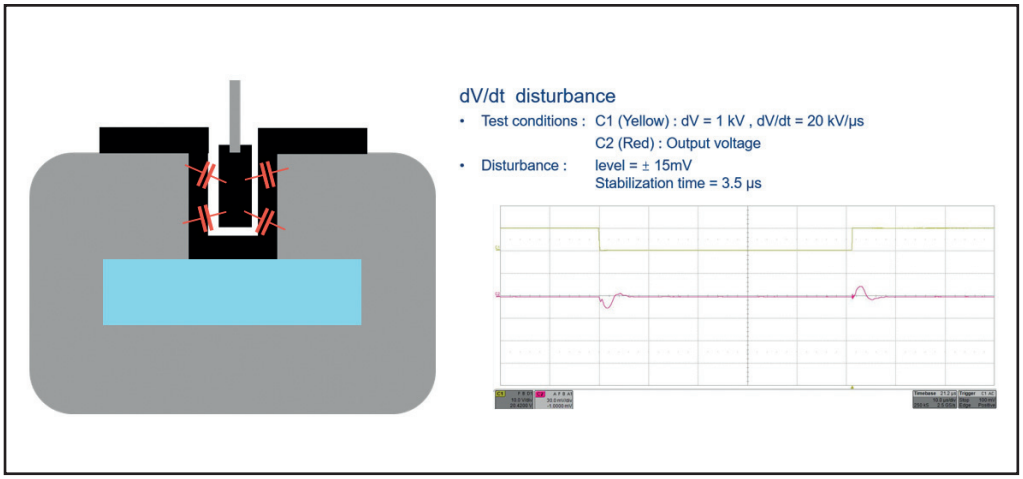


LEFT Figure 5: **HSTDR busbar restrictions**

Conclusions

Having produced its first current sensor for battery monitoring systems over 20 years ago, LEM is no newcomer to the automotive market and the company is continually developing innovative new products for this demanding sector. LEM has built up an extensive portfolio of such products as sensors for use in traction inverters, DC/DC converters and on-board chargers, with the aim always to go smaller and smarter wherever possible. The company focuses on solving customers' problems by exploring today's technologies to take them further as well as developing tomorrow's solutions by foreseeing future challenges and working to address them.

RIGHT Figure 6: **HSTDR immunity to high switching speeds (dV/dt)**



Finding the Right Technology to Solve Datacenter Power Challenges

Although Silicon (Si) is the most familiar technology, its smaller bandgap limits operating temperature, its low breakdown electric field restricts its use to lower voltages, and its low thermal conductivity limits power density compared to wide bandgap (WBG) materials, like gallium nitride (GaN) and Silicon Carbide (SiC). Digitization and the rapid deployment of cloud services have boosted the growth of datacenters worldwide. WBG helps to reduce their power consumption. **Anuj Narain, Director Power Platforms and Applications, Wolfspeed, USA**

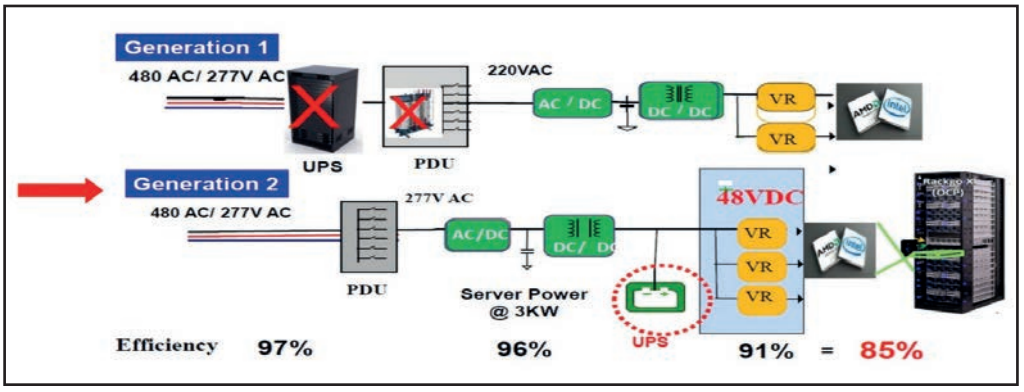
Datacenters consume close to one percent of global electricity, a number that is only expected to grow. Industry trends, such as metaverse and augmented and virtual reality, will continue to demand more energy than the planet can sustainably produce. While increasing renewable energy contribution is a step in the right direction, it is not enough, and energy efficiency is another area of focus that targets the nearly 40 percent of datacenter operational costs due to energy consumption by servers and their cooling systems (Figure 1).

Global standards for datacenter power supplies also continue to evolve toward higher efficiencies. The Open Compute Project (OCP) 3.0 offers further optimization of hardware that lowers energy consumption, and the 80 Plus Platinum and Titanium certification requirements as well as EU's Ecodesign in Europe (ErP) Lot 9 regulations continue to evolve (Table 1). The next update to Lot 9 is already scheduled for January 2026.

Power architecture evolution

As processor and server power is increasing, datacenters are using more power per rack. They now need 2-4 kW discreet blocks with the industry trending toward even higher power densities. Distributing this power at the first-generation 12 V levels means having to handle much higher currents. To provide 1 kW to a server rack, the traditional 12-V architecture needs to deliver 83 A of current. To control I?R losses and address safety concerns, more copper would be needed in the wiring harness of such a system.

A one-percent efficiency improvement can result in saving kilowatts at datacenter level and second-generation power architectures, using 48 V (Figure 1), result in 16-times lower I?R losses while still being below the UL-60950-1 standard 60 V DC Safety Extra – Low Voltage (SELV) limit beyond which additional insulation, spacing, and testing are required. To meet new energy efficiency requirements, the



LEFT Figure 1: Global energy savings from Gen2 power architectures can be equivalent to 27 1-GW nuclear power plants (Source: Fred Lee, Power Architecture for the Next Generation of Datacenter)

		Efficiency				Power Factor				80Plus	
Requirement	Output/ Load	10%	20%	50%	100%	10%	20%	50%	100%	230 V non-redundant	230 V redundant
Lot 9 (March 2020)	Multi	—	88%	92%	88%	—	—	0.90	—	Gold	Gold
	Single	—	90%	94%	91%	—	—	0.95	—	Platinum*	Platinum
Lot 9 (Jan. 2023)	Multi	—	90%	94%	91%	—	—	0.95	—	Platinum*	Platinum
	Single	90%	94%	96%	91%	—	—	0.95	—	Titanium	Titanium

Table 1: Lot9 and 80Plus have similar requirements with 80Plus Titanium applications demanding a greater 98.5 percent PFC efficiency

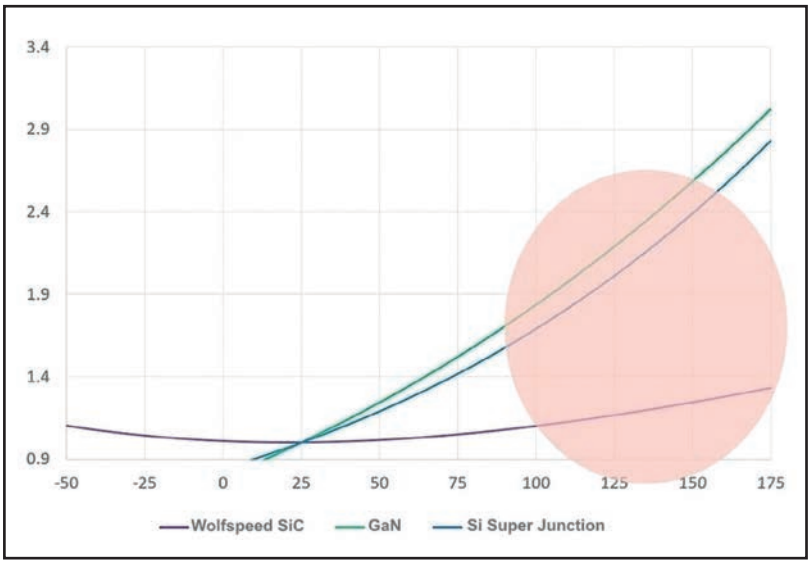


Figure 2: Generic chart showing typical MOSFET $R_{DS(ON)}$ (normalized) change over temperature

enterprise datacenter power sector is therefore adopting a 48 V architecture.

Generation 2 rack systems, built out as discrete 2-4 kW power blocks, replace the massive high-voltage Uninterruptible Power Supply (UPS) and Power Distribution Units (PDUs) from Generation 1 with smaller UPSs per rack that are charged using a 48 V DC supply. The AC/DC and DC/DC supplies not only operate each server board but charge the UPS battery. The removal of load sharing and redundancy from Generation 1 leads to the requirement for each power supply to operate at close to full (100 %) load.

Challenges to server PSUs

Apart from the challenges due to the changes discussed above, it is worth noting that the OCP 3.0, Open Rack V.2 (ORV) and Bitcoin/mining power supply units (PSUs) require a move beyond 2 kW to the 3-4 kW range. Rack manufacturers continue to call for small form factors and low profiles of 40 mm (height), high power density, effective and low-cost thermal management, and EMI design to manage the high-speed switching that reduces size of the magnetics. In addition, there is requirement for full digital control and design flexibility from using power MOSFETs mounted on a daughter card.

In considering semiconductor device technologies to solve these challenges, differences must be noted in terms of bandgap, critical electrical breakdown, electron mobility, and thermal conductivity, all of which affect the peak operating temperature, voltage, efficiency, and thermal management requirements of the system.

The semiconductor solution

Although Silicon is the most familiar technology, its smaller bandgap limits operating temperature, its low breakdown electric field restricts its use to lower voltages, and its low thermal conductivity limits power density compared to wide bandgap materials, like gallium nitride (GaN) and Silicon Carbide (SiC).

For the efficiencies needed in datacenter power supplies, it is important to compare switching and onduction losses. Conduction loss, which is the device's I2R loss, is lower when the ON drain-to-source resistance ($R_{DS(ON)}$) is low and changes less with temperature.

Figure 2 shows normalized $R_{DS(ON)}$ plotted against temperature for the technologies that many designers consider using to meet Gen2 datacenter PSU requirements — SiC, GaN, and Si Super Junction (SJ). It is interesting to note that both GaN and SJ devices boast a lower $R_{DS(ON)}$ below 25°C, which are temperatures not quite practical for datacenter power supplies. As datasheets for GaN and SJ devices often specify $R_{DS(ON)}$ at 25°C, it can mislead engineers into assuming that specification at the much higher operating temperatures for which systems are normally designed.

Another interesting characteristic to note in Figure 2 is the change in $R_{DS(ON)}$ over temperature. SiC's curve remains nearly flat, and although the other technologies both show a significant increase in $R_{DS(ON)}$, this change is particularly dramatic for GaN. Since designers have to use $R_{DS(ON)}$ at real-world junction temperatures of 120°C to 140°C, a 60-mΩ SiC device would be 80-mΩ "hot," while a 40-mΩ Si SJ or GaN device would really be significantly >80-mΩ hot.

GaN's low switching loss vs low total loss

GaN's high electron mobility is the property that enables its well-known and unmatched efficiency at very high switching frequencies. Among the technologies discussed here, GaN offers the lowest switching loss (Figure 3).

Wolfspeed compared their 60-mΩ SiC device with a 50-mΩ GaN device in a totem pole PFC simulation to find that although GaN had slightly lower switching losses over the entire power range, any gains were offset by the increased

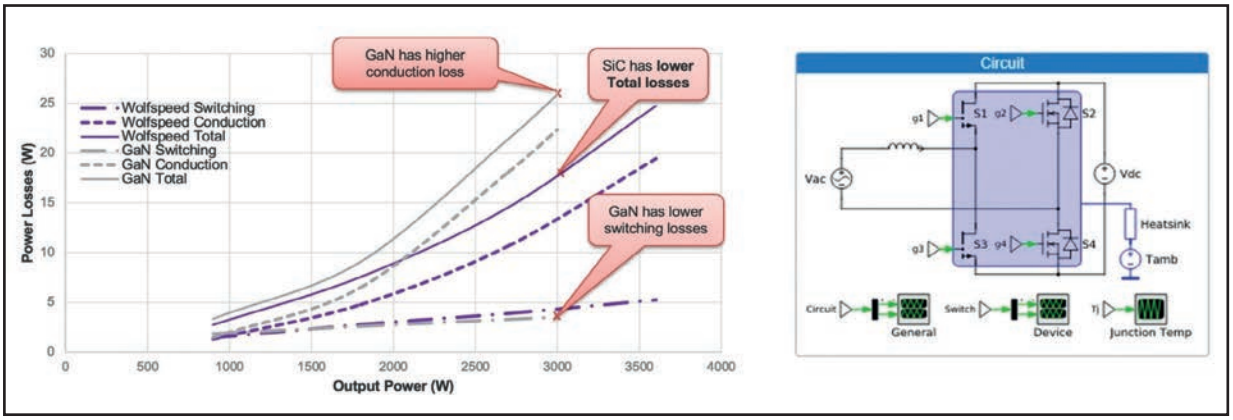


Figure 3: A study comparing a Wolfspeed 60-mΩ Silicon Carbide with a 50-mΩ GaN device in a totempole PFC simulation (power loss vs output power left, circuit right)

conduction losses with power and consequently junction temperature increase. This requires GaN devices to be made oversized to compensate for higher conduction losses regardless of switching frequency.

The GaN testing had to be stopped at 3 kW due to power limitations of the device. The study clearly demonstrated that SiC results in significantly lower total losses, especially at the high power levels at which WBG semiconductor use is most compelling, such in as datacenters. The various device-level performance specs of the three semiconductor technologies are compared in the radar chart in Figure 4.

At first glance, we notice GaN's benefits are the lowest reverse recovery charge Q_{rr} for the lowest switching loss in continuous conduction mode (CCM) synchronized rectifier, the lowest time-related output capacitance $C_{oss(tr)}$ for low dead time, and high frequency and efficiency, and the lowest energy-related output capacitance $C_{oss(er)}$ for minimum switching loss in hard-switched topologies. Notice that SiC trails close behind GaN in these attributes, while Si lags significantly.

Silicon wins include the lowest junction-to-case thermal resistance R_{thjc}, which confers better thermal performance, and the highest threshold voltage V_{th}, which offers better immunity to noise and makes Si devices easier to drive. Note that GaN has an extremely low V_{th}.

The maximum junction T_{jmax} and the avalanche energy, single pulse E_{as} indicate device robustness. SiC is the most robust as shown, while GaN has no E_{as} capability. SiC also has the lowest $R_{DS(ON)}$ change over temperature, which results in low conduction loss at high temperature. This is where GaN lags considerably to undo all gains from low switching loss.

Put together, SiC's strengths help deliver the highest efficiency at higher power levels, as well as high power densities required for enterprise datacenters and similarly demanding applications.

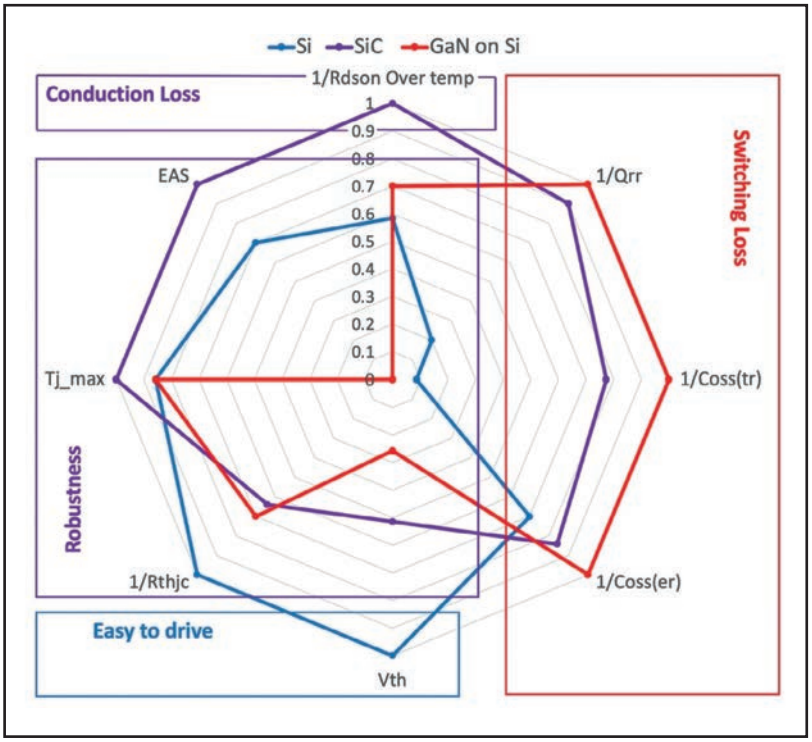


Figure 4: Silicon Carbide excels in high-voltage, high-power and high-temperature applications, such as datacenter power supplies

The package point of view

Since Wolfspeed developed the SiC technology for a successful transition from Si, many of the common surface-mount and through-hole packages are available for SiC products. GaN, on the other hand, faces unique challenges toward package standardization.

For instance, GaN through-hole packaging is uncommon because products need to have lower parasitics and allow very-high-frequency switching to best utilize the material's strengths. GaN is often either offered in large QFN or custom packages. Large QFN suffers from board-level reliability concerns and custom packages lack multisource availability as well as tooling capability at subcontractors.

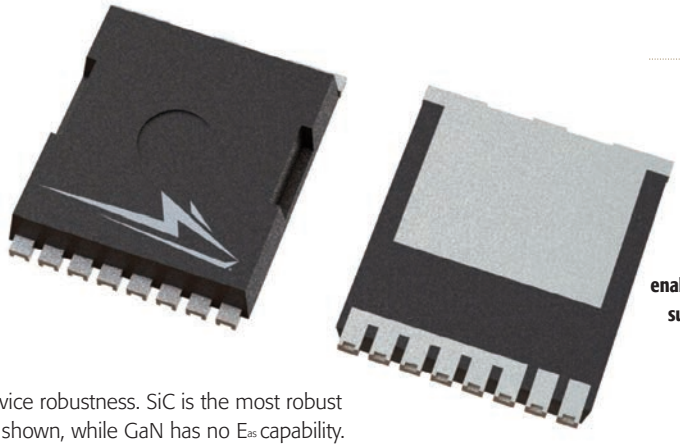


Figure 5: The TOLL package is significantly smaller than the standard TO-263 and enables low-cost surface-mount assembly

GaN's power device package challenges do not end here. Other common concerns include:

- Kelvin source pins, widely adopted in SiC for better switching control, are not feasible in cascode GaN since other internal parameters like the cascode FET and capacitances go unaccounted. The common source cannot be eliminated and the cascode GaN is limited to TO-247-3 (three-lead) package in which the vulnerability to gate oscillation limits switching speeds.

Some custom packages on the market are so thin, they constrain the space available for a heatsink.

- Another custom package on the market has a top-side cooled drain, which requires thermal interface materials (TIMs) with high thermal conductivity to extract heat away from the device.
- Yet another TO-Leadless (TOLL) package for GaN places the gate and the Kelvin source in a direction different from standard Si, which makes transition from the latter technology cumbersome.

As the market moves towards high-power density design and tighter space constraints, the TO-Leadless (TOLL) package offers advantages of low height and smaller footprint, and its leadless form results in low lead inductances that would otherwise become a concern in high frequency operation. The package's larger drain tab area addresses thermal performance concerns from small packages (Figure 5).

TOLL is a relatively new package for the datacenter and server power supply market. Wolfspeed is, however, supporting that market with product development in this direction, such as with new TOLL package variants for datacenter and server power.

A system-level comparison

Compared with Si-based H-bridge, SiC-

Figure 6: Silicon Carbide is the best choice in a totem pole PFC, especially for high reliability applications

	# PFC Choke	# Power Semiconductor	Power Density	Peak Efficiency	Cost	# Control	# Gate Drive
SiC CCM Totem Pole Semi-BL PFC	1	4	Highest	98.8%	Medium	2	2
SiC CCM Totem Pole bridgeless PFC	1	4	Highest	99.1%	High	3	3
GaN CCM Totem Pole Semi-BL PFC	1	4	Highest	98.8%	High	2	3
GaN CCM Totem Pole bridgeless PFC	1	4	Highest	99.2%	Highest	3	4
GaN CRM Totem Pole bridgeless PFC	2	6	Medium	99.1%	Highest	4	5

Table 2: Topology and component analysis of Silicon Carbide- and GaN-based bridgeless PFCs

based CCM totem pole PFC can have not only higher efficiency but higher power density at similar or lower cost. A comparison of efficiency between technologies clearly shows that while both SiC- and GaN-based CCM totem pole PFCs can achieve >99 % efficiency, GaN has the efficiency advantage only at very light loads. As discussed earlier, GaN's much higher $R_{DS(ON)}$ change over temperature (Figure 2) results in its dramatically drooping efficiency curve at higher power/loads. In applications, like datacenters, that operate at or near full load 24/7, GaN therefore fails to meet efficiency requirements. SiC, on the other hand, provides an efficiency similar to that of GaN at half load and better efficiency at full load (Figure 6).

Taking a broader look to include power density, the number of components, and relative cost of SiC- and GaN-based CCM totem pole PFC (Table 2), it is noted that SiC is better than GaN not only in terms of efficiency in high-power density applications, but also in terms of gate drive complexity, control, and cost.

In yet another comparison of real-word WBG demonstrator designs from various companies, Wolfspeed SiC shows clear advantages (Table 3). Some key points to note are:

- Many of the existing reference designs require impractical thermal management and restrict design flexibility.
- GaN FET-based totem-pole designs have lower efficiency at full load due to the high temperature coefficient of $R_{DS(ON)}$.
- As expected, SiC's low temperature coefficient of $R_{DS(ON)}$ results Wolfspeed's design to exhibit a nearly flat efficiency curve from half load to full load.
- While SiC and GaN meet requirements for bridgeless PFCs in the 2-4 kW range, high conduction losses make GaN thermal design challenging beyond 4 kW.
- System frequencies of the reference designs are limited to the 45-47 kHz and

	Peak Efficiency	Full-Load Efficiency	HF Switch	LF Switch	Height (mm)	Power Density (W/in³)	Efficiency Standard	Physical Standard	Comments
Company A 2.6kW	99.14%	98.70%	GS66516B 32mΩ **GaN**	IXFH60N65X2	40	78	80+ Titanium/ ErP Lot9	None	SMD GaN
Company B 2.5kW	99.2%	98.50%	IGO60R070D1 70mΩ **GaN**	IPT65R033G7	45	/	80+ Titanium/ ErP Lot9	None	eGaN, limited to 2.5kW by 70mΩ
Company B 3kW	98.9% (50% load)	98.5%	IMZA65R048M1H 65mΩ 650V **SiC**	IPW60R017C7 (SJ MOS)	40	32	80+ Titanium/ ErP Lot9	OCPv3	PFC SiC primary & Si secondary, LLC Si. No daughter card.
Company C 4kW	99%	98.55%	GAN041-650WSA 41mΩ **GaN**	STY139N65M5	50	/	80+ Titanium/ ErP Lot9	None	Cascode GaN
Company D 3.6kW	97.7%	97.10%	SCTW35N65G2V 55mΩ **GaN**	TN3050H-12GY	57	/	80+ Titanium/ ErP Lot9	None	SiC, SCR, low efficiency
Company E 4kW	98.73%	98.57%	LMG3410R050 50mΩ **GaN**	STY139N65M5	35	**123**	80+ Titanium/ ErP Lot9	None	GaN, interleaved, switching at 115 kHz (in CE band)
Company F 3.3kW	99%	98.55%	TP65H050WS 50mΩ **GaN**	STY139N65M5	50	/	/	None	Cascode GaN
Wolfspeed 2.2kW	98.79%	98.68%	C3M0060065J/K 60mΩ **SiC**	FRED diode	64	20	80+ Titanium/ ErP Lot9	None	SiC, no SR
Wolfspeed 3.6kW	>99% (50% load)	>98.5%	C3M0045065L 45mΩ **SiC** TOLL	VS30CDU06H M3 (diode)	40	**92**	80+ Titanium/ ErP Lot9	OCPv3	SiC primary with SR option, daughter card concept

Table 3: A competitive analysis of wide bandgap reference designs on the market

RIGHT Table 4: **Efficiency and cost comparison of four- and two-MOSFET options available for Wolfspeed's 3.6 kW design**

	4 x MOSFETs	2 x MOSFETs in HF leg + 2 x Diodes in LF leg
MOSFET cost %	55.6%	27.8%
Diode cost %	0.0%	8.7%
Gate drive cost %	37.0%	18.5%
PCB, Heatsink	3.7%	3.7%
Assembly cost	3.7%	3.7%
Efficiency @ 50%	99.1%	98.6%
Efficiency @ 100%	98.9%	98.5%
Total cost %	100.0%	62.4%

60-67 kHz ranges to keep harmonics under 150 kHz for CE's EMI requirements. This negates GaN's advantage from low switching losses.

Wolfspeed's 3.6 kW solution

Wolfspeed's new 3.6 kW totem-pole PFC reference design (Table 3, last row) is aimed at solving the datacenter and server power supply challenge with >99% efficiency at half load and >98.5% full load, achieving 80 Plus Titanium and ErP Lot 9 requirements.

The design also offers the flexibility to tradeoff some of the high efficiency for lower cost, while still meeting the efficiency standards mentioned above (Table 4). The lower cost option replaces two of the MOSFETs in the low-frequency (LF) leg of the design with diodes, while retaining them in the high-frequency (HF) leg.

A two-daughter-card design concept gives customers the flexibility to choose the right option depending on their system design priorities. In developing such solutions, Wolfspeed uses its experience building a broad portfolio of the most field-tested SiC and GaN on SiC solutions on the market.

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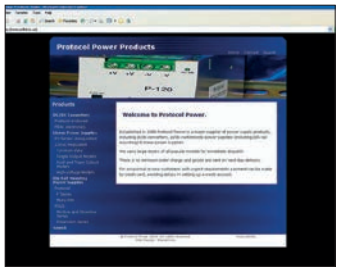

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