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SILICON CARBIDE

Practical Use of SiC Power Semiconductors

THE EUROPEAN JOURNAL FOR POWER ELECTRONICS AND TECHNOLOGY

Also inside this issue

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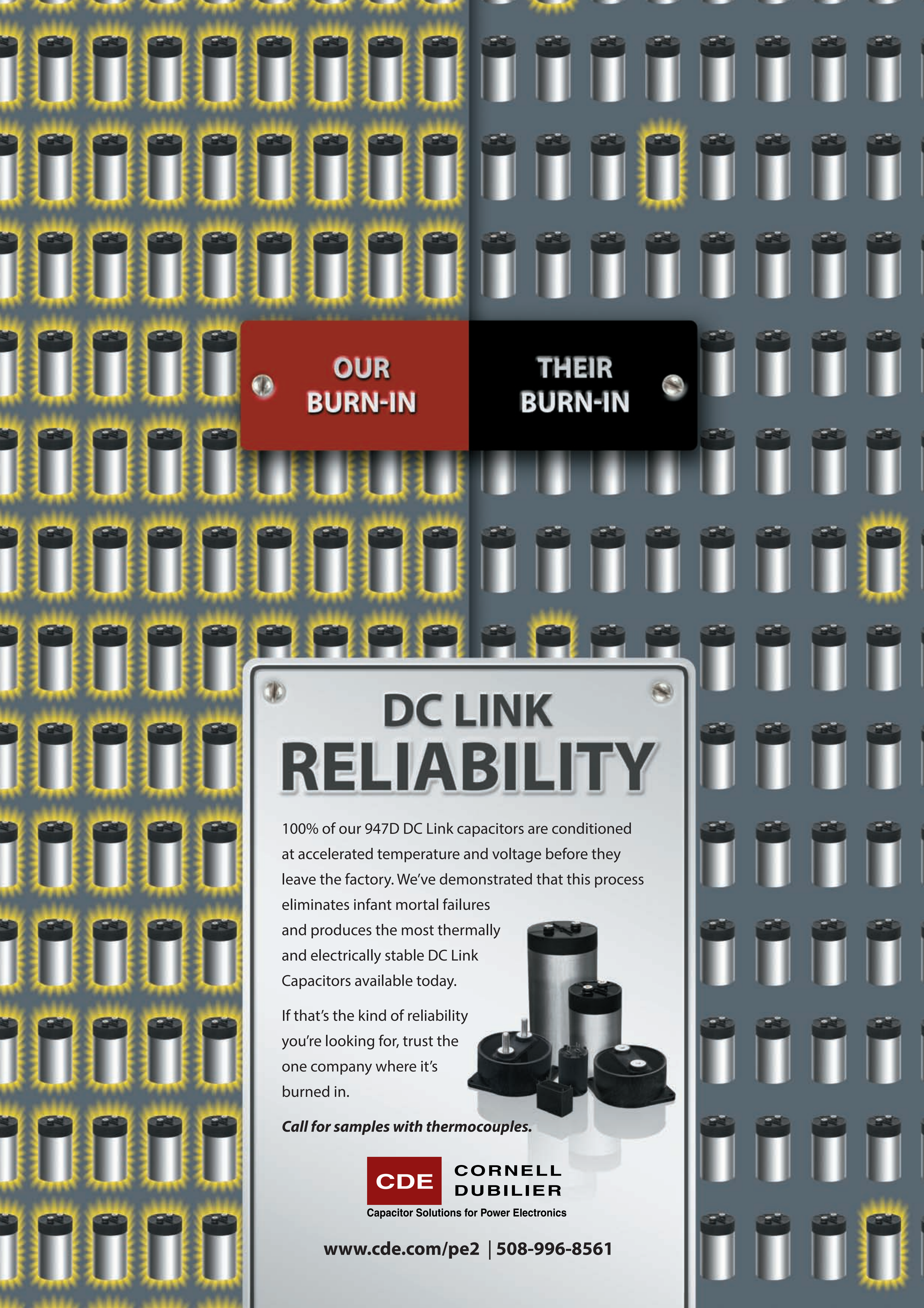
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The Year of SiC and GaN

According to the crystal ball of market researchers such as IHS, the emerging market for Silicon Carbide (SiC) and Gallium Nitride (GaN) power semiconductors is forecast to grow at a remarkable factor of 18 up to $2.8 billion during the years 2012 to 2022, energized by demand from power supplies, photovoltaic (PV) inverters and industrial motor drives. Thus market revenue is expected to rise by double digits annually.

SiC power devices are enabling components mainly in the context of higher switching frequencies and/or small footprints in power electronics. However, this trend imposes new challenges on the packaging of the chips. Typical stray elements like inductances become crucial elements in the circuit. In addition, different considerations regarding the thermal design in power modules arise when SiC chips are taken into consideration. Furthermore, the aspects of power density as well as the general utilization of SiC's high temperature capability are important factors in reliable implementation of SiC-based power semiconductors in modern systems. Our cover story will give an insight into how these boundary conditions can be implemented in innovative solutions using SiC chips. SiC power technology, predominantly in form of Schottky diodes, is meanwhile established in the market. High-power solutions using power-module technologies have recently become available. Usually, the aim of such components is to enable system benefits, for example by increasing the switching frequency or reducing losses. If this is successful, the high cost of SiC-based components can be compensated by reduced efforts for passive elements and/or cooling.

While the discrete, unipolar SiC devices as single chips are more or less ready to achieve higher frequencies (>100 kHz in PFC units), this is still a challenge for power modules. Solutions in a power range with traditional modules have high stray inductances and thus the di/dt is increased if combined with an increase in the frequency. A plug and play between SiC and Silicon at chip level in existing modules could devaluate the theoretical SiC performance. Thus it is necessary to improve high-current modules in order to get the full benefit of SiC in the frequency range above 20 kHz. Whilst the reduction of parasitic elements in power modules using SiC chips is in line with the approach also used for future Silicon solutions, it might happen that different optimization criteria will apply for the thermal design. The reason for this is that the cost contribution of chips in a power module with SiC is different from one with Silicon. Thus, the best solution for a given frame size with respect to semiconductor area placed in the module could be different. Furthermore, it is expected that the die size of a SiC transistor at 1200 V, for example, comes down to one tenth or less of the area needed in the current Silicon-based IGBT technology, assuming the same total losses for both options. This will result in a huge increase in power and current density, and will require more efforts with respect to an effective heat removal and the connection of chips to terminals.

Also Richardson RFPD, an Arrow company focuses on SiC and has launched its SiC Tech Hub, a micro-website featuring the latest news and new product releases related to Silicon Carbide technology. The company has an extensive SiC offering, including a selection of of Schottky diodes, MOSFETs and IGBTs from industry-leading manufacturers Cree, Microsemi, Vincotech and Powerex. The SiC Tech Hub brings together these products with design resources. The wide range of design resources offered on the SiC Tech Hub includes application notes, brochures, datasheets, presentations, selector guides, supplier documentation, technical articles and videos. Visitors to the SiC Tech Hub may also sign-up for emailed product updates, links to technical presentation videos, and other resources like white papers and technical articles as soon as they are published.

But the most interesting news comes with the GaN merger of US-based Transphorm and Japan-based Fujitsu Semiconductors. Device manufacturers such as International Rectifier, GaN Systems, Panasonic, or Transphorm are competing to commercialize GaN power devices. Transphorm has already released high voltage commercial GaN devices, the company continues to make significant improvements in performance, quality and productivity. Given this, Fujitsu, Fujitsu Semiconductor and Transphorm will bring together their complementary strengths in technology and manufacturing. Integrating Transphorm's operations with Fujitsu will enable high-volume and high-performance GaN power device production at Aizu-Wakamatsu plant in Japan. In addition to being a future user for GaN devices, Fujitsu has also built customer relationships with many power management companies in Japan, one of the most important markets for GaN. Recently power supply manufacturer Delta Electronics has committed its interest in GaN power.

Conferences/exhibitions will focus on these subjects in 2014. First will be CIPS 2014 in Nuremberg, here Daisuke Ueda, Advanced Technology Research Laboratories, Panasonic, Japan, will give a keynote on "Present and Future of GaN Power Devices". At APEC 2014 a dedicated Rap-Session will give an answer to the question "Will GaN and SiC devices become a higher value proposition for design engineers and enter mainstream adoption displacing Silicon power semiconductors in new designs and applications?" And at PCIM Europe 2014 PEE will host a panel discussion on "Si vs SiC/GaN - Competition or Coexistence".

Interesting events to come!

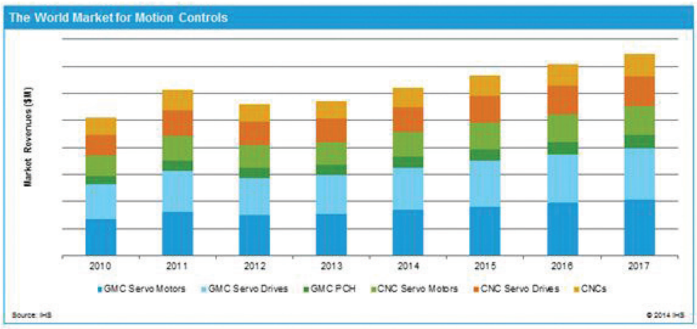
Achim Scharf
PEE Editor

Motion Control Revenues Fall Short in 2013

Global sales of motion control products recovered in 2013 to reach $12.2 billion, but growth was far too weak to overcome the 2012 market declines, leaving market revenues well below the peak level reached in 2011. According to market researcher IHS strong growth is forecast to return to the market in 2014, propelling market revenues to a new record high by the end of the year.

The motion control market reached a record level of $13.2 billion in 2011 following two years of market growth in excess of 20 %. In 2012, the motion-control market suffered from the poor economic situation in the Eurozone, a weak semiconductor market in Japan, and the fallout from overproduction in China. Market revenues declined in all three of these regions, and the global motion-control market decreased by 8.3 %. Conversely, the American market provided a bright spot for motion controls, growing over 5 % in 2012.

The results for 2013 are expected to reveal another year of subdued growth. Stable industries like packaging, materials handling, and food, beverage and tobacco continue to propel growth in machinery production and correspondingly, the motion-control market. However, motion-control sales have been constrained in 2013 by the market's dependence on volatile industries like semiconductor, machine tool, and robotics, which are known for their cyclic growth patterns. Large declines in these industries in 2009 contributed significantly to the severe decline in the motion-control market that year, and high growth in these industries in 2010 and 2011 boosted the post-recession recovery of the motion-control market.



In 2013, machinery production declined at the global level for the semiconductor and robotics industries and grew very little in the machine tool industry, according to the latest research from IHS on machinery production. Combined, these three industries account for approximately 50 % of revenues in the motion-control market, while the more stable industries like packaging, materials handling, and food and beverage account for only 16 % of market revenues. Still, the motion-control market is estimated to have grown between 1.8 % in 2013, as small declines in the machine tools and semiconductor machinery sectors were offset by growth in the rest of the motion-control market.

The outlook for 2014 is more optimistic. In the Eurozone, GDP growth is expected to accelerate and renewed confidence should spur investment in machinery upgrades, leading to an increase in motion control sales. In the Americas, recovery of the semiconductor machinery market will boost growth of motion control revenues in 2014, while in Asia, the machine tool market is forecast to recover. Globally, the motion-control market is forecast to grow by over 8 percent to reach $13.3 billion in 2014, exceeding the 2011 record value by 0.6 %.

www.ihs.com

Richardson RFPD offers SiC Tech Hub

Richardson RFPD launched its SiC Tech Hub, a micro-website featuring the latest news and new product releases related to Silicon Carbide technology.

SiC offers significant advantages in high power, high voltage applications where power density, higher performance and reliability are of the utmost importance. Industrial applications like solar inverters, welding, plasma cutters, fast vehicle chargers and oil exploration are a few examples that benefit from the higher breakdown field strength and improved thermal conductivity that SiC offers over Silicon.

Richardson RFPD has an extensive SiC offering, including a selection of of Schottky diodes, MOSFETs and IGBTs from industry-leading manufacturers Cree, Microsemi, Vincotech and Powerex. The SiC Tech Hub brings together these products with design resources. The wide range of design resources offered on the SiC Tech Hub includes application notes, brochures, datasheets, presentations, selector guides, supplier documentation, technical articles and videos. Visitors to the SiC Tech Hub may also sign-up for emailed product updates, links to technical presentation videos, and other resources like white papers and technical articles as soon as they are published. "As we continue to expand our design support resources, a centralized resource for Silicon Carbide was the next logical step," said Dave Rossdeutcher, Director Global Marketing. "With the participation of our key suppliers, the SiC Tech Hub will provide focused SiC content to support our energy and power market customers and their design activities with this rapidly expanding technology."

www.richardsonrfpd.com/sicpower

GvA partners with Fuji Electric

Mannheim-based GvA Leistungselektronik and Fuji Electric Europe are partnering for the sales of power semiconductors in Germany.

GvA as a distributor, developer and manufacturer of custom specific power electronics sees in this new product line a complement of its existing program and can thus offer its customers IGBT modules in high diversity. The product range of Fuji Electric scores with a large product range of IGBT modules in the voltage classes 600, 1200, 1700 and 3300 V, and rated current of 8 A to 3600 A. "With GvA we can not only gain a competent distribution partner for Germany. Their know-how as a developer and producer in almost every field of power electronics gives us the assurance that our customers receive the best possible advice also from a practical point of view", commented Fred Eschrich, General Manager of Fuji Electric Europe. "In our new modular inverter system MODIS for example, we use the IGBT modules of Fuji together with the intelligent IGBT drivers of Amantys with very good test results. We believe that our broad range of experience also benefits our customers. With the wide product range of Fuji we can also reach customers in Germany, we could not address so far", GvA Managing Director Werner Bresch added.

www.gva-leistungselektronik.de

Transphorm and Fujitsu Integrate GaN Power Businesses

Fujitsu Limited, Fujitsu Semiconductor Limited, and Transphorm, Inc., announced that they have reached an agreement whereby Fujitsu Semiconductor and Transphorm will integrate their GaN power devices for power supplies businesses. The three companies have also agreed that both Fujitsu and Fujitsu Semiconductor will take a minority equity position in Transphorm.

Device manufacturers around the world are competing to commercialize GaN power devices. Transphorm has already released high voltage commercial GaN devices, the company continues to make significant improvements in performance, quality and productivity. Given this, Fujitsu, Fujitsu Semiconductor and Transphorm will bring together their complementary strengths in technology and manufacturing. "Integrating Transphorm's operations with Fujitsu will enable high-volume and high-performance GaN power device production at Aizu-Wakamatsu, and we will also benefit from Fujitsu's strong technological capabilities underpinned by Fujitsu Groups' years of developments in the field of GaN power device. In addition to being a future user for GaN solutions, Fujitsu has also built customer relationships with many power management companies in Japan, one of the most important markets for Transphorm", commented Transphorm's CEO Fumihide Esaka. "From 2009, Fujitsu Semiconductor has moved forward on developing the GaN mass production technology, and at the end of 2011 began sample shipments of GaN power devices with 600 V breakdown voltage, followed by 150 V breakdown voltage GaN. We have positioned GaN power devices as one of our future core products for the Aizu-Wakamatsu plant. The business integration will enable us to collaborate with Transphorm and leverage their technologies to accelerate mass production", added Fujitsu Semiconductor's President Haruki Okada.

The employees at Fujitsu and Fujitsu Semiconductor who are directly involved in the GaN power device business will be reassigned to the new company, where they will continue development and production work with Transphorm's employees. After the integration, Transphorm will continue R&D work at both its prototyping line in the US as well as Fujitsu Semiconductor's Aizu-Wakamatsu plant, which will be under exclusive contract with Transphorm to handle wafer processing.

www.transphormusa.com, http://jp.fujitsu.com/fsl/en/

8th International Conference on Integrated Power Electronics Systems

Higher power efficiency, density, reliability, and lower volume and cost: How to reach this goals and what solutions are feasible will be discussed again at the 8th CIPS (Conference on Integrated Power Systems) from February 25-27 in Nuremberg / Germany. 235 engineers and scientists attended the CIPS 2012 at Nuremberg from March 6 to 8. They came from 17 countries in Asia, America and Europe.

The conference is organized by VDE ETG and ECPE and technically co-sponsored by the IEEE PELS and ZVEI. The conference papers did undergo a peer review process which allows their storage in the IEEE Xplore digital data base. The Technical Program Committee has selected 81 papers to be presented; 29 of them will be poster presentations. The best poster as well as the best young engineers presentation will be awarded.

As usual for CIPS there is a frame of 3 Keynotes and 9 Invited Papers given by worldwide leading experts

Keynote Papers

- What are the big challenges in power electronics?
- Johann W. Kolar, ETH Zurich, Switzerland
- Simulation and test vibration – nonlinear effects in durability of electronic systems
- Abhijit Das Gupta, University of Maryland, USA
- Present and future of GaN Power Devices
- Daisuke Ueda, Advanced Technology Research Laboratories, Panasonic, Japan

Invited papers

- Power module reliability
- Transient hygro-thermal-response of power modules in inverters-mission profiling for climate and power loading
- Power Supply With Integrated PassivEs-POWERSWIPE
- Practical Aspects and Uses of Thermal Interface Material Testing Methods
- EMI and Integration
- Power Electronics - Key Technology for Renewable Energy Systems - Status and Future
- New applications in power electronics for integrated high-speed magneto-resistive current sensors
- Packaging very fast switching power semiconductors
- SiC Power Electronics

Participants especially from universities and research institutions are invited to present results and demonstrators from current research in the Table Top Exhibition.

More Power in 2014

APEC 2013 in Long Beach/California closed with a record of nearly 4,000 delegates (+ 27 %) and 187 exhibitors, making it one of the greatest power electronics conferences and showing the increasing interest in the role of power electronics for energy efficiency. Wide bandgap technologies such as SiC and GaN were of major interest, and this will continue in the 2014 event from March 16-20 in Fort Worth/Texas.

APEC 2014 will start on March 17 afternoon with the plenary session, traditionally a number of speeches highlighting the actual subjects of power electronics within the conference, before the exhibition opens within the late afternoon. Already on March 15/16 tutorials will be offered.

Plenary session on actual topics

Transforming energy management is the first speech given by Sami Kiriaki, SVP Texas Instruments. The topic of power and energy management continues to draw the interests of semiconductor, business and investment communities. Leading technology companies have always respected power, but it is an area that has transcended from the "necessary evil" of the past to the "technology enabler" of today and the future. Power and energy management enable every portable device to be portable, and without it the run-time alone would have limited many markets. Advanced power management strategies developed in the portable world have been transformed into new power technologies used in many transportation and stationary applications. These include new circuit solutions that minimize losses, while improving the response to load variations. Developments in leading-edge semiconductors, circuits, packaging and manufacturing allow designers to now take a systems approach to power and energy management, which will help fuel growth for power electronics in markets, such as portable, transportation, computing and communication. This presentation will cover the challenges for these industries, and describe how new power and energy management technologies are addressing them. For example, the expansion of the wireless Internet will be limited by the need for energy. Efficient power and energy management solutions at each node in the network are required. These solutions will benefit from the new power management technologies to become more power efficient, more power dense, and more responsive to wide dynamic load variations. New power solutions will change the type of products and the way we do business in this diverse power management industry.

Power electronics in emerging applications is the subject to be presented by Dong F. Tan, Northrop Grumman Corporation. The company's Advanced Electrical Power Systems (AEPS) features modularity and scalability to minimize cost, schedule and technical risk. Its minimum set of five standard electronic slices allows various units and hence the power system to be configured either as regulated or unregulated bus. Its peak power tracking capability, together with high power conversion efficiency and tightly regulated bus voltage, reduces significantly the required solar array capacity and payload power distribution size and weight for a given mission. It supports either Li-Ion or NiH2 batteries to deliver prime bus power from 1 to 8 kW with scalability and modularity. This presentation focuses on simulated and measured performances of the peak power tracker (PPT) circuit implemented for a flight program. A brief overview of PPT architecture and implementation, a report on simulation and measurement results on steady-state responses, and key performance, such as tracking accuracy and tracking time, will be reported. Transient responses for mode changes under various orbit conditions, such as eclipse entry and eclipse exit, will be presented. Various modes under different illumination conditions will also be discussed.

Mission critical power will be discussed by Miguel Chavez, Director of Engineering, Eaton. A look at mission critical power and how the evolution of industries requiring uninterrupted electric power and advances in power electronics have helped shape its path. From early computer rooms to today's hyper-scale data centers, the demands for safe and reliable power have grown significantly and are part of a world that expects to be interconnected 24/7. What will the future require? The trends, technological and otherwise, that will impact how the challenges of supplying the world with mission critical power are addressed.

ARPA-E initiatives in high-efficiency power conversion will be introduced by Tim Heidel, Program Director, Advanced Research Projects Agency–Energy (ARPA-E). Advances in power electronics promise substantial energy efficiency gains across a wide range of power conversion applications. Innovations in wide bandgap power semiconductor devices and magnetic materials developments, in particular, hold enormous potential, but, today, are still at a somewhat early stage of technological maturity. ARPA-E is an agency of the U.S. Department of Energy that focuses on funding early stage technologies that have the potential to have a transformational and disruptive impact on the United States' energy future. Over the past four years, ARPA-E has launched several power electronics focused programs including the agency's ADEPT (2010), Solar ADEPT (2011), and SWITCHES (2013) programs. This talk will give an overview of some of the successes from these programs thus far and some of the challenges that have yet to be overcome.

Fort Worth's convention center, home of APEC 2014

Significant developments and trends in 3D packaging will be discussed by Brian Narveson and Ernie Parker, Co-Chairman of the PSMA Packaging Committee. The packaged and modular power supply industry is constantly challenged by its customers to deliver more power in a smaller volume. This applies whether selling 1 W modules or multi kW AC/DC product. The focus on footprint alone is no longer adequate. The efficient use of the z-dimension to minimize the volume of the package is now in the forefront. Cost effective, volume efficient 3D packaging is rapidly being adopted by the power industry. The Packaging Committee of the Power Supply Manufactures Association (PSMA) has undertaken a study to obtain an overview of the technology and product trends that are evolving, what the drivers are and what the market opportunities will be over the coming years. This study provides valuable insights into state of the art products and technology roadmaps while identifying R&D and manufacturing challenges that need to be addressed. The study encompasses developments from chip level integration and Silicon stacking to high-power modules (up to 10 kW). The study also covers emerging technologies for additive manufacturing such as 3D printing and how it is being used in the power supply industry. The presentation would verbally and graphically present the results of this study, which includes the state of the industry with identification of key technology, manufacturing and market trends in 3D power packaging.

System reliability vs. efficiency, this is the final subject to be discussed by Brian Fortenbery from the Electric Power Research Institute (EPRI). System designers often strive to increase reliability by building redundancy into their architectures. Since we know that even the most reliable components must fail eventually, the best approach to overcoming that risk is to add in a redundant component to provide the required functionality in the case of a failure. The problem with this approach is that usually, we like to allow each component to carry equal parts of the load, and switch over in the event of a failure. As such, the efficiency of the system suffers, and energy use is increased. This presentation will discuss the pros and cons of this approach, and suggest some alternatives that can increase efficiency and save energy.

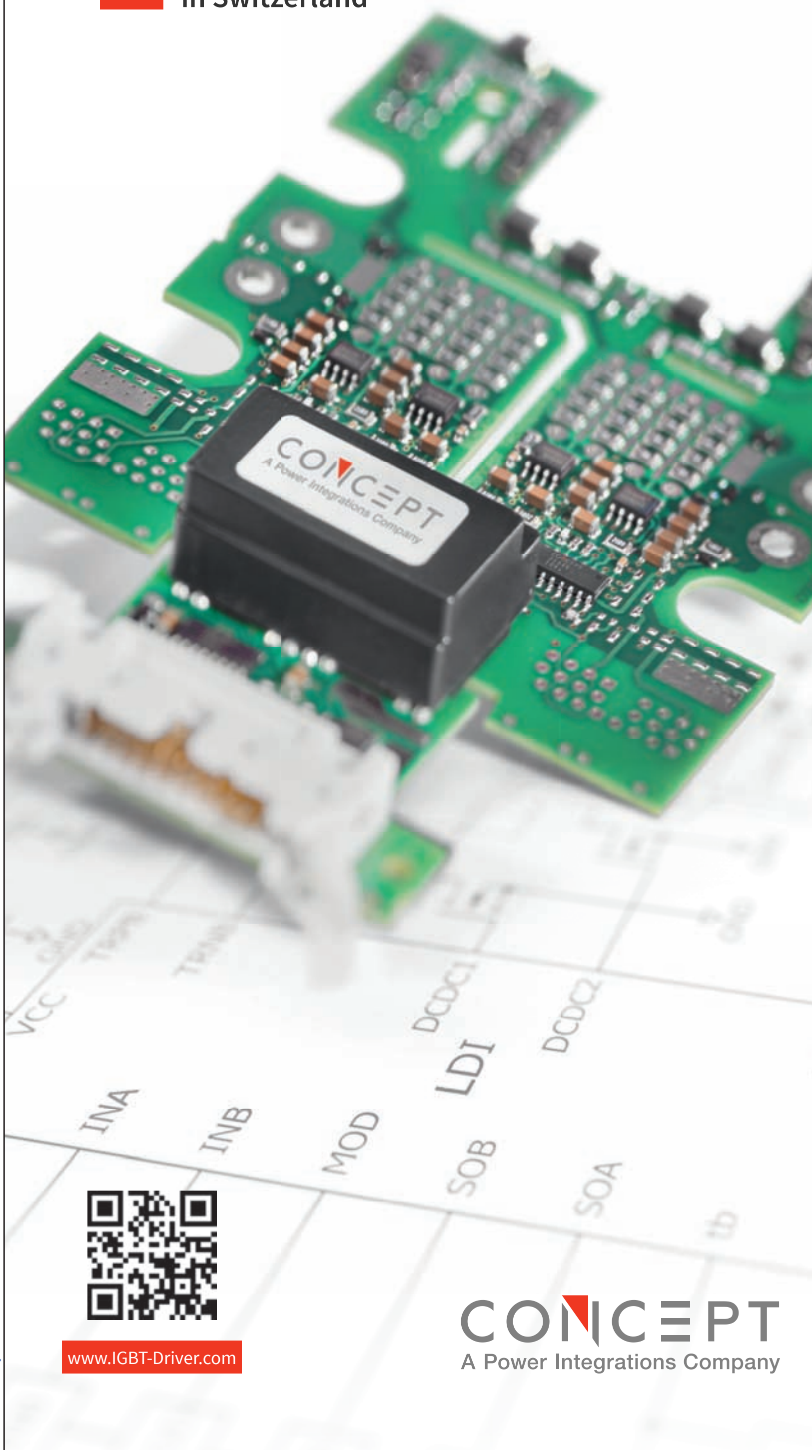
Rap sessions

Rap (panel) sessions are intended to discuss certain subjects under a broader scope with a number of penelists. Two sessions will be held on March 18 from 5.00 – 6.30 pm.

Session 1 will cover smart grid infrastructures. Once upon a time power grid infrastructures only concerned large-scale industrial operations, civil engineers, and municipalities. Today we are faced with the convergent pressures of the near-simultaneous advent of the Internet of Things and the Smart Grid. This means that everyone at every level of today's users, distributors, and generators of power must be aware of the technologies, infrastructures, regulations, and protocols involved. These systems range from consumer handheld products and remote service subsystems involved in the "Internet of Things" to the smart-home and micro grid-oriented bridge technologies, to the municipal grid itself. The real challenge, however, lies in how we integrate not only the systems, but the management protocols, regulatory issues, service priority concerns, and privacy & security. In a world of negotiated power, who decides what facilities and organizations take priority in a brownout situation? How are the various layers of management, from various sectors of the industry, negotiate and determine priority in a system? How do we address security in a system of interleaved and overlapping devices and systems? There are many aspects of the smart grid beyond simply being "smart" that must be determined and create plans and strategies for in order to properly achieve the lofty goals having set for the industry.

Session 2 is a follow-up to a 2013 session now entitled Wide Bandgap Semiconductors vs Silicon in Power Electronics. For several years we keep hearing about how these semiconductors are going to provide dramatic improvements in power electronics system performance. Significant resources have been and continue to be expended - will this be the year of exponential growth? Will the huge financial investments made thus far pay off soon? Will the technology performance match the rhetoric and when? Will the price/performance ratio be where it needs to be? What applications will be first? Will the innovation, performance, device and circuit techniques and implementation using Silicon devices continue to dominate new designs. Will GaN and SiC devices become a higher value proposition for design engineers and enter mainstream adoption displacing Silicon power semiconductors in new designs and applications? Will Silicon continue to be good enough at a lower price or will wide bandgap devices enter main stream adoption? Perhaps answers can be given by the panel of experts.

More about APEC 2014 in our next issue.

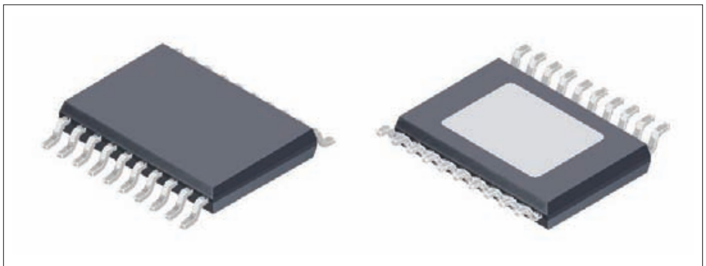


Microstepping Motor Driver Featuring Translator

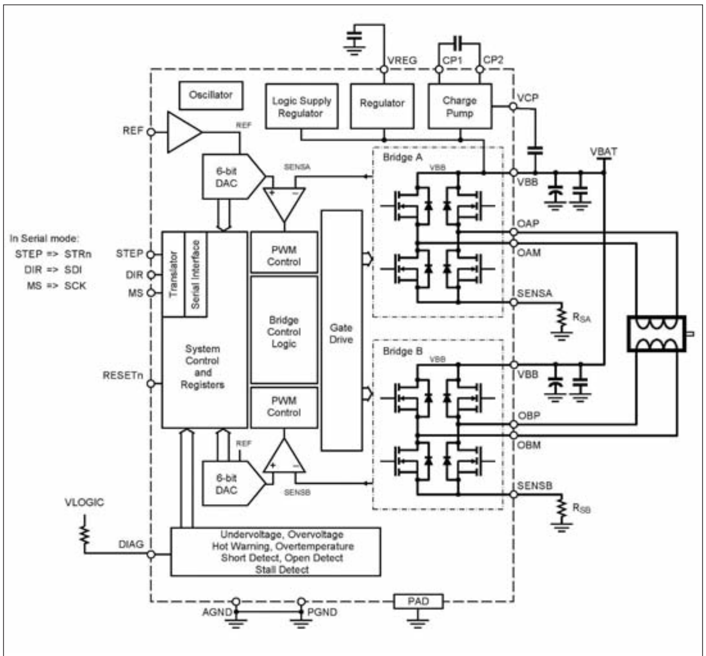
Allegro’s new A4992 IC is a microstepping motor driver with integrated phase current control and a built-in translator for easy operation. It is a single chip solution designed to operate bipolar stepper motors in full, half, quarter, eighth, and sixteenth step modes, at up to 28 V. The A4992 is supplied in a 20-pin TSSOP power package with an exposed thermal pad (package type LP). This package is lead (Pb) free with 100% matte-tin lead frame plating.

At power-on the A4992 is configured to drive most small stepper motors with simple step and direction inputs. The device can be used for high temperature applications such as headlamp bending and levelling, throttle control, and gas recirculation control in automotive applications. It is also suitable for other low current stepper applications such as air conditioning and venting. It provides a flexible microstepping motor driver controlled with simple step and direction inputs. It can also be switched into an optional serial interface mode, where it can be configured and driven via an SPI compatible serial interface.

The current regulator operates with fixed frequency PWM. It uses adaptive mixed current decay to reduce audible motor noise and increase step accuracy. The current in each phase of the motor is controlled through a DMOS full bridge using synchronous rectification to improve power dissipation.



The A4992 is supplied in a 20-pin TSSOP power package with an exposed thermal pad



A4992 functional block diagram

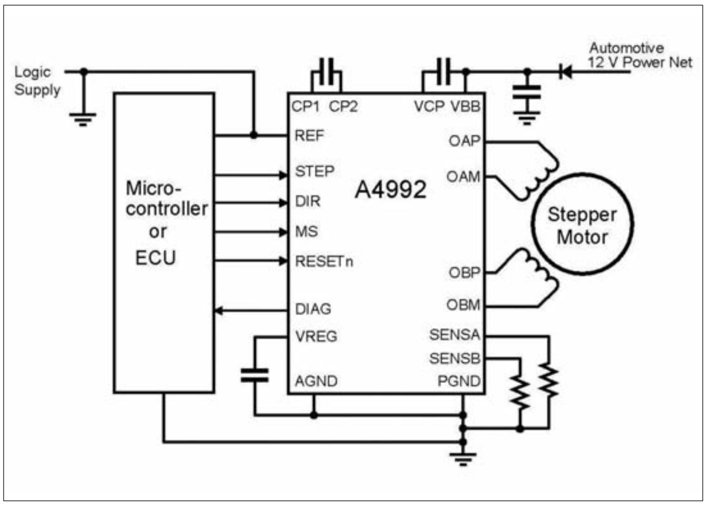
Internal circuits and timers prevent cross-conduction and shoot-through when switching between high-side and low-side drives. The outputs are protected from short circuits. Features for low load current and stalled rotor detection are included. Chip level protection includes hot thermal warning, overtemperature shutdown, and overvoltage and undervoltage lockout. An optional serial interface mode, using the STEP, DIR, and MS inputs, can be used to configure several motor control parameters and diagnostics.

Serial interfacing

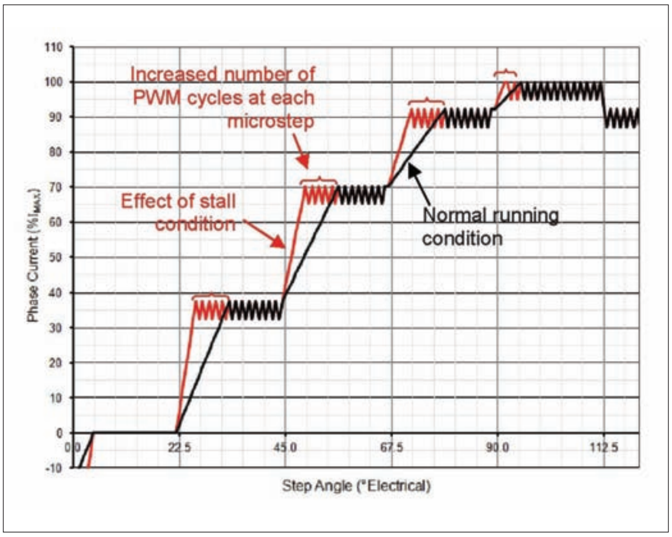
A three wire synchronous serial interface, compatible with SPI, can be used to control all features of the A4992.

The A4992 powers-up in the default step and direction control mode. The serial mode is only available following a specific sequence on the DIR and MS pins when STEP is high. The sequence starts when STEP is high and MS is held high and DIR is held low for longer than the Sequence Minimum Hold Time (t_{SSH}). MS must then be held low and DIR high for longer than t_{SSH}, followed by holding MS high and DIR low for longer than t_{SSH}. The final step is to hold DIR high for t_{SSH}, at which time the A4992 will enter the serial control mode.

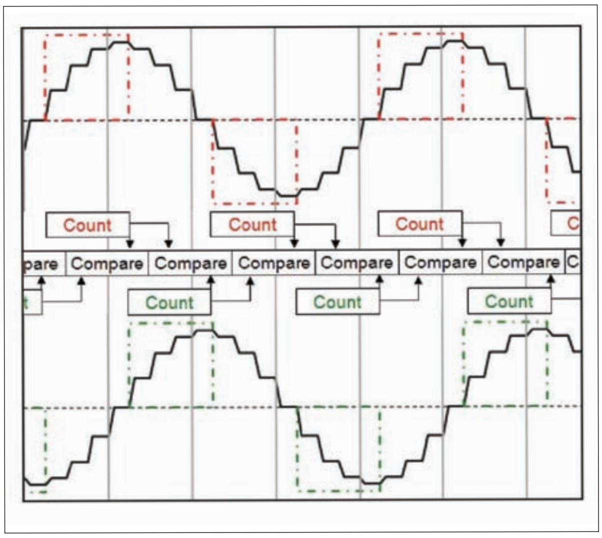
If STEP is taken low at any time during the sequence then the sequence is reset and the sequence of MS and DIR must be repeated. When the sequence is accepted by the A4992, the DIAG output will change state for the Serial Mode Acknowledge Pulse duration (t_{SAP}) , to indicate that the switch was successful. For example if a fault is present when switching between modes, DIAG will be low during the sequence and will first go high, to acknowledge the mode change, then go low after t_{SAP}. If no fault is present, DIAG will be high during the sequence and will first go low to acknowledge the mode change, then go high after t_{SAP}. When in serial control mode the function of the STEP, DIR, and MS pins change. STEP assumes the function of STRn, the serial data strobe input, DIR functions as SDI, the serial data input, and MS as SCK, the



Typical A4992 application schematic



LEFT: Effect of stall condition on current rise



RIGHT: Stall detect by PWM count compare

serial clock.

The A4992 will remain in the serial mode as long as the SER bit remains set to 1. If a serial transfer occurs when SER is 0, then the A4992 will revert to the step and direction control mode after the Serial Mode Exit Time, t_{SSEX}, following the rising edge of STRn. The STRn, SDI, and SCK inputs will then revert to their default functions, STEP, DIR, and MS, respectively. The DIAG output will change state for t_{SAP} to indicate that the switch was successful.

The A4992 can be operated without the serial interface, by using the default settings and the STEP and DIR inputs. Application-specific configurations are only possible, however, by setting the appropriate register bits through the serial interface. In addition to setting the configuration bits, the serial interface can also be used to control the motor directly.

Detecting stall conditions

A PWM monitor feature is included in the A4992 to assist in detecting the stall condition of the stepper motor. This feature uses the indirect effect of the back EMF on the current rise quadrant to determine the point at which a stall occurs.

When a motor is running normally at speed, the back EMF, generated by the magnetic poles in the motor passing the phase windings, acts against the supply voltage and reduces the rise time of the phase current. The PWM current control does not activate until the current reaches the set trip level for the microstep position. When a motor is stopped, as in a stall condition, the back EMF is reduced. This allows the current to rise to the limit faster and the PWM current control to activate sooner. Assuming a constant step rate and motor load this results in an increase in the quantity of PWM cycles for each step of the motor.

The A4992 uses this difference to detect a motor changing from continuous stepping to being stalled. Two PWM counters, one for each phase, accumulate the count of PWM cycles when the phase current is stepped from zero to full current. At the end of each phase current rise, the counter for that phase is compared to the counter for the previous current rise in the opposite phase. If the difference is greater than the PWM count difference in the Configuration register, then the ST fault signal will go low.

This stall detection scheme assumes two factors:

- The motor must be stepping fast enough for the back EMF to reduce the phase current slew rate. Stall detection reliability improves as the current slew rate reduces.
- The motor is not being stepped in full step. Although stall detection cannot be guaranteed using this detection method, good stall detection reliability can be achieved by careful selection of motor speed, count difference, and by conforming to the above factors.

More application information:

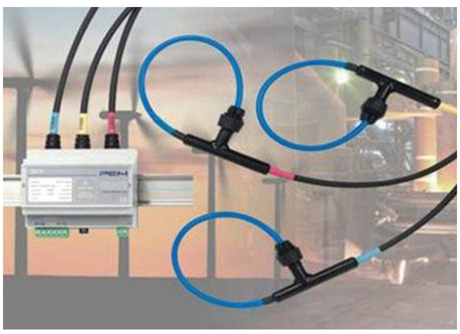
www.allegromicro.com/en/Products/ Motor-Driver-And-Interface-ICs/Bipolar-Stepper-Motor-Drivers/A4992.aspx

New current transducer from PEM

The new RCTrms 3-ph current transducer from Power Electronic Measurements (PEM) delivers a convenient, safe and accurate solution for measuring current in three phases. It features a thin, clip-around, flexible sensor coil and provides accurate true rms measurement with 4-20mA or 0-5V output, enabling simple installation with PLC's, SCADA systems or automation equipment.

The compact, DIN-rail or panel mountable RCTrms-3ph extends the design of PEM's proven RCTrms single-phase transducer, connecting to three Rogowski coils to capture measurements from three current phases simultaneously. This significantly reduces cost per channel, while enabling safe and fast installation.

With 18 current ratings options from 100A to 50,000A, and a choice of 300mm, 500mm, 700mm or custom coil lengths, the RCTrms-3ph can be used in many applications and connected to a wide variety of SCADA systems, PLCs, data loggers, protection equipment or motor controllers. The clip-around coil design allows fast and easy positioning, and provides accurate results without needing to be centralised around the conductor. An isolated BNC-BNC cable-split option is available, to ease installation such as when threading through existing conduit.



RCTrms-3ph operates from a 12V-24V supply, and generates an accurate, true-RMS output as an industry-standard 4-20mA or 0-5V signal. The transducer provides a galvanically isolated measurement. Each unit is supplied with a traceable calibration certificate.

The RCTrms-3ph uses non-magnetic materials, which ensures excellent linearity and prevents damage from over currents. Typical accuracy is better than 1% of reading from 10 to 100% full scale. The units are safe, with 2kVdc power-supply isolation and 2kVpeak coil rating, and are CE marked and compliant with EMC EN 61326-1 2006 and IEC61010-1:2001.

Further information can be found at **www.pemuk.com.**

First Products for Vicor's Converter housed in Package Technology

Vicor has introduced a powerful component packaging platform – 'Converter housed in Package ChiP' in March 2013. New generation components can provide a staggering 4X increase in power density and 20 percent reduction in power losses, i.e. power densities up to 3 kW/in^3 (183 W/cm^3) and up to 98 % efficiency.

ChiP technology is made possible by many stages being analogous to semiconductor wafer fabrication. Individual converters are arrayed to utilize 100 % of the PCB material, with no area lost to lead/pin attach. The array is then sawn into individual 'chip-scale' components with no superfluous, non- value- added packaging, thus minimizing space used in customer designs.

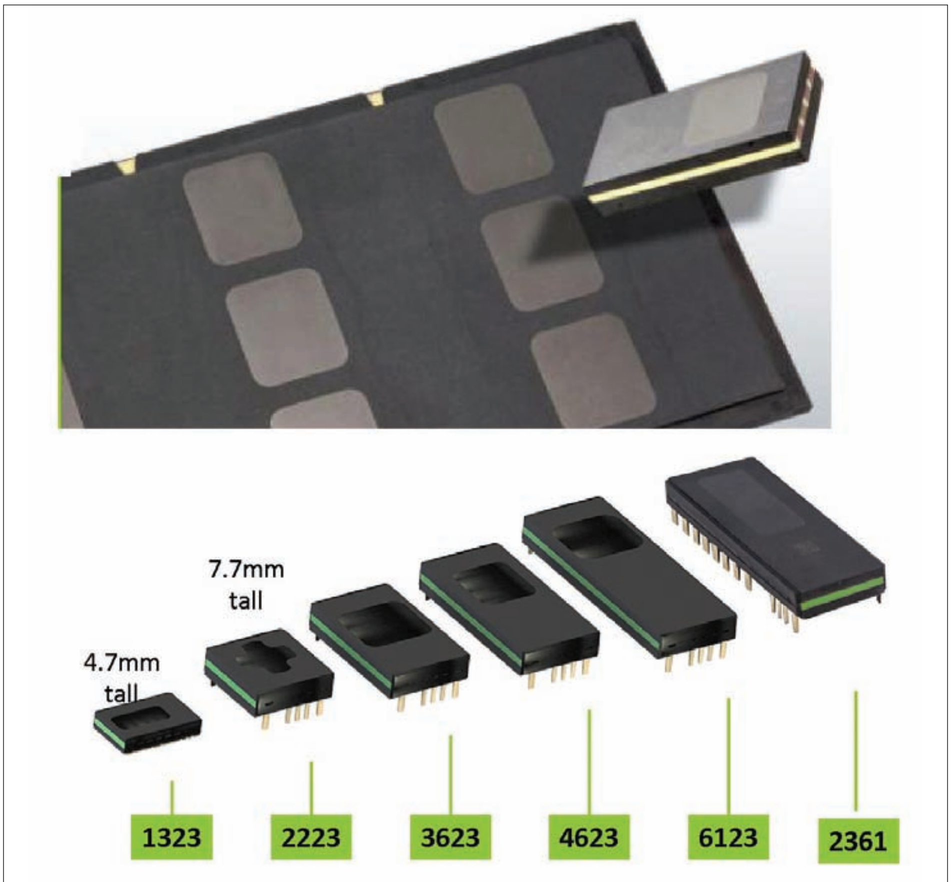
ChiP utilizes integrated magnetic structures (but not for the output inductor) penetrating through a high density interconnect substrate with symmetrically two-sided layout to essentially double power density. Similar to how microprocessors are sawn out of scalable wafers, a multiplicity of ChiPs are constructed on a panel, molded, and then sawn into as many as 80 individual power components, exposing 'bar codes' from which interconnect terminals are formed. X- and y- dimensions are flexible, allowing low- or high- power converters, with additional flexibility in the z- axis to allow optimized magnetic transformer or inductor designs.

The lineup of components includes five different package sizes, with more on the way. This is enabled by the underlying scalability of the ChiP manufacturing process. Process flexibility enables a wide range of power component sizes to be built using the same manufacturing tooling and processes without waste, resulting in cost-effectiveness. This dimensional flexibility is reflected in the package reference, again analogous to semiconductors. For example, a '4623' package measures 46 mm by 23 mm as sawn.

ChiP technology supports packages as thin as 4.7 mm ranging from '1323' to '6123' with current capability up to 180 A, voltage capability up 430 V and power capability up to 1.5 kW. With an expanding array of package sizes, voltage capability up to 800 V and power capability up to 4 kW are possible. ChiP packaging offers flexible cooling paths including single- or dual- sided cooling plus dissipation through the leads, as well as cold- plate options and standardized finned heatsinks.

ChiP bus converter

The VI Chip Bus Converter is a Sine Amplitude Converter (SAC), operating from a 260 to 410 VDC primary bus to deliver an isolated 32.5 to 51.3 VDC unregulated secondary voltage.



The Sine Amplitude Converter (SAC) uses a high frequency resonant tank to move energy from input to output. The resonant tank is formed by a parasitic capacitance and leakage inductance in the power transformer windings. The resonant LC tank, operated at high frequency, is amplitude modulated as a function of input voltage and output current. A small amount of capacitance embedded in the input and output stages of the module is sufficient for full functionality and is key to achieving high power density of 98 %.

Low impedance is a key requirement for powering a high-current, low-voltage load efficiently. A switching regulation stage should have minimal impedance while simultaneously providing appropriate filtering for any switched current. The use of a SAC between the regulation stage and the point of load provides a dual benefit of scaling down series impedance leading back to the source and scaling up shunt capacitance or energy storage as a function of its K factor squared.

However, the benefits are not useful if the series impedance of the SAC is too high. The impedance of the SAC must be low, i.e. well beyond the crossover frequency of the system.

A solution for keeping the impedance of the SAC low involves switching at a high frequency,in this case 1.5 MHz. This enables small magnetic components because magnetizing currents remain low. Small magnetics mean small path lengths for turns. use of low loss core material at high frequencies also reduces core losses.

A major advantage of SAC systems versus conventional PWM converters is that the transformer based SAC does not require external filtering to function properly.

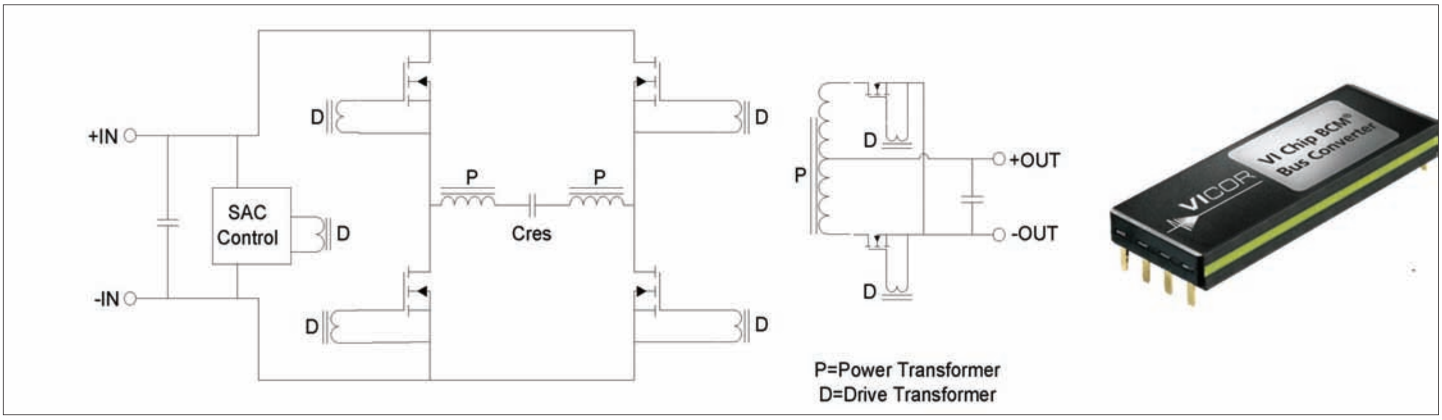
The BCM380y475x1K2A30 offers low noise, fast transient response, and industry leading efficiency and power density. In addition, it provides an AC impedance beyond the bandwidth of most downstream regulators, allowing input capacitance normally located at the input of a POL regulator to be located at the input of the BCM module. With a K factor of 1/8, that capacitance value can be reduced by a factor of 64X.

Current sharing

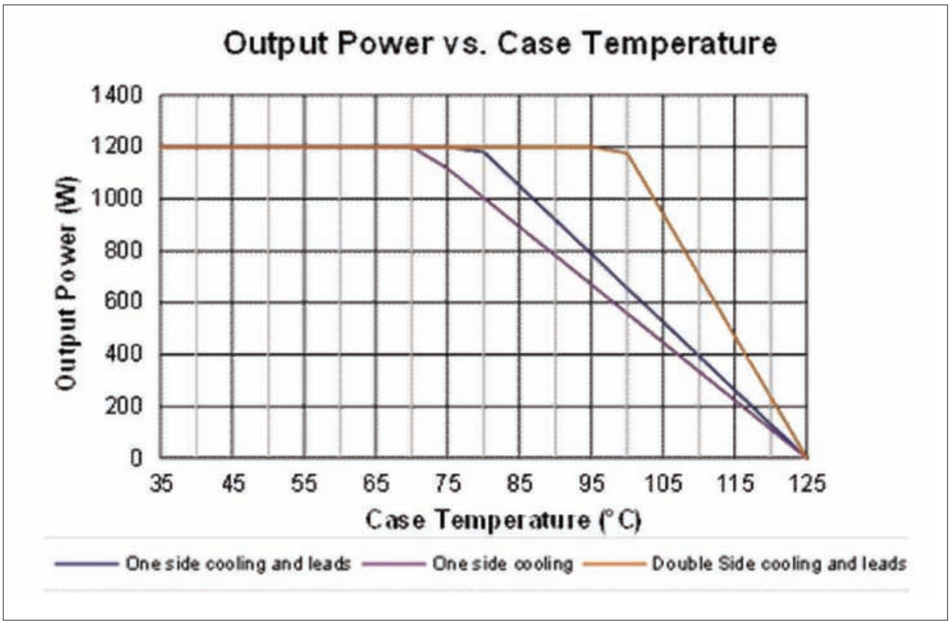
The performance of the SAC topology is based on efficient transfer of energy through a transformer without the need of closed loop control. For this reason, the transfer characteristic can be approximated by an ideal transformer with a positive temperature coefficient series resistance.

This type of characteristic is close to the

LEFT: ChiP power components are formed out of a scalable power platform



ABOVE: Principle of Sine Amplitude Converter (SAC) topology



Cooling options include top, bottom, or both sides plus leads

impedance characteristic of a DC power distribution system both in dynamic (AC) behavior and for steady state (DC) operation.

When multiple BCM modules of a given part number are connected in an array they will inherently share the load current according to the equivalent impedance divider that the system implements from the power source to the point of load.

Thermal management

Leveraging the thermal and density benefits of ChiP's packaging technology, the BCM module offers flexible thermal management options with very low top and bottom side thermal impedances. Thermally-adept ChiP-based power components, enable customers to achieve low cost power system solutions with previously unattainable system size, weight and efficiency attributes, quickly and predictably.

Reverse operation

BCM modules are capable of reverse power operation. Once the unit is started, energy will be transferred from secondary back to the primary whenever the secondary voltage exceeds VIn • K. The module will continue operation in this fashion for as long as no faults occur. The BCM380y475x 1K2A30 has not been qualified for continuous operation in a reverse power condition. Furthermore fault protections which help protect the module in forward operation will not fully protect the module in reverse operation.

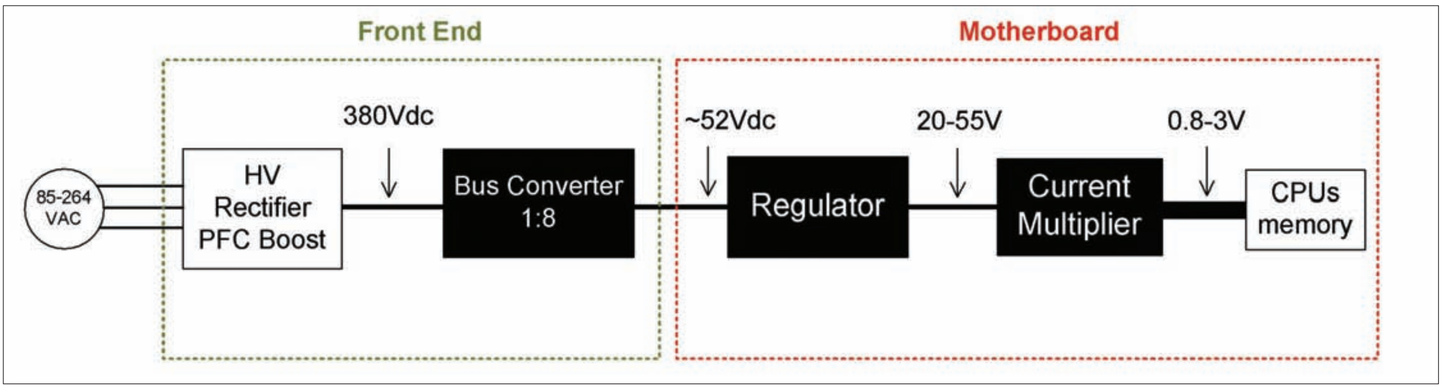
Transient operation in reverse is expected in cases where there is significant energy storage on the output and transient voltages appear on the input. Transient reverse power operation of less than 10 ms, 10 % duty cycle is permitted and has been qualified to cover these cases.

CHiP supports all known architectures including isolated bus conversion, DC/DC, buck, boost, and buck-boost regulation and POL current multiplication. Zero-current and zero-voltage switching topologies are also supported with the aid of the online-tool PowerBench. AC/DC with PFC eliminates one regulation stage compared to a conventional approach and thus increases efficiency, and the regulator rejects line frequency from input and regulates the point of load. Component-based approach enables different partitioning of the system. The Bus Converter can be part of the Frontend or the Motherboard,

An BCD380x475x1K2A30 1.2 kW Evaluation Board is available for order from Digikey, Future Electronics, and Vicor.

http://www2.vicorpower.com/6123BCM

BELOW: AC to Point of Load and Post Boost PFC application



High Efficiency AC/DC Converter IC with Integrated PFC

ROHM has recently announced the development of a high-efficiency AC/DC converter that integrates PFC (Power Factor Correction) and QR (Quasi-Resonant) controllers into a single package, making it suited for 100 W-class equipment such as TVs and industrial power supplies.

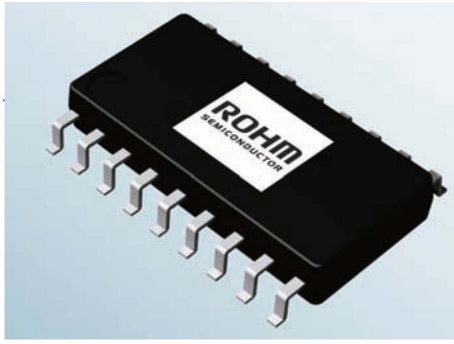
The BM1C001F is the first to incorporate an ON/OFF setting function and new PFC output control method within the PFC controller. This improves efficiency during light loads and significantly reduces standby power. Power supplies utilizing this IC ensures compliance with Energy Star 6.0, the latest international energy standard. In addition, the 2-controller-in-one design reduces the number of external parts, contributing to power supply miniaturization.

In recent years came a need for greater efficiency to improve energy savings in electronic devices of all types. But in order to control harmonics in equipment over 75 W, which can be harmful to other devices, a PFC controller is required, which may have a negative effect on efficiency. Also, to reduce design and evaluation loads while enabling easy repair, power supply adapters are currently progressing in 100 W-class equipment. However, conventional solutions combine an AC/DC converter with built-in QR controller with a separate PFC circuit, which can present problems regarding board space and power supply size.

In response, ROHM integrated a special function that allows for flexible ON/OFF setting of the PFC controller. This improves conversion efficiency during light loads while reducing standby power consumption. In addition, a new proprietary PFC output control method is included in the PFC controller for boost converter operation, significantly increasing efficiency - particularly in 100 VAC systems. For example, integrating this IC in a 100 W class power supply will result in 89 % efficiency at 100 VAC and 89.5 % efficiency at 230 VAC, clearing the latest Energy Star standard (6.0) stipulating at least 88% efficiency. Also, layout optimization makes it possible to integrate the PFC and QR controllers in a single package, reducing parts count by 20 % compared with conventional solutions.

ON/OFF setting function improves conversion efficiency

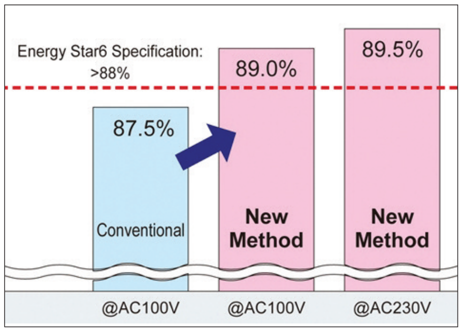
The industry's first PFC controller ON/OFF setting function improves conversion efficiency at light loads and reduces standby power consumption. It monitors the load power on the secondary side and switches the PFC controller ON/OFF, including in the load region where PFC is not required (below 75 W), improving power supply conversion efficiency.



High-efficiency AC/DC converter IC with integrated PFC and QR control function

Adopting this IC in 100 W class power supplies results in a standby power of less than 85 mW at 100 VAC and 190 mW at 230 VAC, clearing the latest Energy Star standard (6.0) requiring 210 mW or less.

www.rohm.com/eu



100 W-class efficiency comparison Source: ROHM

New Precision Single-Phase Power Analyzer

Engineers developing power supplies for single-phase electronics face new demands for greater energy efficiency and lower line pollution, along with a growing array of government regulations and commercial demands to reduce energy consumption. As new semiconductor technologies such as GaN (Gallium Nitride) and SiC (Silicon Carbide) emerge, new test and measurement tools are required to keep pace. “Thus power is one of the most dynamic segments in electronics today given the intense interest on the part of consumers, business and government to reduce overall energy consumption. Improving battery life is another key driver,” said Curt Willener, general manager, Power Analyzer Product Line, Tektronix.

Tektronix’s new PA1000 single-phase power analyzer provides engineers designing and testing power supplies, consumer electronics and other electrical products with accurate power measurements. Features such as a color graphical display, one-button application modes and intuitive menu system enable optimum instrument set up in seconds, and the PWRVIEW PC software includes comprehensive reporting features such as a full compliance IEC62301 standby power certificate.

A full-color graphics display makes setup and other tasks easy and intuitive, with one-button access to measurement results, power waveforms, harmonic bar graphs, and menus. Application-specific test modes for standby current, lamp ballast testing and energy integration help to simplify optimization of instrument settings, saving engineers time and reducing mistakes. PWRVIEW PC software further simplifies testing with one-click test automation for compliance-test applications.

Standard interfaces include LAN, USB and GPIB,

Spiral shunts

The PA1000 offers 0.05 % basic accuracy and 1 MHz measurement bandwidth. Two internal current shunts are included - one for precise low-current current measurements up to 1 A, and another for current measurements up to 20 A.

The 1 A shunt is particularly useful for maintaining measurements resolution and accuracy on demanding low-current signals common to standby power testing. The 20 A shunt design ensures stable, linear response over a wide range of input current levels, ambient temperatures, crest factors, and other variables. This new design is superior to other shunt technologies and contributes to the instrument’s reliable accuracy and repeatability over a wide range of signal conditions common in today’s power conversion technologies. The spiral construction not only minimizes stray inductance (for optimum high frequency performance) but also provides for high overload capability and improved thermal stability.

Application-specific test modes

Some applications require special instrument settings to ensure proper measurements. The PA1000 simplifies setup for these applications by automatically choosing instrument settings and parameters that are optimized for each type of measurement application, resulting in more reliable measurement results with less opportunity for user setup error.

Ballast mode - synchronizes measurements for highly modulated electronic ballast waveforms. In modern electronic lighting ballasts, it is often difficult to make accurate measurements because the output signals are high frequency waveforms that are heavily modulated by the power frequency. Ballast mode provides a way of locking the measurement period to the power frequency.

Standby power mode - driven by consumer demand and energy efficiency regulations (such as ENERGY STAR), there is an ever-increasing need to measure power consumption of products while they are in standby mode. One of the most widely used standards for measurement is IEC 62301. Part of this standard requires the measurement of power over a prolonged period of time without missing any short duration power events. The PA1000 standby power mode provides continuous sampling of voltage and current to produce an accurate Watts measurement over the user specified period.

Inrush mode - for measuring the peak current during any event. Typically this is used to measure the peak current when a product is first switched on.

Integrator mode - used to provide measurements for determining energy consumption (Watt-hours, Ampere-hours, etc.). The PA1000 ➡20

Tektronix’s new PA1000 offers 0.05 % basic accuracy and 1 MHz measurement bandwidth

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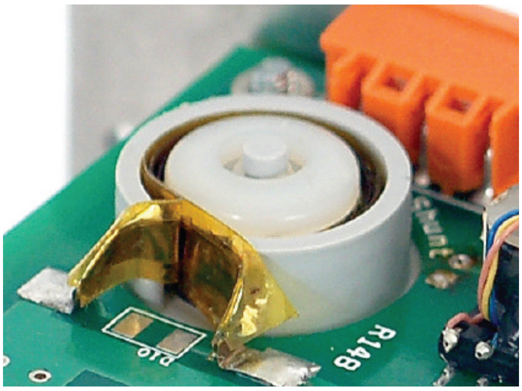
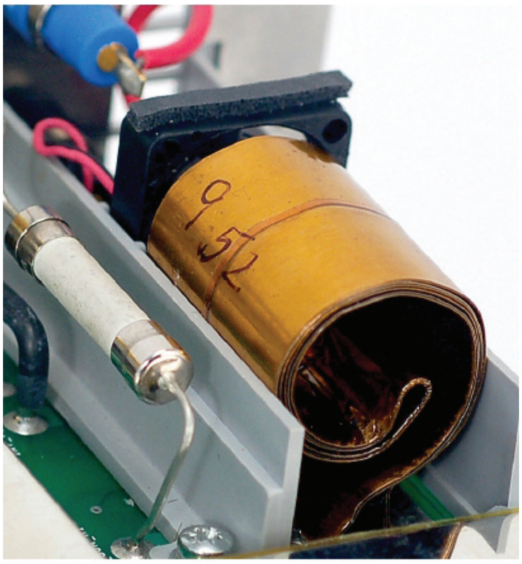


The 1 A shunt is particularly useful for low-current signals



The 20 A shunt design ensures stable response over a wide range of input current levels

17 features harmonics analysis to the 50th harmonic as a standard feature. Harmonics, THD and related measurements can all be analyzed simultaneously with other power parameters.

PWRVIEW PC software

PWRVIEW is a supporting software application for Windows PCs that compliments and extends the functionality of the PA1000. It enables the user to do the following:

- Communicate with the PA1000 over any of the instrument comm ports
- Change instrument settings remotely
- Transfer, view, and save measurement data in real-time from the instrument, including waveforms, harmonic bar charts, and plots
- Log measurement data over a period of time
- Communicate with and download data from multiple PA1000 instruments
- Create formulae for the calculation of power conversion efficiency and other values
- Export measurement data to .csv format for import into other applications
- Automate instrument setup, data collection, and report generation for key applications with just a few clicks, using wizard-driven interfaces
- Perform automated full compliance testing for Low Power Standby per IEC 62301, Edition 2
- Additional test automation will be added with future releases

www.tek.com/power-analyzer/pa1000

Practical Use of SiC Power Semiconductors

Silicon Carbide (SiC) power devices are enabling components mainly in the context of higher switching frequencies and/or small footprints in power electronics. However, this trend imposes new challenges on the packaging of the chips. Typical stray elements like inductances become crucial elements in the circuit. In addition, different considerations regarding the thermal design in power modules arise when SiC chips are taken into consideration. Furthermore, the aspects of power density as well as the general utilization of SiC's high temperature capability are important factors in reliable implementation of SiC-based power semiconductors in modern systems. The article will give an insight into how these boundary conditions can be implemented in innovative solutions using SiC chips. **Peter Friedrichs, Senior Director SiC, Infineon AG, Erlangen, Germany**

SiC power technology, predominantly in form of Schottky diodes, is meanwhile established in the market. High-power solutions using power-module technologies have recently become available. Usually, the aim of such components is to enable system benefits, for example by increasing the switching frequency or reducing losses. If this is successful, the high cost of SiC-based components can be compensated by reduced efforts for passive elements and/or cooling.

While the discrete, unipolar SiC devices as single chips are more or less ready to achieve higher frequencies (>100 kHz in PFC units), this is still a challenge for power modules. Solutions in a power range with traditional modules have high stray inductances and thus the di/dt is increased if combined with an increase in the frequency. A plug and play between SiC and Silicon at chip level in existing modules could devaluate the theoretical SiC performance. It is necessary to improve high-current modules in order to get the full benefit of SiC in the frequency range above 20 kHz.

Current and power density considerations for state-of-the-art SiC devices

Whilst the reduction of parasitic elements in power modules using SiC chips is in line with the approach also used for future Silicon solutions, it might happen that different optimization criteria will apply for the thermal design. The reason for this is that the cost contribution of chips in a power module with SiC is different from one with Silicon. Thus, the best solution for a given frame size with respect to semiconductor area placed in the module could be different. Furthermore, it is expected that the die size of a SiC transistor at 1200 V, for example, comes down to one tenth or less of the area needed in the current Silicon-based IGBT technology, assuming the same total losses for both options. This will result in a huge increase in power and current density, and will require more efforts with respect to an effective heat removal and the connection of chips to terminals.

SiC diodes

Several new generations of SiC Schottky diodes have been introduced since the first launch in 2001, each leading to a further increase in power density. Since 2006, Infineon has been using a Merged-Pin-Schottky (MPS) structure [1] for 600/650 V diodes, mainly in order to offer a sufficient surge-current capability. Other devices on the market are designed as JBS (Junction Barrier Schottky) diodes; from a design point of view, the layout is similar, the difference being that the main purpose of a JBS is to shield the electric field in reverse mode from the Schottky interface in order to keep the leakage current low, while in an MPS the main purpose is to offer surge current. In these diodes, only a part of the active area is used for the current flow; the rest is passive, being in operation in the MPS for only a short period of time (pulse mode). This again represents a further local increase in the current density, as shown in Figure 1 using the basic principle of the MPS diode as an example.

The shown values today are close to the highest current densities for silicon power parts, which are known from low voltage transistors (e.g. 25 V at around 1300 A/cm²).Taking into account the voltage drop at operating temperature (which can

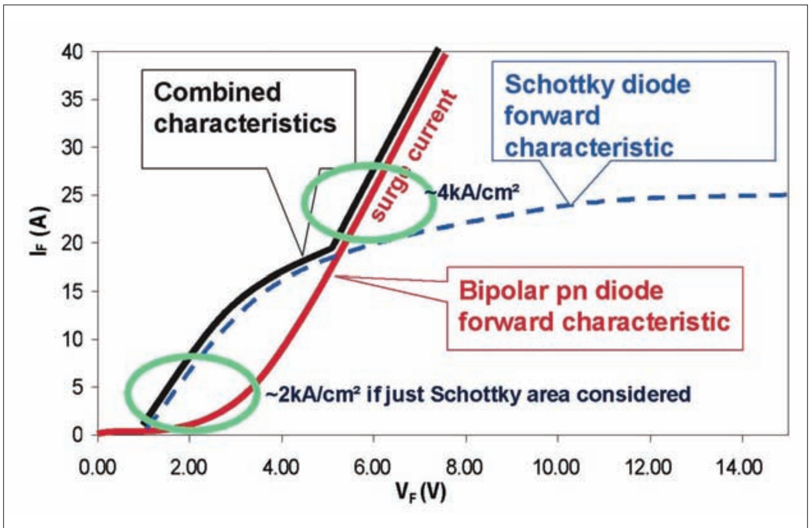


Figure 1: Current densities in recent generations of Infineon's 650 V MPS diodes (3G and 5G devices)

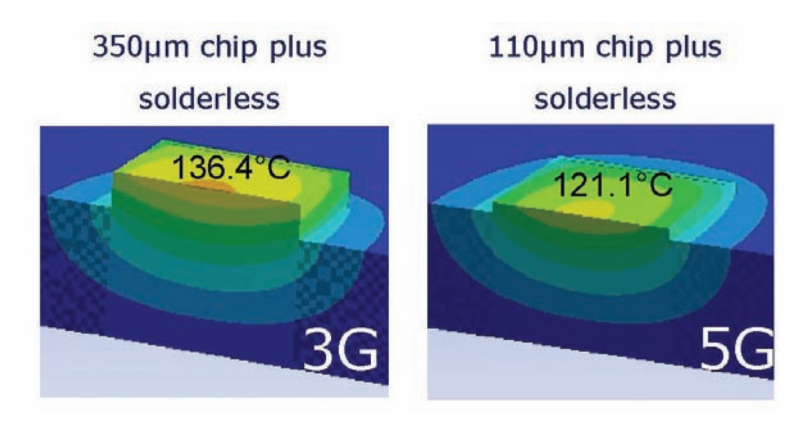


Figure 2: Chip thickness shrink effect on the maximum temperature of an SiC diode with 5.1mm² area on a copper lead frame and a power stress of 170 W; due to the smaller die thickness, the effective R_{th} is reduced

be > 2V), it becomes obvious that heat generated by the power density at the chip with >2kW/cm² can be effectively removed only if effective heat spreading is implemented between junction and case.

Another aspect of modern device design is the reduction of the die thickness. In the special case of vertical SiC devices, the active layer is just a few µm thick, and thus any additional material below it is merely an increase in the (differential) on-resistance and the thermal resistance of the chip [2]. It is thus reasonable to thin the wafers down to the smallest possible value, often defined by the handling capability in manufacturing. Infineon introduced thin (110 µm) wafer devices with its 5th diode generation (5G), offering a further step in power density, as shown in Figure 2.

But this benefit has a drawback – the thermal capacitance, which is important under pulse current stress, is also reduced due to the shrunken volume of the semiconductor. Technologies must therefore be developed to compensate for this, otherwise only reduced pulse ratings are possible. One approach is a good thermal connection of the chip to the lead frame, e.g. by solderless assembly technique, enabling the utilization of the underlying copper as a support for pulsed operation [3].

SiC transistors

The focus today is on the implementation of unipolar high-voltage (600 V … 1700 V) transistors, offering threshold-free linear I-V characteristics, integrated body diodes, and negligible dynamic losses compared to the competing Si-IGBT technology. The Ron x A values expected for 600 V components that seem to be achievable long term are around 1mΩcm² [4]. The benchmark with the above-mentioned low-voltage Silicon technology shows that such values are still a factor of 20 higher than the best-in in-class devices for 25 V today. So it seems that experience with Silicon is sufficient to handle high current densities for SiC transistors.

Nevertheless, one mode of operation will need closer attention. It seems to be mandatory for the success of SiC transistors in industrial applications to operate the internal body diode as a freewheeling diode. There might be some concerns regarding efficiency in this operation mode, because the forward voltage drop is too high; however, one can turn on the channel after a short dead time and then the I-V characteristic in reverse mode is identical to or even slightly better than in forward mode (see Figure 3).

Anyway, there might be a critical situation should the driver circuit fail when diode mode is required by the system. To cope with this mode, one may be forced to define the actual current rating, not from the attractive threshold-less forward I-V, but out of the power handling capability in reverse mode. Thus, lowest VF is required, or alternative solutions for designing the diode function in the 3rd quadrant mode must be developed.

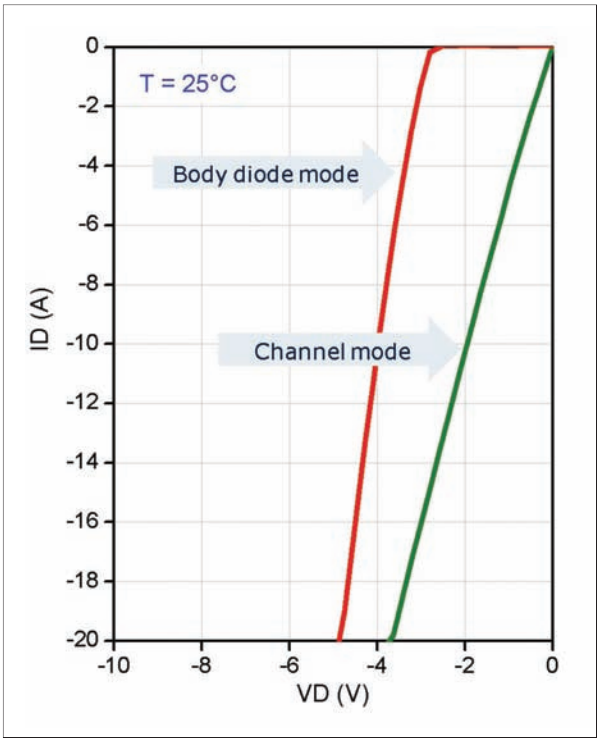


Figure 3: SiC transistors (example SiC JFET from Infineon) in 3rd quadrant – channel mode possible to reduce losses by turning on the channel in freewheeling operation; however, in critical modes the I-V in diode mode might define the current handling capability

High-frequency optimization

Real power circuits with SiC chips inside contain inductance and capacitance as major parasitic elements, and these cause serious deviations from perfect switching. Basic effects of parasitic inductance are:

- a voltage dip during turn-on of a transistor, caused by rise of current
- a voltage spike during turn-off of a transistor, caused by current fall
- the parasitic capacitance together with the inductance form resonant circuits, which show damped oscillations after each switching transition

The effect of parasitics is already more pronounced when a combination of an IGBT with an SiC freewheeling diode is considered, since the diode performance also speeds up the transistor and thus, under improper conditions, oscillations could be observed as seen in Figure 4 (left side) when no special precautions are taken. Therefore, an optimum circuit design with minimum parasitic inductance is a prerequisite for the optimization of power semiconductors towards lowest losses [5].

To meet these demands, rules were

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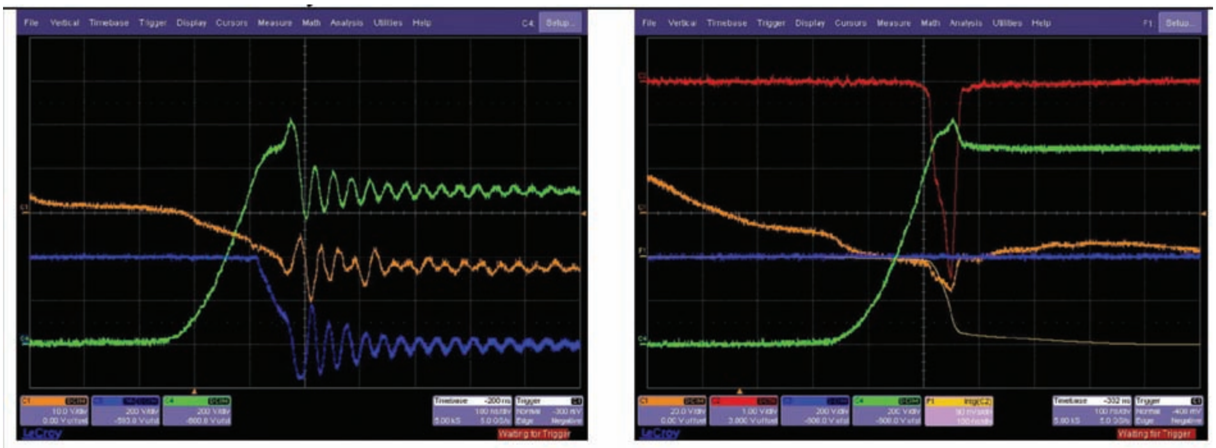


Figure 4: Left - standard module switched with 400 A (turn-off) and a DC link bias of 700 V; the green trace shows the voltage; blue (left) or yellow (right) the current; and orange the gate signal. Right - new module approach, DC link bias now 900 V

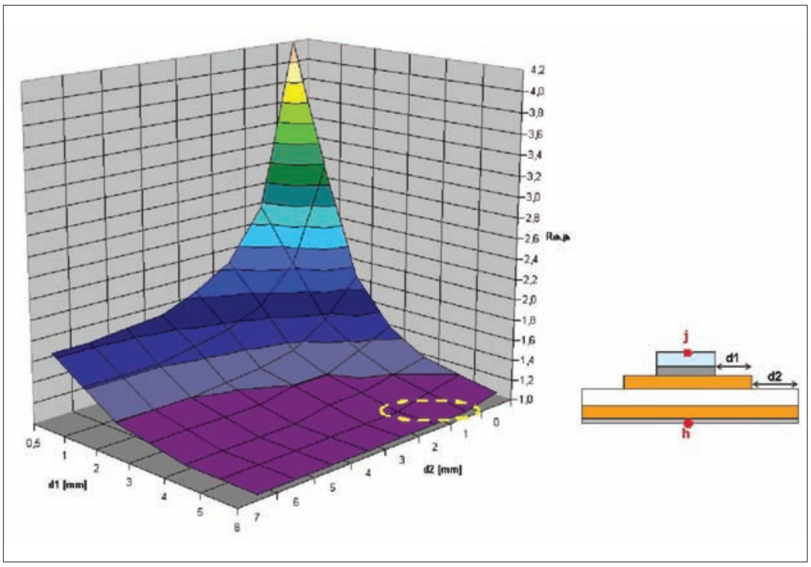
developed at Infineon [6] for the design of power modules. It is well known that a strip-line type of circuit design brings parasitic inductance to a low value, depending on width and distance of the strip line [7]. The graph on the right in Figure 4 shows the effect on the switching performance of power semiconductors of an improved module layout, taking these considerations into account. Whereas, in the standard module, a severe over-voltage peak plus oscillations are observed, the new solution can eliminate these effects almost completely. It has to be noted that the improvement was achieved without changing the chip technology, but simply by a more careful design of the package. These considerations will also take into account the fact that, on the midterm scale, paralleling of a high number of dies will be the preferred method of achieving higher power levels in SiC.

In order to avoid a degradation of the high performing SiC chips by an unsuitable environment, Infineon will drive the implementation of SiC semiconductors only in module platforms that enable this approach.

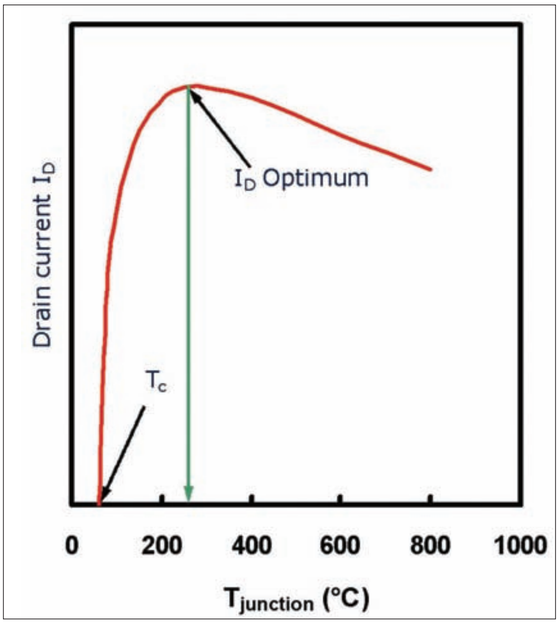
Thermal considerations

The final power-handling capability of a semiconductor module is defined by the chip area inside the module combined with the thermal performance expressed by the R_{th}. For Silicon chips, as much as possible chip area is usually placed on a given footprint in a power module, because normally the area cost per chip is not so much different from the cost per module area, mainly for larger power ratings.

In the case of SiC, different considerations apply. The chips are much more expensive than Silicon ones, so it is beneficial to choose a different ratio of chip area to module area to get the optimum solution with respect to the price/power ratio for a given footprint. The reason for this is that, by proper design, the effective R_{th} per chip can be reduced by a factor of up to 4 due to heat spreading effects, as shown in Figure 5 (base-plate-free module).



ABOVE Figure 5: Effective thermal resistance for a configuration in a base-plate-free module. Setup shown on the right side. A 0.32 mm thick ceramic with 0.6 mm Cu on both sides is assumed



LEFT Figure 6: Extractable current from a system with a given R_{th} and T_c, the component having a dependence of its on-resistance on temperature with an $R \sim T^2$ law

In addition, there is a trend towards higher maximum chip temperatures, in order to increase the removable heat for a given die area, and thus its current-handling capability. It must be mentioned that doing this will increase the absolute losses, so that efficiency targets could be violated, depending on the ratio of loss increase to increase in power-handling capability. In contrast to IGBTs, this loss increase might be huge for unipolar SiC devices, because now a resistive component with a heavy increase in the R_{on} with temperature is in place, mostly with a power law in the form of $R_{on} \sim T^x$, with x values between 2 and even 2.5, as recently presented for high voltage SiC MOSFETs.

Taking this into account, one can see that, for unipolar devices, a continuous increase of Tj can even lead to a reduction in current-handling capability, because more power is dissipated than can be removed by the increase of T_j. Figure 6 shows this result for a typical dataset, assuming x=2 as the exponent in the power law for the increase of the resistance with temperature.

In addition to these considerations, it is known that the reliability of power systems, mainly the power cycling capability, is degraded when the temperature swing between off state and maximum temperature is increased [8]. Thus, for the sake of both efficiency and reliability, it might be wiser to offer good cooling and keep the temperature differences in the thermal stack low.

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MOSFETs Make Step Change in Performance to Meet New Application Requirements

Low voltage MOSFET devices (<40 V) are used extensively in the power systems of portable electronic devices, domestic appliances, data communication servers, medical equipment and telecom infrastructure deployments. Exacting demands continue to be placed on the engineers involved in the design of such MOSFETs. The article will look at the forces at work and how significant, yet potentially conflicting, technical challenges need to be tackled. **Wharton McDaniel, Product Marketing Manager Power MOSFETs, ON Semiconductor, Phoenix, USA**

Our everyday lives are now almost totally reliant on the use of various forms of electronics equipment, however there are major concerns about the rise in worldwide energy consumption that this is leading to - its depletion of fossil fuels, the impact it has on the environment (in terms of carbon emissions, etc.) and the enlargement of utility bills too. Greater consumer awareness, the implementation of hard-hitting legislative measures (such as EnergyStar), plus OEMs' testing performance roadmaps, are all compounding the acute pressure being placed onto power semiconductor manufacturers. Next generation of power systems will consist of components that possess a number of highly favorable attributes.

Important drivers

There are two main dynamics that are currently responsible for defining MOSFET development. On one side you have the high end processing being required by sever farms. Here the power demand and density of the microprocessors found in racks has grown immensely - presenting electricity consumption, real estate and thermal management obstacles that need to be overcome. Conversely, in computing it is not the processing capacity that is now the main concern. As computer platforms have migrated from bulky desktop PCs to lightweight, streamlined portable products, such as tablets and smartphones, this is no longer the key selling point for customers. The criteria by which the power systems are outlined have changed here, with battery life and system compactness now being prioritized. The switching frequencies of both these types of power systems must be raised, so that smaller magnetics and passive components can be used, with less space thus needing to be allocated.

Having established what the drivers are at the application level, how does this translate into the components specs? There are three main parameters which should be scrutinized when specifying MOSFETs for a power system. These are:

1. On resistance (R_{DSON}) is vital when it comes to mitigating a MOSFET's conduction losses, so this should be as low as possible.
2. Figure-of-Merit (FOM) - defined by R_{DSON} x Q_G (total gate charge), this is an indicator of both the switching and conduction losses of the MOSFET, so it is used as an important selection criteria when deciding on which component to use.
3. Switching performance - The better switching characteristics of the MOSFET are, the lower the switching losses will be. With increased switching frequencies being witnessed all the time, this will become even more crucial in the coming years.

MOSFET design and its implications

MOSFET usage became more common in the 1980's, and in the decades that have passed since then a lot has changed in terms of the way these devices are fabricated and the performance specs they can deliver. Though it is for very different reasons, the MOSFETs serving both of the very disparate applications scenarios we discussed earlier need to dissipate as little power as possible (when active and also when inactive), so keeping R_{DSON} low must be one of the fundamental goals. Support very high conversion efficiencies is also a huge plus point, as is having a small die size - as in both portable products and server implementations board space is at a premium. The question is how to go about achieving this performance 'wish list' at the component level.

There are two elementary constituents that MOSFET design can be broken down into. In the past it was possible for component manufacturers to get away with just doing one of these really well, then dealing with the other solely as an afterthought. Now though they need to be addressed simultaneously, with equal emphasis.

Process technology - ten years ago a CPU generally required a current of around 10 A to drive it, today it is more likely to be 100 A. This has dictated an order magnitude reduction in R_{DSON} simply to keep form factors and heat dissipation levels in check, otherwise a substantial expansion in the size and cost of electronic equipment would have been unavoidable. Furthermore, a MOSFET's overall switching performance can be greatly augmented through a reduction in its capacitances. Continued development of new semiconductor processes have allowed the MOSFET R_{DSON} and capacitance reductions needed by OEMs to be realized. These reductions should remain scalable - keeping pace with smaller semiconductor geometries for the foreseeable future. The advent of shielded-gate trench topology is helping to keep the industry ahead of the game, with features which minimize switching overshoot, complementing the lowered R_{DSON}. With switching frequencies rising, as already stated, overshoot is becoming more of an issue, so this topology's ability to mitigate its effect is highly advantageous.

Package technology - a great deal of

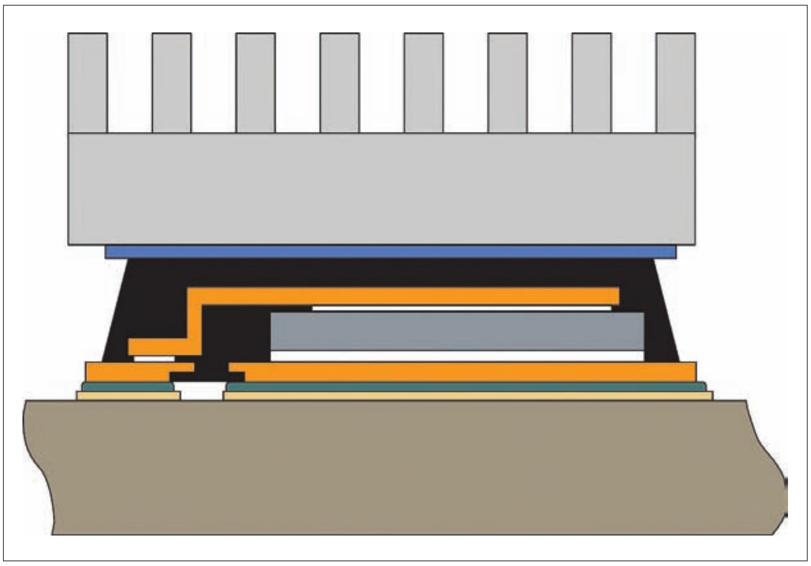


Figure 1: **Thermally enhanced SO8FL package with heatsink**

effort must be put into curbing the interconnect and thermal resistances of any power MOSFET package. The interconnect resistance has to be minimized with respect to the R_{DSON} values of the die (especially as we are now reaching sub milliohm levels) - otherwise any improvement in the Silicon will not be worthwhile. The use of clips in place of bondwires has been the main means of keeping interconnect resistance as a small percentage of the total RDSON. The exposed pad on the bottom of surface mount packages provides the primary low resistance thermal path. Now there are surface mount packages which have reduced thermal resistance to the top of the package, allowing heatsinking from the top of the package (see Figure 1). This type of package is important where the PCB cannot be an effective heatsink. It is clearly no good if semiconductor expertise has managed to provide strong performance qualities only to then be let down by poorly implemented packaging.

The continuing reduction in die size over the years brought on the migration from leaded power packages, such as TO220, to surface mount packages for single MOSFETs and now to dual packages. High power phase pairs of MOSFETs now are available in 5 mm x 6 mm packages. Performance is enhanced due to the reduction of the interconnect resistances and inductances. Also, this gives the designer a great advantage where space is at a premium as is shown in Figure 2.

The specification of MOSFETs which offer engineers an optimized balance of conduction loss characteristics and switching efficiency can prove vital to end product development. Utilization of the latest semiconductor processes and packaging technologies have helped to minimize the losses being experienced as well as reducing the energy dissipated from system designs so that the accompanying thermal management mechanisms take up less space. This means that the end products can be placed in to sleeker, less cumbersome form factors. Also greater system reliability and longer lifespan can be assured.

Conclusions

In conclusion, there needs to be continued investigation and then implementation, within the power electronics arena, of more effective ways by which to curb the losses that are related to the MOSFET switching activity and improve conversion efficiency levels, while simultaneously reducing R_{DSON}. Technological progression is enabling processes where both R_{DSON} and the capacitances associated with the switching circuit can both be lowered substantially. The upshot of this is that the PCB area that needs to be utilized and switching performance characteristics are both being improved as more compact passive components can be employed and higher switching frequencies can be utilized. Difficulties still lie ahead, however - eventually die sizes will start to get so small that the approaches to interconnect and thermal management will have to change dramatically again.

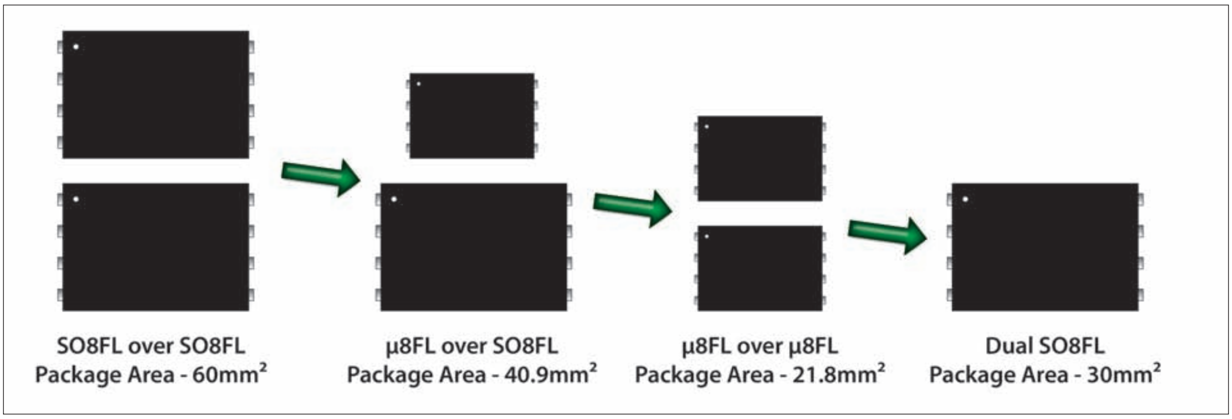


Figure 2: **Progression of package technology**

Fine Tuning of Digital Control in POL Regulators Optimize Dynamic Response and Minimize Component Count

Power system design encompasses many requirements and criteria. This article is about perhaps the most basic of all requirements – a stable voltage supply of the operating circuitry. **Patrick Le Fèvre, Ericsson Power Modules, Sweden**

Each electronic circuit on the printed circuit board (PCB) is designed to operate over a limited range of DC voltage, outside of which circuit operation or performance is not guaranteed. A generalized view of the static voltage and associated tolerance is shown in Figure 1.

In order to achieve high speed and low power dissipation, recent microprocessor , DSP and FPGA chips require voltage levels of 1 to 3.3 VDC with a tolerance of as little as ±30 mV. These types of requirements place severe demands upon the power system.

Dynamic response

Most types of circuits demand dynamic input current for short periods of time. The power system is designed to handle fast dynamic current by means of decoupling capacitors located in proximity of the electronic circuits, while the power supply handles low frequency and longer duration dynamic demands (see Figure 2).

The power supply control loop, the distribution impedance and the decoupling capacitors decides how the dynamic current is shared between the decoupling capacitance and the power supply.

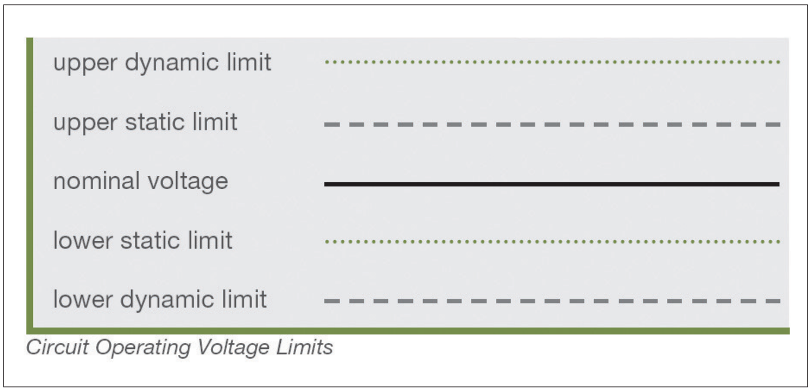


Figure 1: **Circuit operating voltage limits**

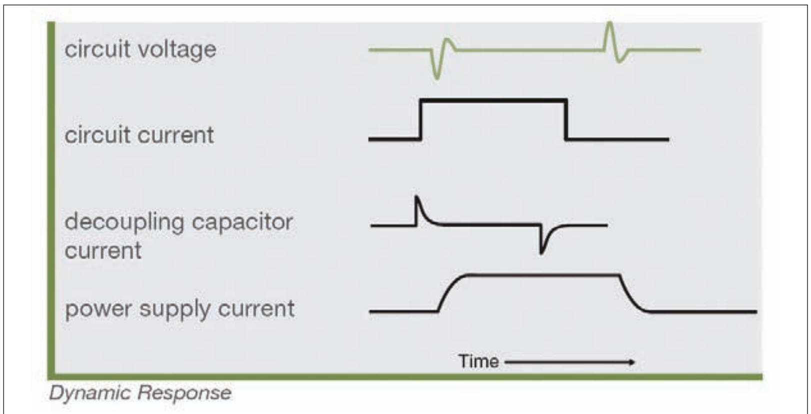


Figure 2: **Principals of dynamic response**

Digital control of POL regulators

Digital control is not a magic wand that can twist the physical laws, but it makes it possible to improve and optimize the dynamic response performance because the digital protocol does not have to take into account any tolerance problems which are the case for the capacitive and resistive networks used in analog control loops.

Ericsson now offers a useful software tool that designs, simulates, analyses and configures the POL regulator within minutes. It includes simple tools for robust design of control loops, together with more advanced design and analysis tools to optimize the dynamic response performance and minimize the number of decoupling capacitors needed for a certain load transient requirement. The tools are integrated in the DC/DC Power Designer software, enabling quick and efficient automated design and analysis.

Modelling of the POL regulator

The most common topology for POL

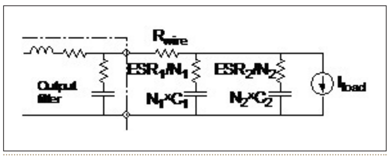


Figure 3: **Model of the power module with external decoupling capacitors**

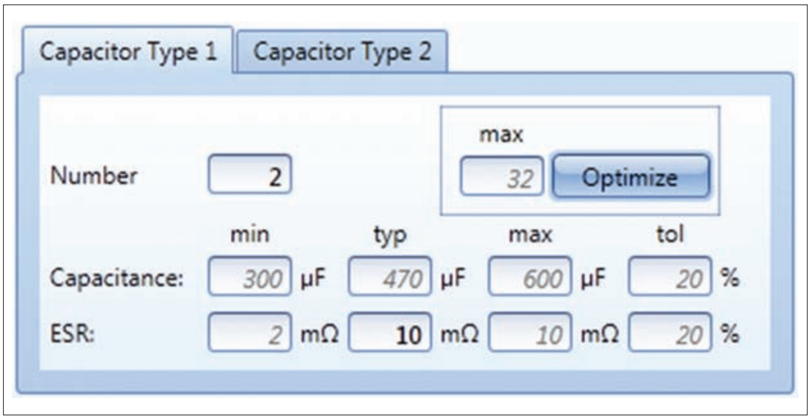


Figure 4: Capacitor description

regulators is the buck converter. The output filter of the POL regulator consists of an internal output capacitance and an additional mix of different types and sizes of decoupling capacitors on the PCB in proximity of the electronic circuits. Figure 3 shows the fundamental schematic. As the decoupling capacitors become a part of the system that should be controlled, they must be included in the model. The model also includes a resistance, R_{wire}, for modelling of the lead resistance on the PCB. Two different types of capacitors are included in the model.

System analyzes and component tolerances

The decoupling capacitors are entered into the tool with capacitance and ESR, including tolerances. Tolerances are important because they define the 'corners' of the system. This is handled by calculating all the corner cases for the power train filter. Figure 4 shows the enter field for capacitor data.

Using two different capacitors, each with tolerances for the capacitance and the ESR, yields a total of 16 corner systems and one typical system. All 17 systems (16 combinations of min/max values, plus one with typical values) are then simulated and evaluated. Each system's natural frequency and damping ratio are then calculated and the results are used as input to the control loop design.

Control loop design

The tool uses a linearized model of the power train and a system transfer function based on a sampled state-space model and the control loop design is fairly straight forward using standard control theory. In today's digital control circuits, the PID regulator is often implemented as second order digital filter, where the integrator part is fixed and in many cases impossible to remove. Hence, the software tool is designed to define the placement of two zeros and the total gain in the loop.

A common tool for open loop design is the Bode plot, shown in Figure 5, in which the compensation zeros are placed to obtaining the proper behavior and adjust the gain to meet the robustness requirements in terms of phase and gain margins. Common values for these requirements are 60°, and 6 dB, respectively.

The tool plots the typical system, analyses all 16 corners systems, and plots the systems with the minimum and maximum values for the phase and gain margin. If all design requirements are fulfilled, a green signal together with the word 'Stable' is shown in the upper left corner, which gives quick answer of the loop stability.

However, the phase and gain margins are not enough for a robust control loop. This cannot be observed in the open loop Bode plot only, but becomes obvious in the closed Bode plot, see Figure 6, and can be handled with additional design requirements.

If the gain becomes too high the system attenuation at higher frequencies stops to be monotonically increasing, and instead starts to increase towards the Nyquist frequency. The Nyquist frequency is $f_s/2$, where fs is the switching frequency. Another indication is that the gain around the system's resonance frequency forms a peak. This results in a sensitive system and output voltage oscillations during transients. This can be avoided if restrictions are put on the peak gain and the gain at the Nyquist frequency. The rules (peak gain < 1 dB; gain at Nyquist <

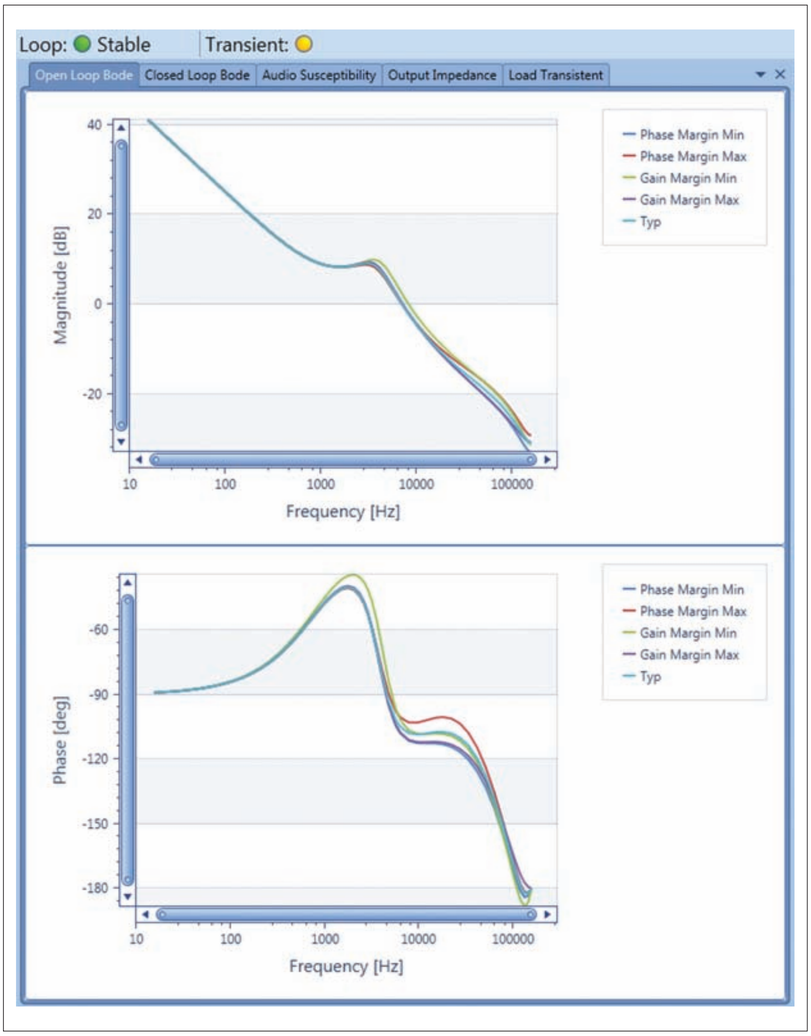


Figure 5: Open loop Bode plot

-6 dB) have been shown in practice to work well.

An additional key figure that is a little coinciding with these former key figures is the bandwidth, which in the past has earlier been used as a rule of thumb (bandwidth < f_s/10) for avoiding oscillations.

This rule of thumb describes the benefits of high switching frequency. Besides the advantage of smaller capacitive and inductive components, higher switching frequency will make it possible to increase the bandwidth of the control loop and thereby improve the dynamic response.

The tool plots the typical system, analyses all 16 corners systems, and plots the systems with the minimum and maximum values for Peak gain, Bandwidth, and Gain at Nyquist frequency.

A common 'rule of thumb' for placement of the control loop's zeros that is robust and gives good transient behavior is:

- Place first compensation real zero at the systems typical resonance frequency
- Place the second real zero one octave below the first zero

This is implemented in the tool for a simple and robust design, which will in many cases be good enough.

The tool also has an Auto gain function, which automatically maximize the loop gain for maximum performance with the design requirements fulfilled for the typical system. This makes the manual design of the zero's placement much easier and quicker.

Dynamic response optimization

In the case of a known system the load transient can be optimized by placing the compensation zeros differently compared with the rule of thumb described above.

A goal function is defined as the weighted sum, w_x, of the voltage deviation, dV, and recovery time, T_{rec}, during load transients and each normalized with the corresponding system requirements:

$$Goal = w_1 \left| \frac{dV}{dV_{req}} \right| + w_2 \left| \frac{T_{rec}}{T_{req}} \right| .$$

The tool picks zero pairs around the systems resonance frequency and uses an iterative method to find the zero pair which gives the smallest Goal value. First a coarse search is made and then a second fine tuning to find the optimum placement.

For each zero pair placement the control loop's gain is designed based on the closed loop Bode analyses described earlier. Then a load transient simulation is performed with the following user defined load transient key figures:

- Low current level [A]
- High current level [A]
- Slew rate [A/µs]
- Load transient period [ms]

The zeros placements with the smallest Goal value will result in a design with optimized dynamic response.

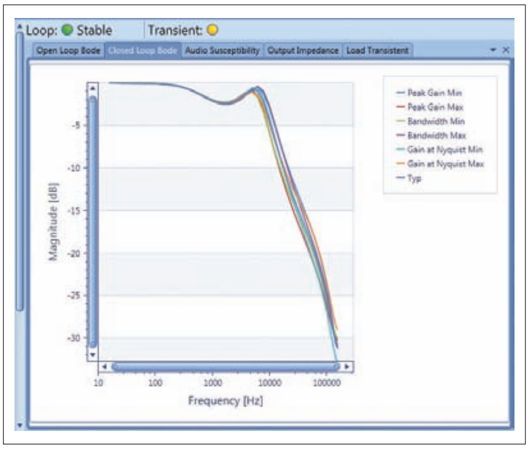


Figure 6: Closed loop Bode plot

Minimizing the decoupling capacitance

The tool can also be used in the design of the decoupling capacitance network by determining the type and number of capacitors and capacitance that is needed in order to meet the load transient requirements. Decoupling capacitors occupy expensive area on the PCB and is also adding to the system cost. Therefore it is important to optimize the system design for minimum decoupling capacitance and number of capacitors.

Design examples

The first example shows the difference between dynamic response at load transients with standard PID settings and optimized settings. The conditions are:

- 2 pieces of 470 µF, 10mΩ
- 8 pieces of 100 µF, 5mΩ
- Input voltage is 12V, output voltage 1.0 V.

With the default PID settings and a 5-15 A load step, with a slew rate of 10 A/µs, gives the voltage deviations and recovery time shown to the left in Figure 7. Using the tool's rule of thumb for placement of the controller's zeros gives the result shown to the right. This shows the potential of optimizing PID for a known load, where in this case, the voltage deviations are halved and the recovery times are reduced with a factor of three.

Using the load transient optimization with equal weights for voltage deviations and recovery time yields the following results shown in Figure 8, which shows that the recovery time can be improved further without significantly increasing the voltage deviations.

The second design example shows how it is possible to reduce the decoupling capacitance and number of capacitors and still improve the dynamic response performance.

Using the tool's 'rule of thumb' PID

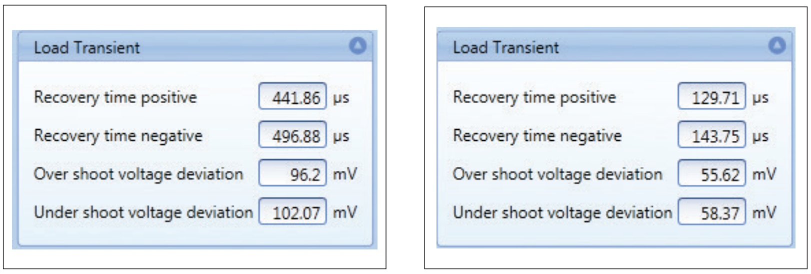


Figure 7: Default PID setting (left) vs. "rule of thumb" PID setting

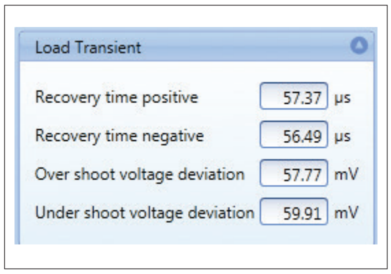


Figure 8: PID settings optimized for best dynamic response

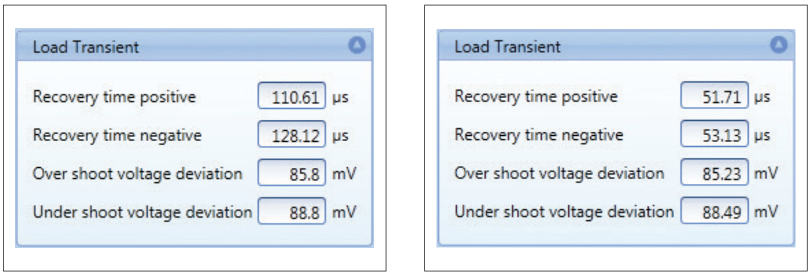


Figure 9: Optimized PID for minimum decoupling capacitance (left), further improvements could be done with the optimized PID settings as shown to the right

settings the number of capacitors can be reduced to one 470 µF and six 100 µF. As the tool runs the optimization for the worst case system, the load transient on the typical system has a margin compared with the load requirements, shown to the left in Figure 9. Further improvements could be done with the optimized PID settings as shown to the right in Figure 9. The result shows that the recovery times are halved and still with maintained voltage deviations.

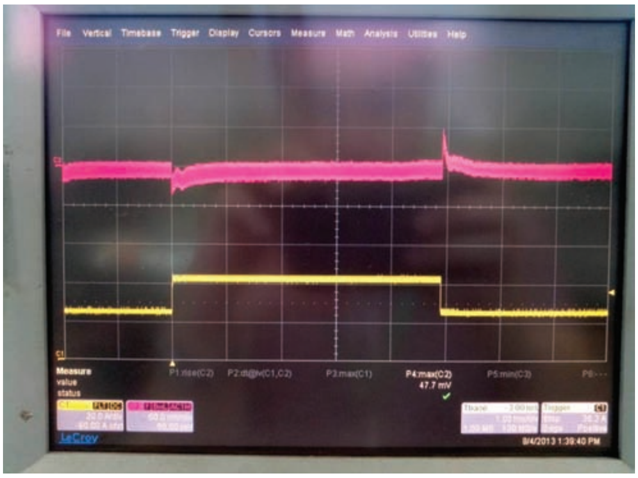


Figure 10: V_{out} deviation with default PID settings and 5,000 µF

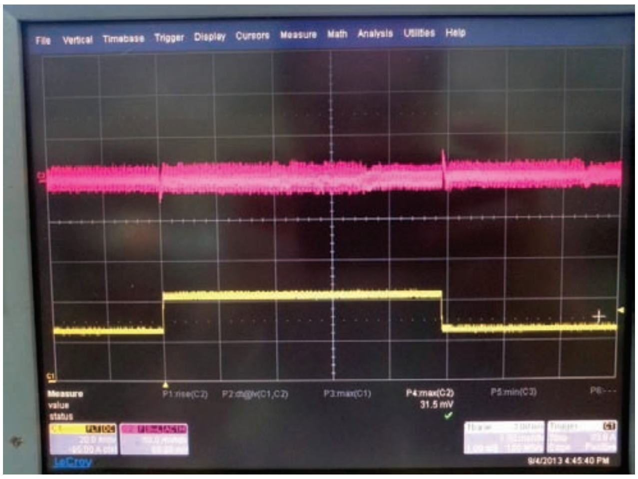


Figure 11: Dynamic response with optimized PID settings and reduced decoupling capacitance

Customer application example

The tool has been used in actual customer applications with very good results. This example shows the improvements achieved using two paralleled Ericsson BMR464 POL regulators with optimized PID settings compared with the default settings.

System requirements:

- V_{in} = 12 V
- V_{out} = 1.0 V
- Current transient 26 to 44 A with 1.8 A/µs slew rate
- V_{out} tolerance = ±3 % (±30 mVp-p)

With the default PID settings and 5,000 µF electrolytic capacitors the measured Vout deviation was 48 mV (see Figure 10).

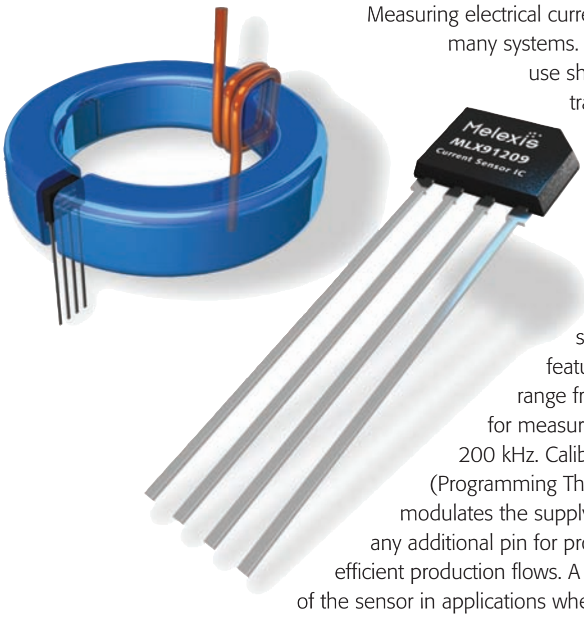
With optimized PID settings and reduced decoupling capacitance with 1,000 µF ceramic capacitors and two electrolytic capacitors with 1,000 µF respective 470 µF capacitance the V_{out} deviation is improved to 32 mVp-p (see Figure 11).

Conclusions

The default wide range PID that Ericsson POL regulators are delivered with is designed for robust and stable operation. With the described tool integrated in the Ericsson DC/DC Power Designer software it is possible for the power system designer to fine tune the POL regulator's control loop in the particular application and significantly improve and optimize the dynamic response performance and/or reduce the required decoupling capacitance.

Fewer output decoupling capacitors can be used to insure a given voltage tolerance which means lower component cost and most importantly it will also have a huge impact and pay-off in terms of reduced time-to-market and increased system packaging density.

Linear Hall Current Sensor



Measuring electrical current in a conductor is critical to many systems. Classic measurement techniques use shunt resistors, current transformers or magnetic field sensors. Hall effect sensors are frequently the choice when measuring DC currents. However the new, improved MLX91209CA can be applied in all current sensing situations. This versatile, high speed Linear Hall IC, which features a programmable sensitivity range from 5 to 150 mV/mT, is suitable for measuring DC and AC currents up to 200 kHz. Calibration is done using PTC (Programming Through Connector) protocol. This modulates the supply voltage and does not require any additional pin for programming, enabling the most efficient production flows. A linear analog output permits use of the sensor in applications where a very fast response of 3 μs is required. Custom calibration is best performed in-situ after the sensor is fixed with respect to the current conductor and ferromagnetic core so that a calibrated current sensitivity is achieved. Typical accuracy of a current sensing system based on the MLX91209 is better than ±0.5 % at room temperature or ±2 % over the full temperature range (from -40°C to 125°C) when applying in-circuit end of line calibration.

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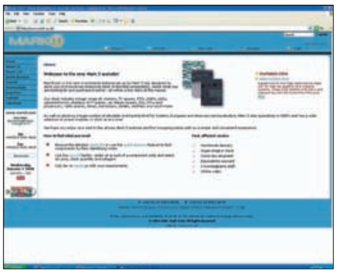

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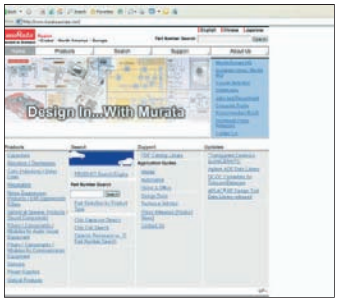

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Ultra-Low $R_{DS(ON)}$ Automotive COOLiRFET™

Package	$R_{DS(on)}$ Max@ 10Vgs (mΩ)	Q_G Typ (nc)	I_D Max (A)	RthjC Max	Part Number
D²PAK-7P	0.75	305	240	0.40°C/W	AUIRFS8409-7P
	1.0	210	240	0.51°C/W	AUIRFS8408-7P
	1.3	150	240	0.65°C/W	AUIRFS8407-7P
D²PAK	1.2	300	195	0.40°C/W	AUIRFS8409
	1.6	216	195	0.51°C/W	AUIRFS8408
	1.8	150	195	0.65°C/W	AUIRFS8407
	2.3	107	120	0.92°C/W	AUIRFS8405
	3.3	62	120	1.52°C/W	AUIRFS8403
TO-262	1.2	300	195	0.40°C/W	AUIRFSL8409
	1.6	216	195	0.51°C/W	AUIRFSL8408
	1.8	150	195	0.65°C/W	AUIRFSL8407
	2.3	107	120	0.92°C/W	AUIRFSL8405
	3.3	62	120	1.52°C/W	AUIRFSL8403
TO-220	1.3	300	195	0.40 °C/W	AUIRFB8409
	2.0	150	195	0.65 °C/W	AUIRFB8407
	2.5	107	120	0.92 °C/W	AUIRFB8405
DPAK	1.98	103	100	0.92 °C/W	AUIRFR8405
	3.1	66	100	1.52 °C/W	AUIRFR8403
	4.25	42	100	1.90 °C/W	AUIRFR8401
IPAK	1.98	103	100	0.92 °C/W	AUIRFU8405
	3.1	66	100	1.52 °C/W	AUIRFU8403
	4.25	42	100	1.90 °C/W	AUIRFU8401

The new International Rectifier AEC-Q101 qualified COOLiRFET™ technology sets a new benchmark with its ultra-low $R_{DS(on)}$. The advanced silicon trench technology has been developed specifically for the needs of automotive heavy load applications offering system level benefits as a result of superior $R_{DS(on)}$, robust avalanche performance and a wide range of packaging options.

The COOLiRFET™ Advantage:

- Benchmark $R_{DS(on)}$
- AEC Q101 qualified
- High current capability
- Robust avalanche capability

Key Applications:

- Electric power steering
- Battery switch
- Pumps
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- Heavy load applications

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